μPD7501
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7501 4-bit, single-chip CMOS microcomputer has advanced fourth-generation architecture with the functional blocks necessary for a single-chip controller, including an 8-bit timer/event counter, an 8-bit serial I/O, and an LCD display controller/driver.

The μPD7501 contains two 4-bit general-purpose registers outside of RAM. The μPD7501 executes a subset of the μPD7500 series B instruction set with a 10-μs instruction cycle time.

Maximum power consumption is 900 μA at 5 V and 300 μA at 3 V. The HALT and STOP instructions further reduce power consumption.

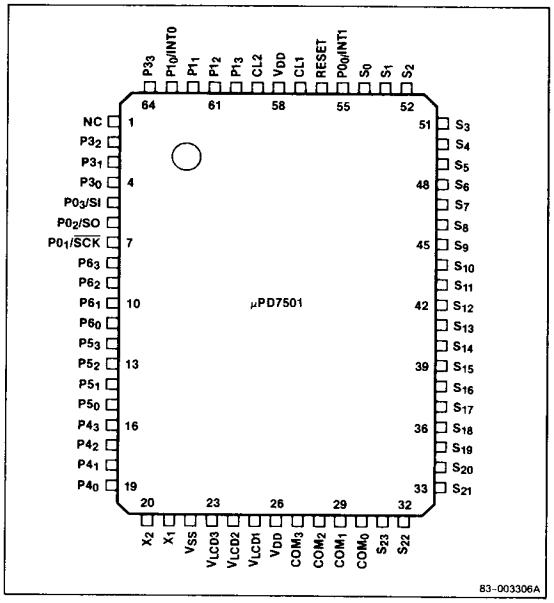
Features

- ☐ 1024 x 8-bit program ROM
- ☐ 96 x 4-bit data RAM
- ☐ Interrupts
  - —External: INT0, INT1
  - —Internal: INTT (timer/event counter), INTS (serial interface)
- ☐ 8-bit timer/event counter
  - —Based on crystal oscillation
  - —External event counter (prescale option by 64)
- ☐ Serial interface
- ☐ LCD controller/driver
  - —Programmable multiplexing mode: triplex or quadruplex
  - —4 common lines (COM_0-COM_3)
  - —24 segment lines (S_0-S_{23})
- ☐ Standby modes: stop, halt
- ☐ Data retention mode
- ☐ I/O ports
  - —3 input ports
  - —1 output port
  - —3 I/O ports
- ☐ RC oscillation clock
- ☐ Crystal oscillation clock
- ☐ 2.5 to 6.0 V operating voltages
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7501G-12	64-pin plastic miniflat	410 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2-4, 64	$P3_3$-$P3_0$	Output port 3
5-7, 55	$P0_3$/SI $P0_2$/$\overline{SO}$ $P0_1$/$\overline{SCK}$ $P0_0$/INT1	Input port 0, serial I/O interface, external interrupt
8-11	$P6_3$-$P6_0$	I/O port 6
12-15	$P5_3$-$P5_0$	I/O port 5
16-19	$P4_3$-$P4_0$	I/O port 4
20, 21	X2, X1	Crystal clock/external event input
22	V_{SS}	Ground
23-25	V_{LCD3}-V_{LCD1}	LCD bias voltage inputs
26, 58	V_{DD}	Positive power supply
27-30	COM_0-COM_3	LCD backplane driver outputs
31-54	S_{23}-S_0	LCD segment driver outputs
56	RESET	Reset input
57, 59	CL1, CL2	System clock input
60-63	$P1_3$-$P1_1$ $P1_0$/INT0	Input port 1, external interrupt

Pin Functions

$P0_3$-$P0_0$ [Input Port 0]; SI, SO, $\overline{SCK}$ [Serial I/O Interface]; and INT1 [External Interrupt]

This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT1. If $P0_0$/INT1 is unused, it should be connected to V_{SS}. If $P0_1/\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_3$-$P1_0$ [Input Port 1] and INT0 [External Interrupt]

Four-bit input port. Line $P1_0$ is shared with external interrupt INT0, a rising edge-triggered interrupt. If $P1_0$/INT0 is unused, connect it to V_{SS}. If $P1_3$-$P1_1$ are unused, connect them to V_{SS} or V_{DD}.

$P3_3$-$P3_0$ [Output Port 3]

Four-bit latched three-state output port 3. Leave unused pins open.

$P4_3$-$P4_0$ [I/O Port 4]

Four-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [I/O Port 5]

Four-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [I/O Port 6]

Four-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

COM_3-COM_0 [LCD Backplane Driver Outputs]

Leave unused pins open.

S_{23}-S_0 [LCD Segment Driver Outputs]

Leave unused pins open.

V_{LCD3}-V_{LCD1} [LCD Bias Voltage Inputs]

LCD bias voltage supply to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}. Leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input event pulses to X1 and leave X2 open. If X1 is not used, leave it open. If X2 is not used, connect it to V_{SS}.

CL1, CL2 [System Clock Input]

Connect an 82-kΩ resistor across CL1 and CL2, and connect a 33-pF capacitor from CL1 to V_{SS}. Alternatively, connect an external clock source to CL1 and leave CL2 open.

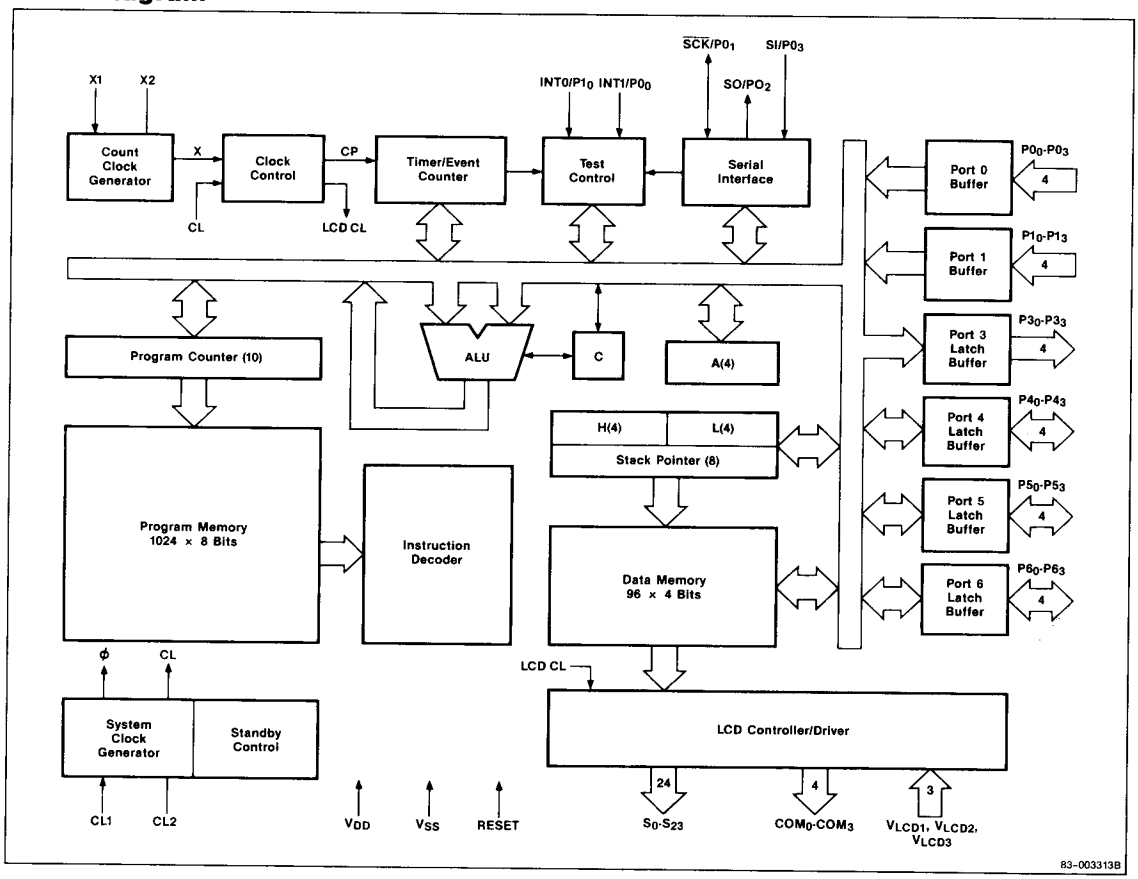
RESET [Reset Input]

A high-level input to the RESET pin initializes the μPD7501 after power-up.

V_{DD} [Positive Power Supply]

Apply a single voltage in the range +2.7 to +6.0 volts for proper operation.

Block Diagram



Details of some blocks on the diagram are illustrated in figures 1 through 6 as listed below.

Figure	Title
1	Interface at Input/Output Ports
2	Clock Control
3	Timer/Event Counter
4	Test Control
5	Serial Interface
6	LCD Controller/Driver

Figure 1. Interface at Input/Output Ports

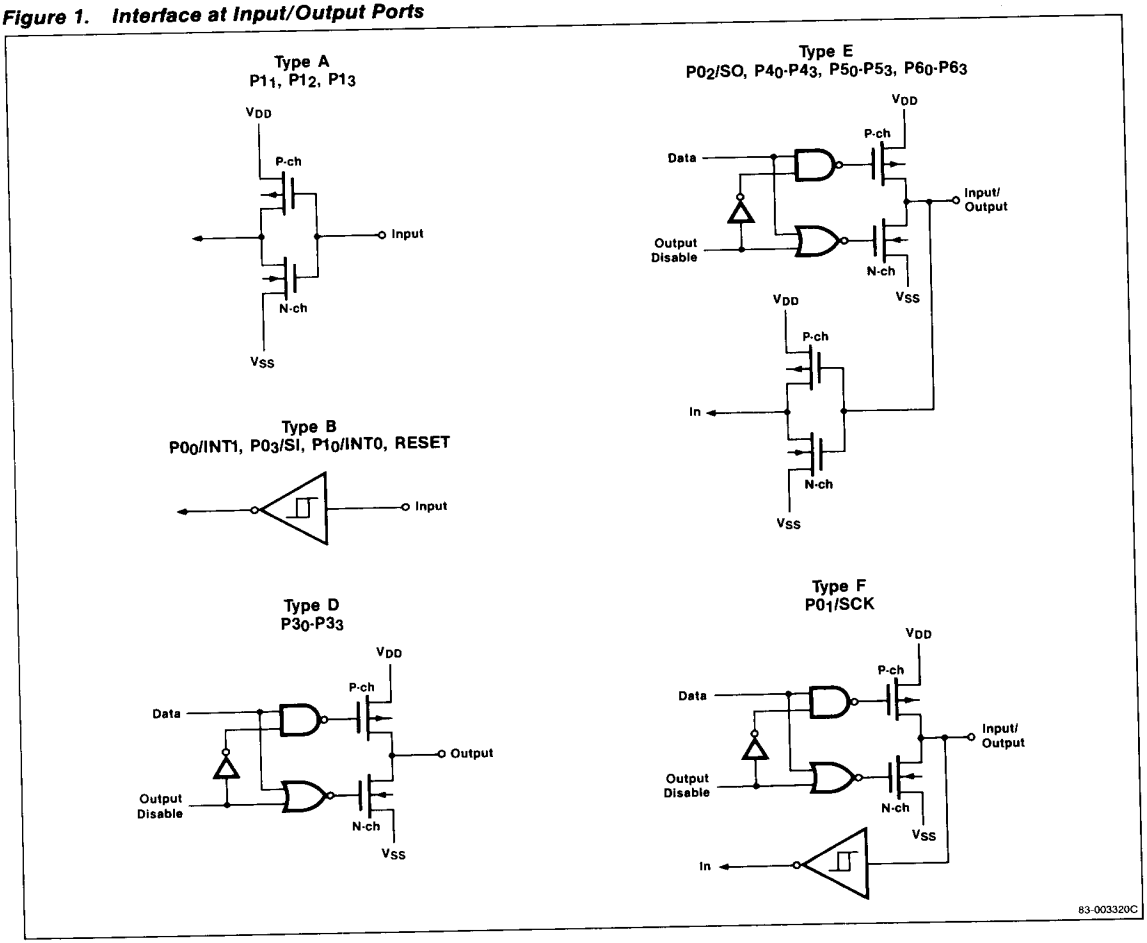
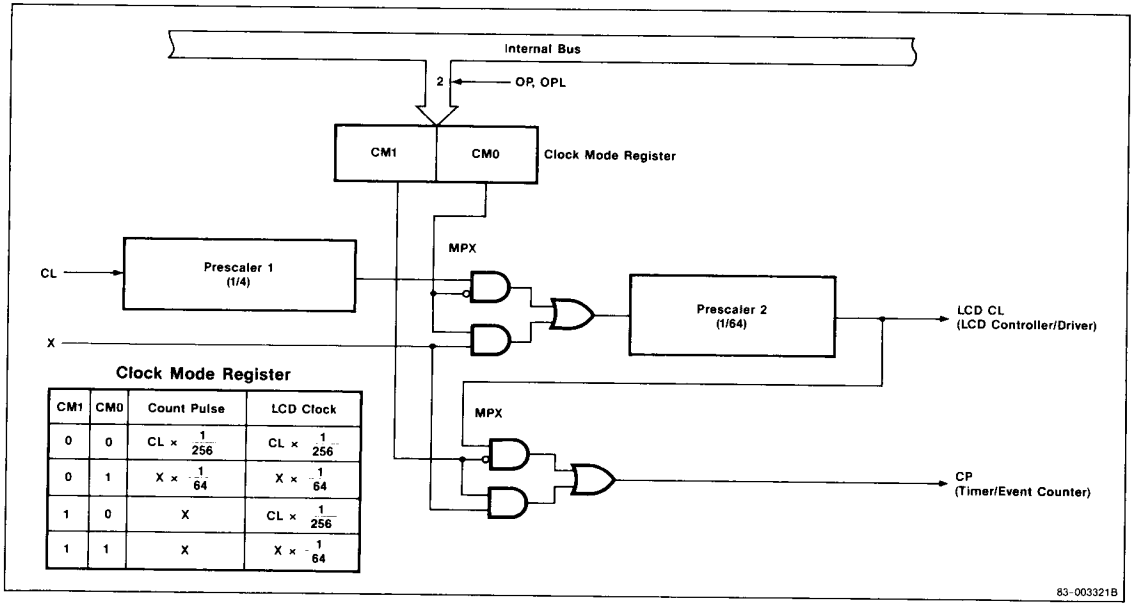


Figure 2. Clock Control



Clock Mode Register

CM1	CM0	Count Pulse	LCD Clock
0	0	CL × $\frac{1}{256}$	CL × $\frac{1}{256}$
0	1	X × $\frac{1}{64}$	X × $\frac{1}{64}$
1	0	X	CL × $\frac{1}{256}$
1	1	X	X × $\frac{1}{64}$

Figure 3. Timer/Event Counter

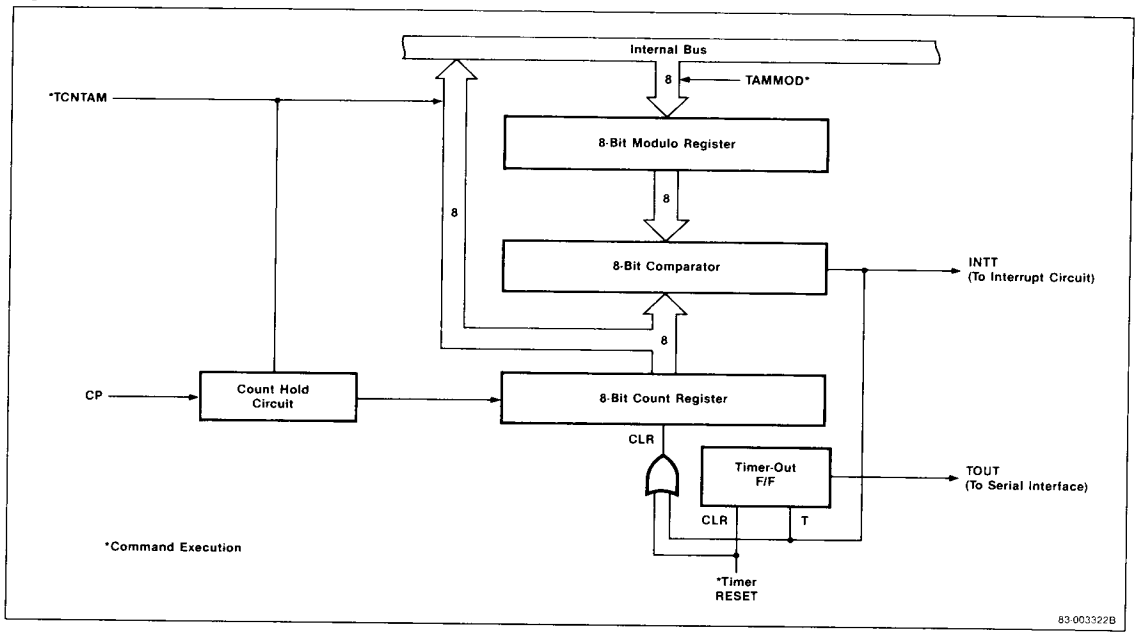


Figure 4. Test Control

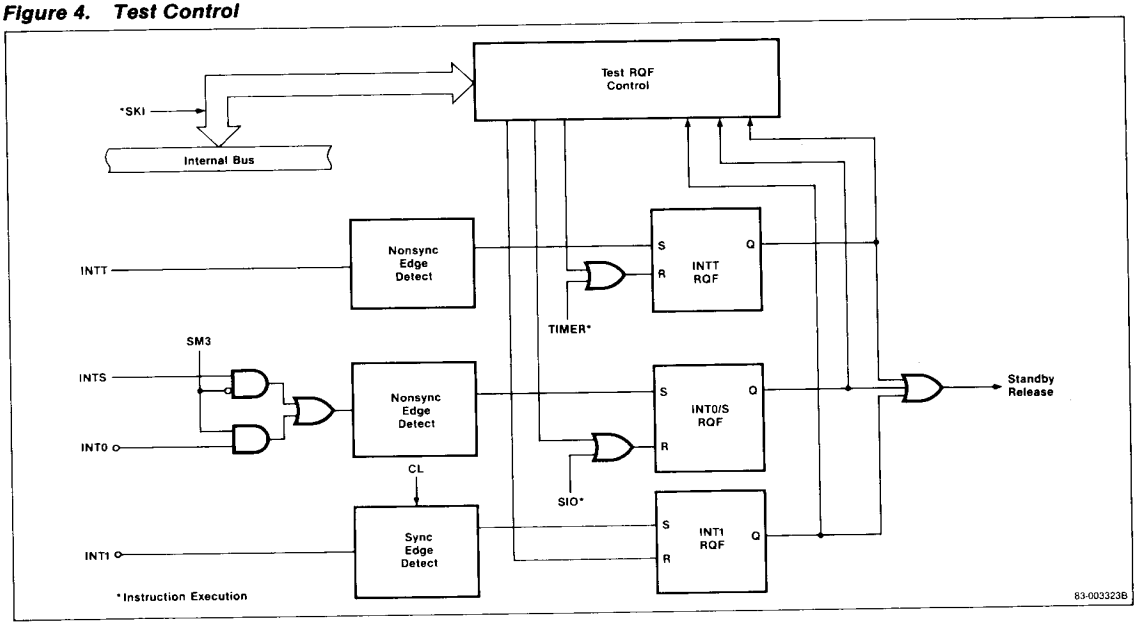


Figure 5. Serial Interface

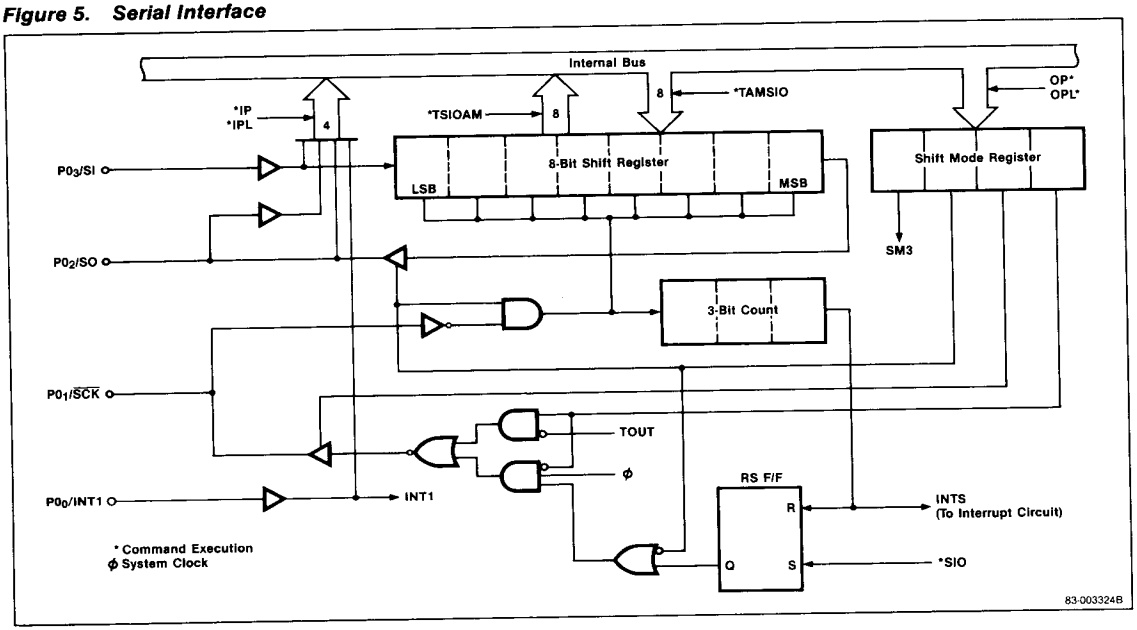
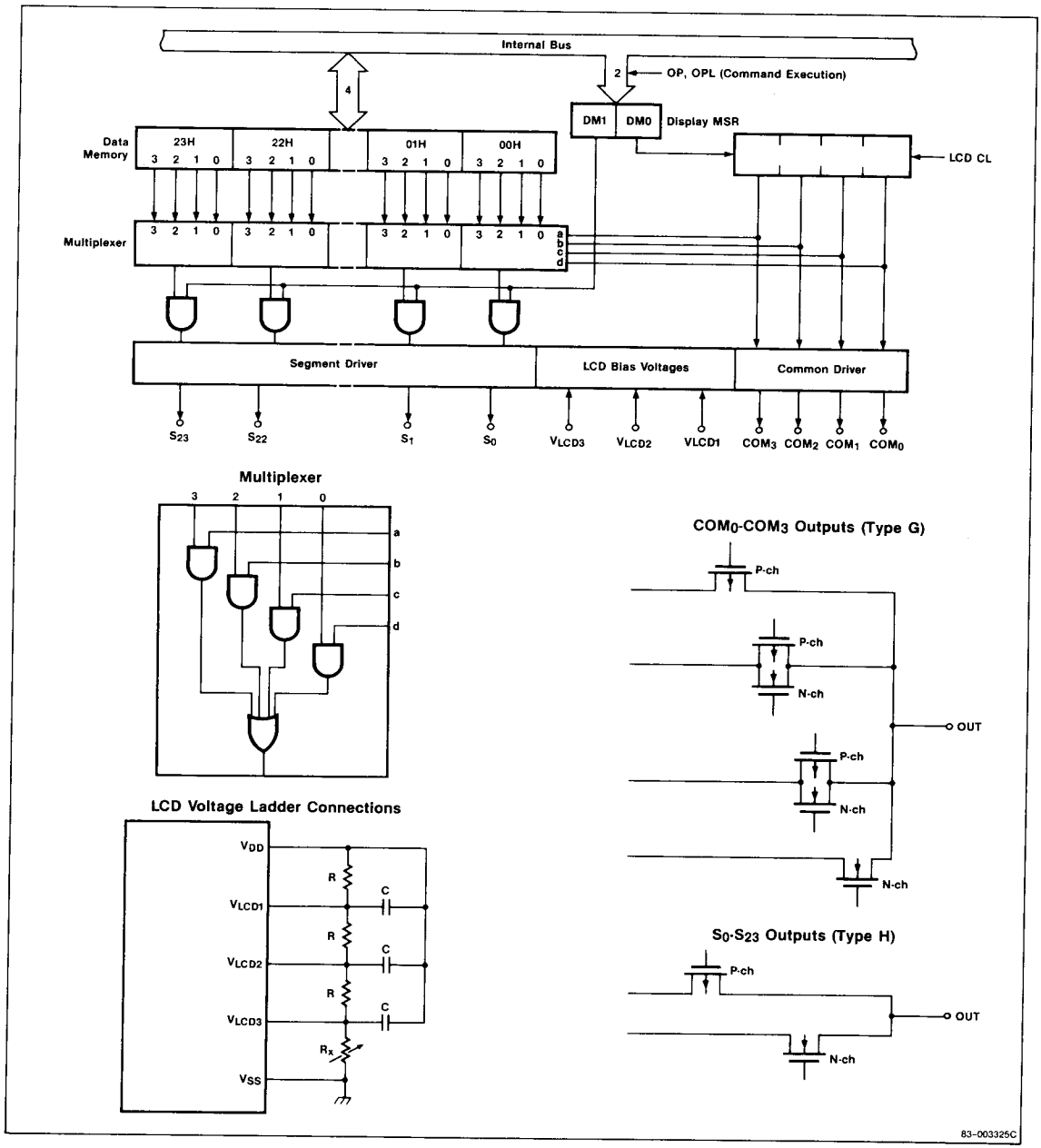


Figure 6. LCD Controller/Driver



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DC Characteristics

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA; V_{DD} = 4.5 to 6.0 V
		V_{DD} − 0.5			V	I_{OL} = −100 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA; V_{DD} = 4.5 to 6.0 V
				0.5	V	I_{OL} = 400 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 0 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Output impedance (Note 1)	R_{COM}		3	5	kΩ	COM_0-COM_3; V_{DD} = 4.5 to 6.0 V
			5	15	kΩ	COM_0-COM_3
	R_S		15	20	kΩ	S_0-S_{23}; V_{DD} = 4.5 to 6.0 V
			20	60	kΩ	S_0-S_{23}
Supply voltage	V_{DDDR}	2.0		6.0	V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
			70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1.0	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

Note:

(1) V_{LCD} = 2.7 V to V_{DD}
$V_{LCD1} = V_{DD} - (1/3)\ V_{LCD}$
$V_{LCD2} = V_{DD} - (2/3)\ V_{LCD}$
$V_{LCD3} = V_{DD} - V_{LCD}$

DC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −80 μA
Output voltage, low	V_{OL}			0.5	V	I_{OL} = 350 μA
Output leakage current, high	I_{LOH}			3	μA	V_O = V_{DD}
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	250	μA	Normal operation, V_{DD} = 3 V ±10%; R = 240 kΩ ±2%, C = 33 pF ±5%
			35	230	μA	Normal operation, V_{DD} = 2.5 V; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
			0.2	10	μA	Stop mode, X1 = 0 V; V_{DD} = 2.5 V
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

Absolute Maximum Ratings

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 V to V_{DD} + 0.3 V
Output current high, I_{OH}	
Per pin	−17 mA
Total, output ports	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, output ports	55 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, V_{DD} = 0 V

Parameter	Symbol	Limits Typ	Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

AC Characteristics

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 160 kΩ ±2% (Note 1)
		75		135	kHz	R = 160 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as input
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		16.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	$\overline{SCK}$ as input
		2.2			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_\phi$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leqq$ 60 ppm.

AC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	V_{DD} = 5 V ±10%; R = 240 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.25			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_\phi$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

Recommended R and C Values for System Clock Oscillation Circuit

T_A = −10 to +70°C

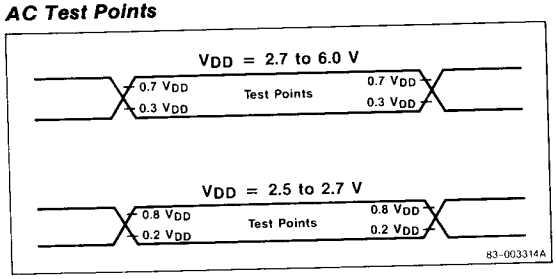
Supply Voltage Range	Recommended Values (Note 1)	Frequency Range
4.5 to 6.0 V	R = 82 kΩ ±2%	150 to 240 kHz, 200 kHz typical
2.7 to 3.3 V	R = 160 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R = 160 kΩ ± 2%	75 to 135 kHz
2.5 to 3.3 V	R = 240 kΩ ±2%	50 to 80 kHz
2.5 V	R = 240 kΩ ±2 %	50 to 77 kHz

Note:

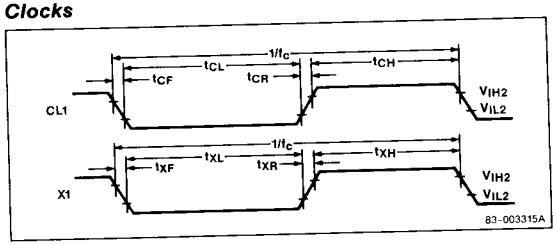
(1) C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

Timing Waveforms

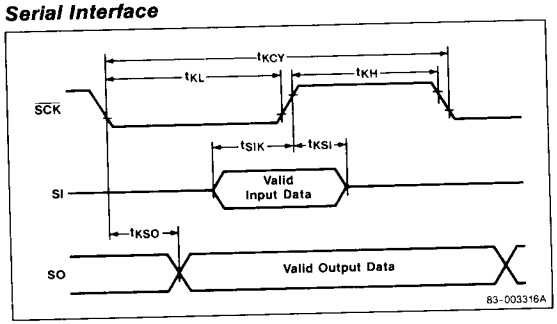
AC Test Points



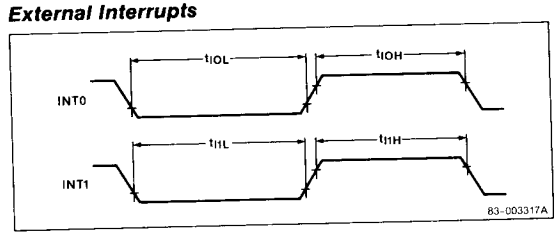
Clocks



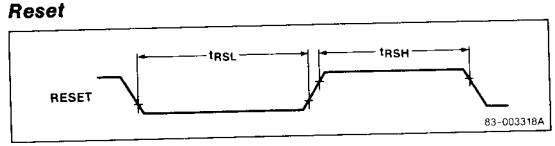
Serial Interface



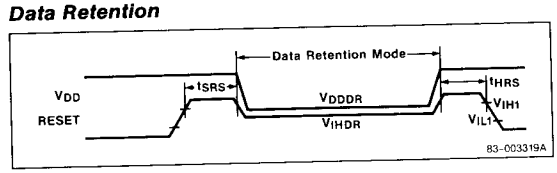
External Interrupts



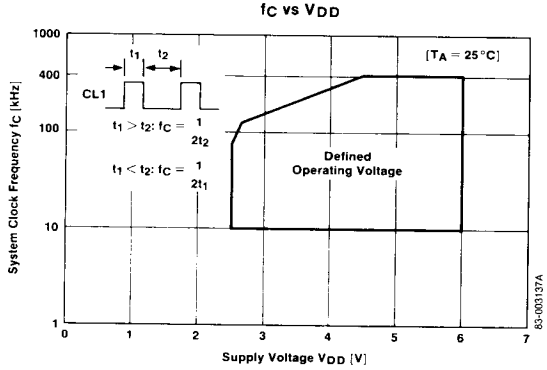
Reset

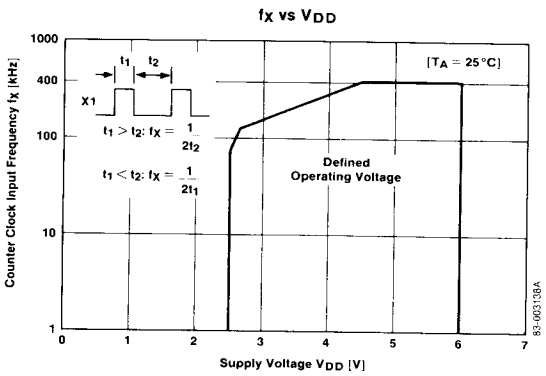


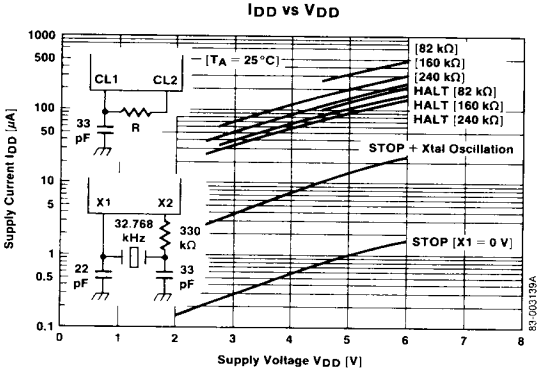
Data Retention

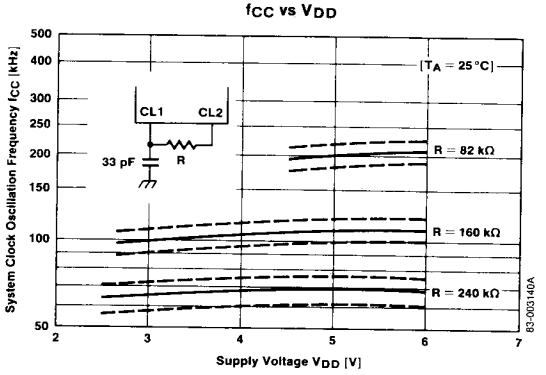


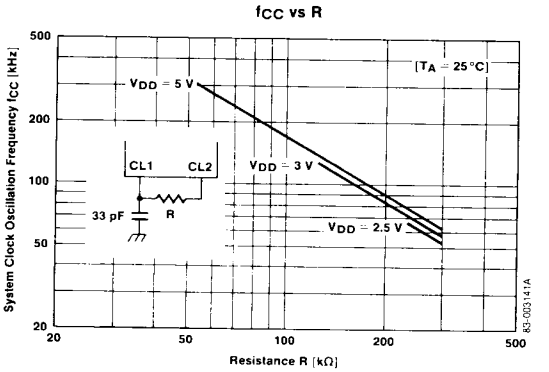
Operating Characteristics

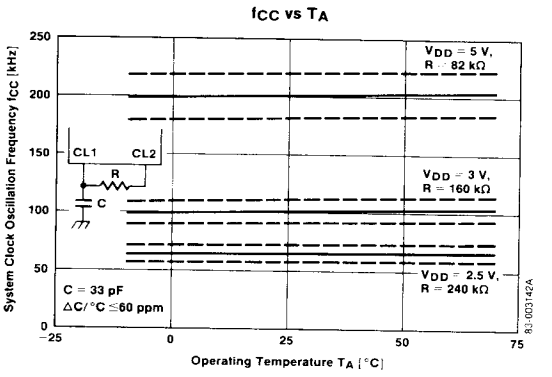






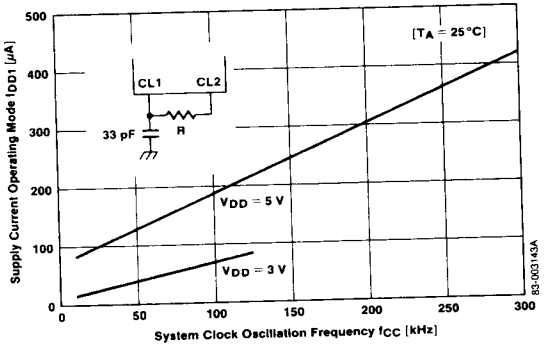




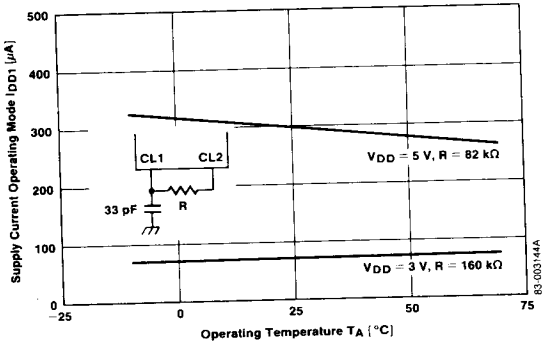


Operating Characteristics (cont)

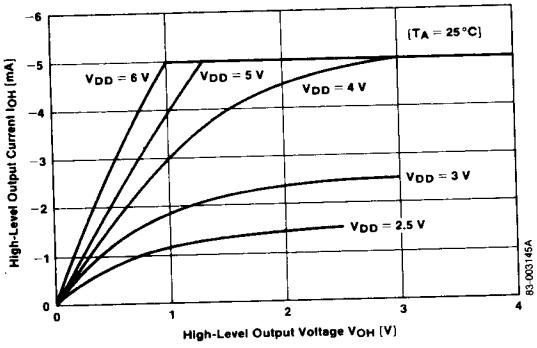
I_{DD1} vs f_{CC}



I_{DD1} vs T_A



I_{OH} vs V_{OH}



I_{OL} vs V_{OL}