PLESSEY
Semiconductors

T-50-09

NJ8820, NJ8820B

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820/NJ8820B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8820 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of -30°C to +70°C. The NJ8820B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

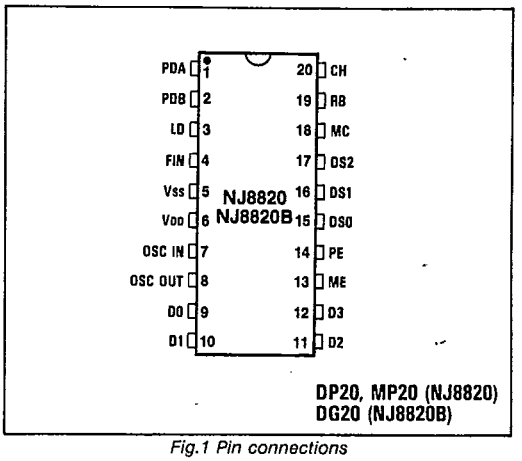


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

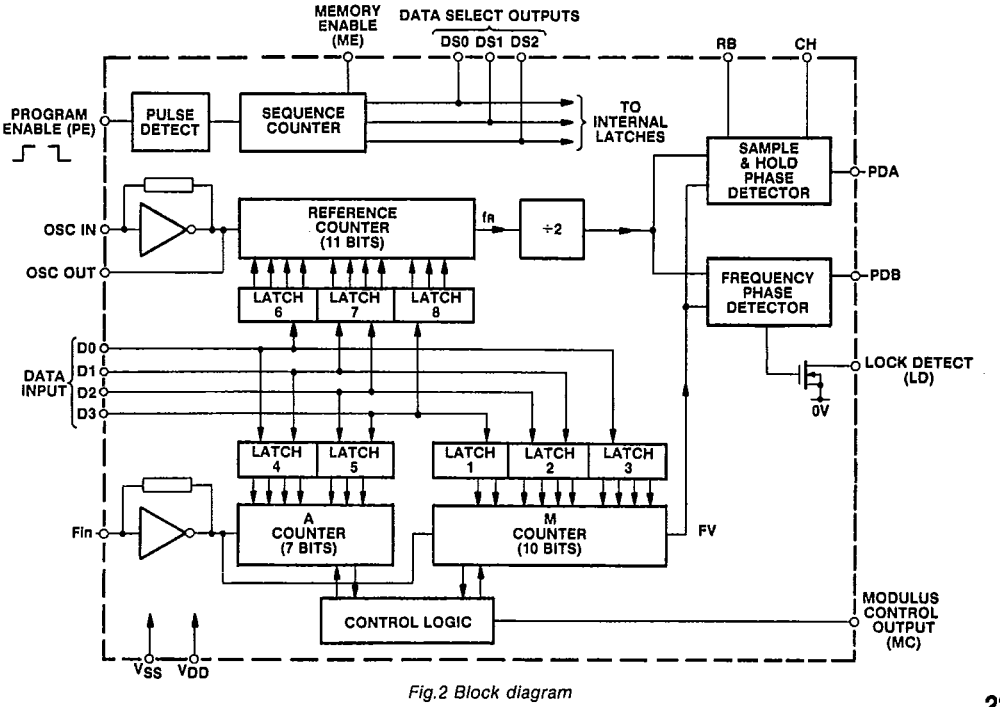


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-Vss 5V ± 0.5V, Temperature range NJ8820: -30°C to +70°C, NJ8820B: -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz }
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-Vss Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_W	5			μs	Pulse to Vss or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs. 2. All counters have outputs directly synchronous with their respective clock rising edges. 3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds. 4. To ensure correct operation of power-on programming. 5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

T-50-09

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
13	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15,16,17	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M $\geqslant$A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/Ps (pins 3 and 13)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C (DG package, NJ8820B)
Storage temperature	-55°C to +125°C (DP and MP packages, NJ8820)

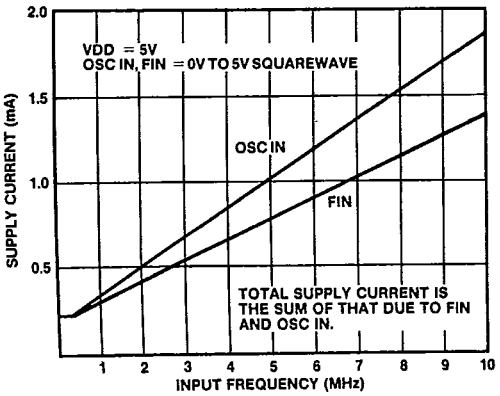


Fig.3 Typical supply current versus input frequency

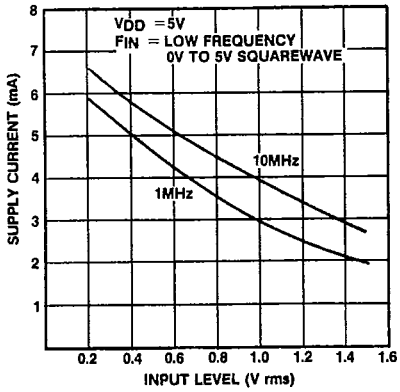


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Program information can be obtained from an external ROM or PROM under control of the NJ8820/NJ8820B. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability as shown in Fig.5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram appears as Figs. 6 to 8. Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

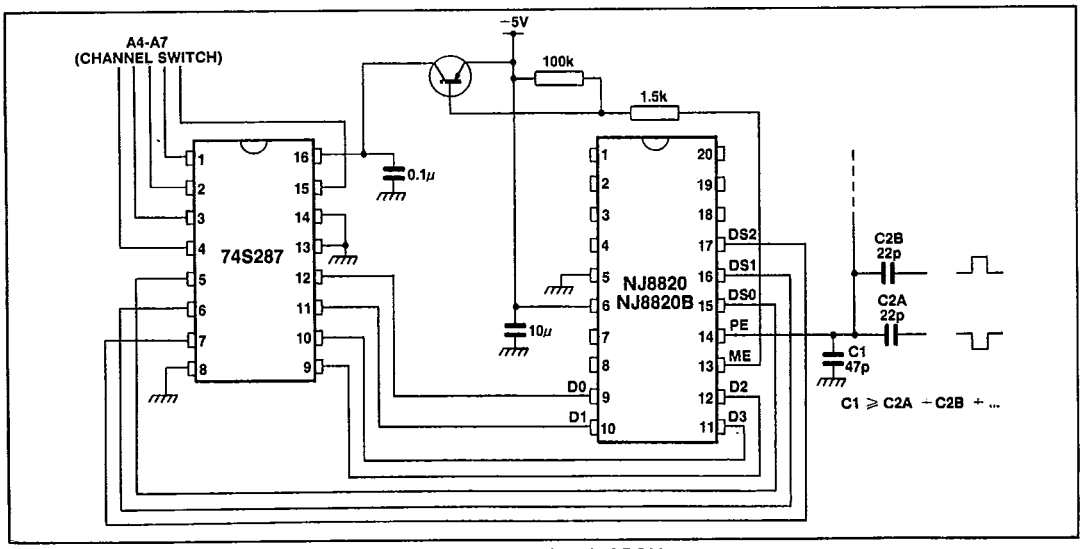


Fig.5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.6 Data map

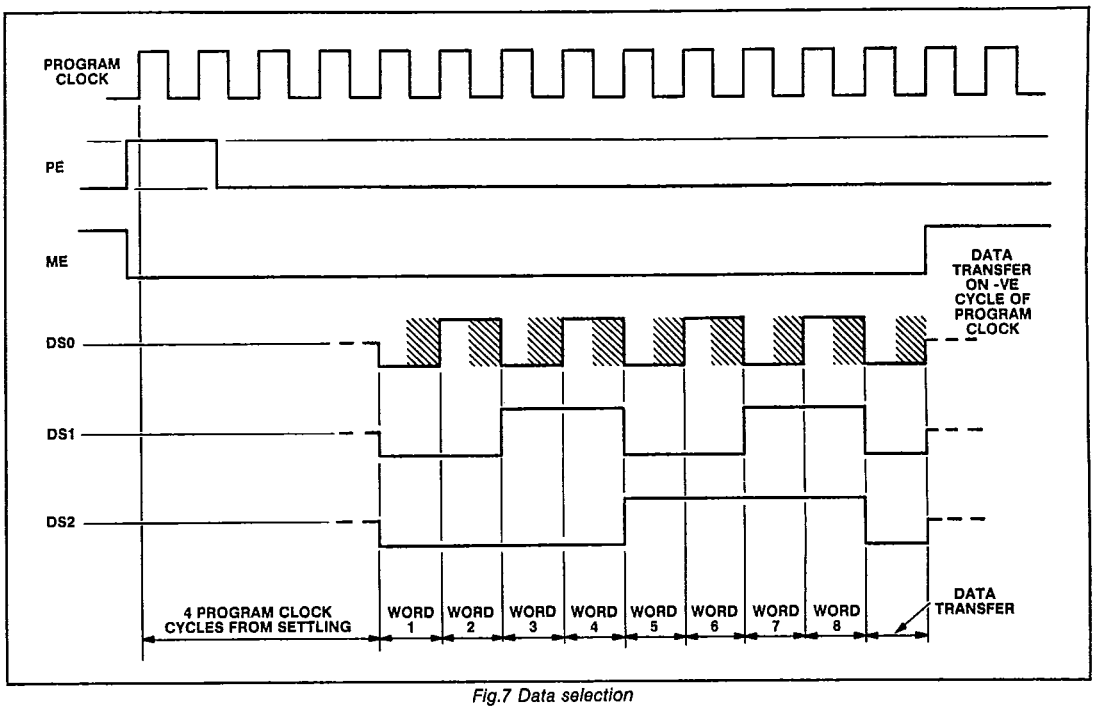


Fig.7 Data selection

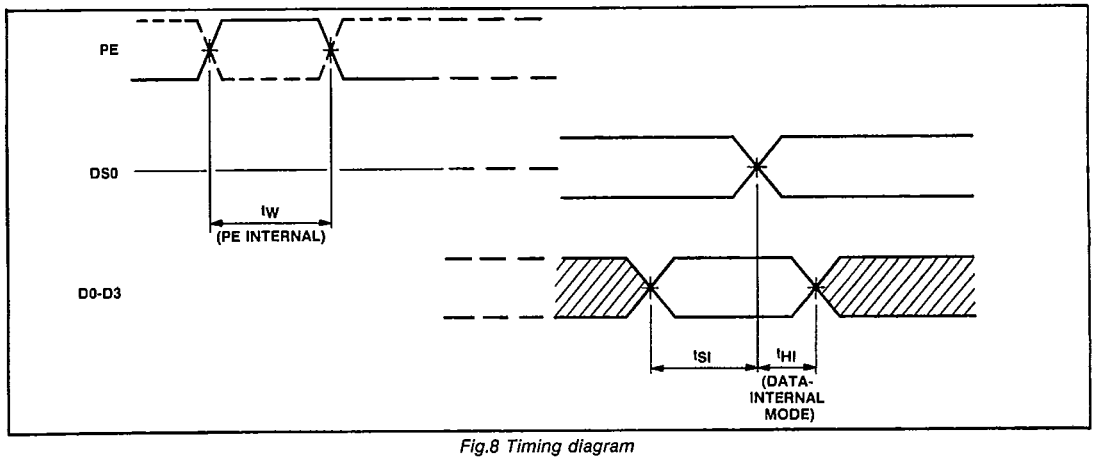


Fig.8 Timing diagram

PHASE COMPARATORS

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

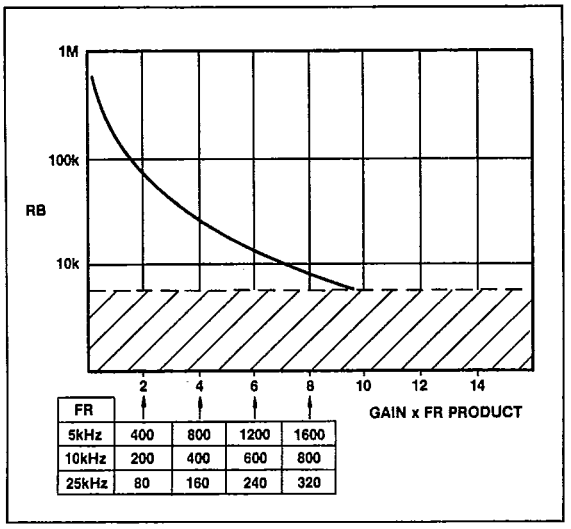
An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of gain frequency product by the desired frequency.

The output from these phase detectors should be combined and filtered to generate a single control voltage to drive the VCO as in Fig.8.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

APPLICATION EXAMPLE

An application example for a synthesiser for operation up to 520MHz is given in Fig.10. This gives up to 32 channels with a maximum supply current of 17mA, (typically 12mA) at 520MHz excluding the VCO. With careful construction the circuit is capable of providing sideband attenuation in excess of 90dB with lock-times of only a few milliseconds for a 1MHz frequency step.

T-50-09

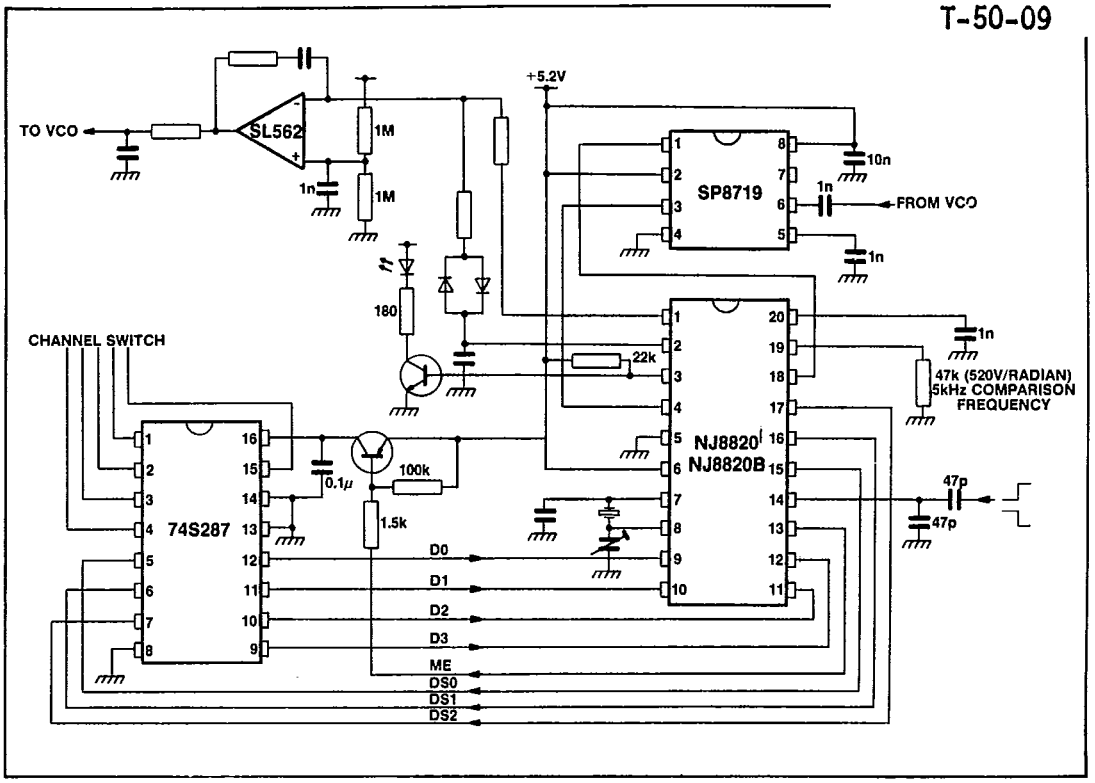


Fig.10 Application example