OPEN FIBER CONTROL S2036

FEATURES

- Implements redundant safety interlock for laser-based fiber optic systems
- Functionally compliant with ANSI XT311 Fibre Channel physical standard
- Enables Class 1 safety compliance for FDA, ANSI, and IEC guidelines
- Operates with the AMCC S2042/S2043, and S2044/S2045 Fibre Channel Chipsets at 265.625, 531.25, and 1062.5 Mbit/s
- On-chip ring oscillator
- Ultra low power operation
- 28-pin SOIC package
- PECL Interface

APPLICATIONS

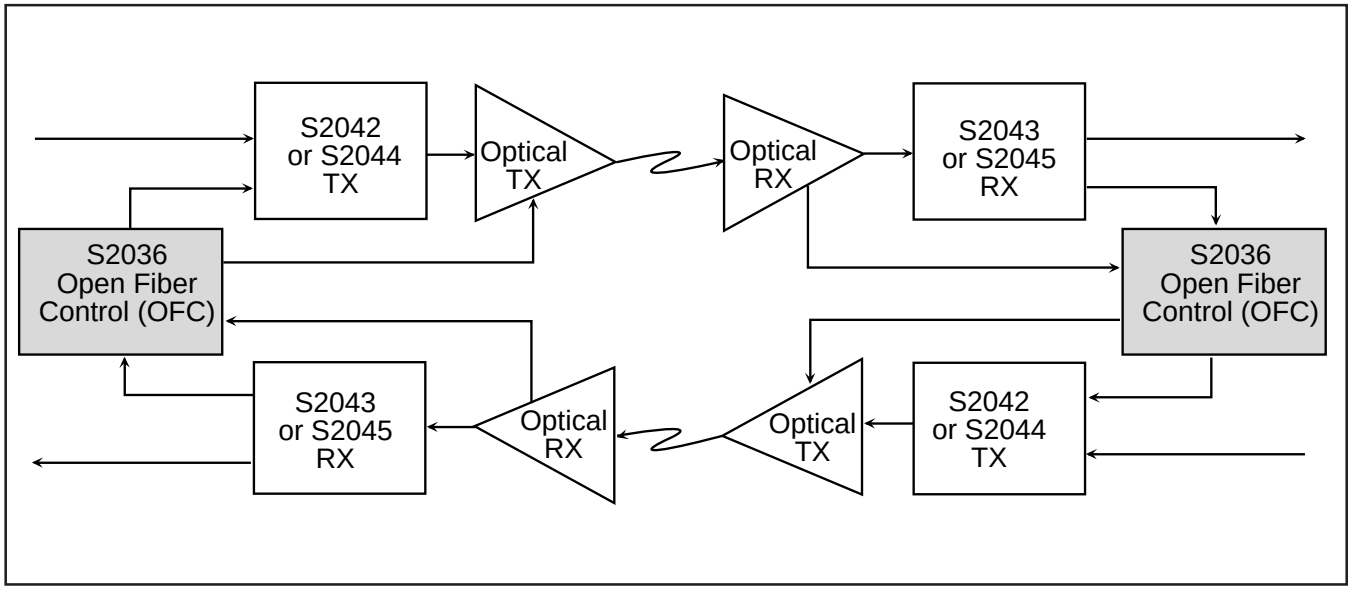
- Laser-based fiber optic systems
- Medical and laboratory instrumentation
- High-speed data and telecommunications
  - Supercomputer
  - Mainframe
  - Broadcast
  - Environments
  - Frame buffer
  - Switched networks
  - Mass storage/RAID
  - Workstation

GENERAL DESCRIPTION

The S2036 is designed specifically to implement the Fibre Channel Open Fiber Control (OFC) system, a redundant safety interlock feature for laser-based fiber optic systems. It is functionally compliant with the ANSI XT311 Fibre Channel physical standard and implements the OFC system defined by that standard, to detect when the optical link has been disrupted and shut down the laser or reduce the optical power level. The S2036 employs effectively redundant paths, each of which can independently turn off the laser.

The chip meets the requirements of Class 1 safety limits defined by FDA, ANSI, and IEC. It is fully compatible with AMCC's S2042/S2043 and S2044/S2045 Fibre Channel chipsets at 265.625, 531.25, and 1062.5 Mbit/s operation. It features low-power operation and a 28-pin SOIC package. Figure 1 shows the S2036 used in a typical network configuration.

Figure 1. System Block Diagram



OVERVIEW

The OFC system is an open fiber link detection and laser control system specified in ANSI XT311 Fibre Channel physical standard. It is used as a safety interlock for point-to-point optical fiber links that use semiconductor laser diodes as the optical source. The major reason for implementing OFC is that the optical power levels required to obtain the desired level of system performance in Fibre Channel exceeds the Class 1 limits defined by national and international laser safety standards, if the optical fiber link between two optical ports is disconnected, such as would occur with an opened connector or a cut fiber. It is extremely important that requirements for Class 1 classification are met, due to the potential for customer exposure to laser radiation.

Since it is only when an optical link is opened that a user can be exposed to laser radiation, implementing OFC allows Class 1 classification requirements to be met, since it can detect when the link has been disrupted and can shut down the laser or reduce the optical power level. The S2036 complies fully with the OFC specifications and Class 1 requirements.

Refer to the ANSI Fibre Channel standard document for details of OFC operation.

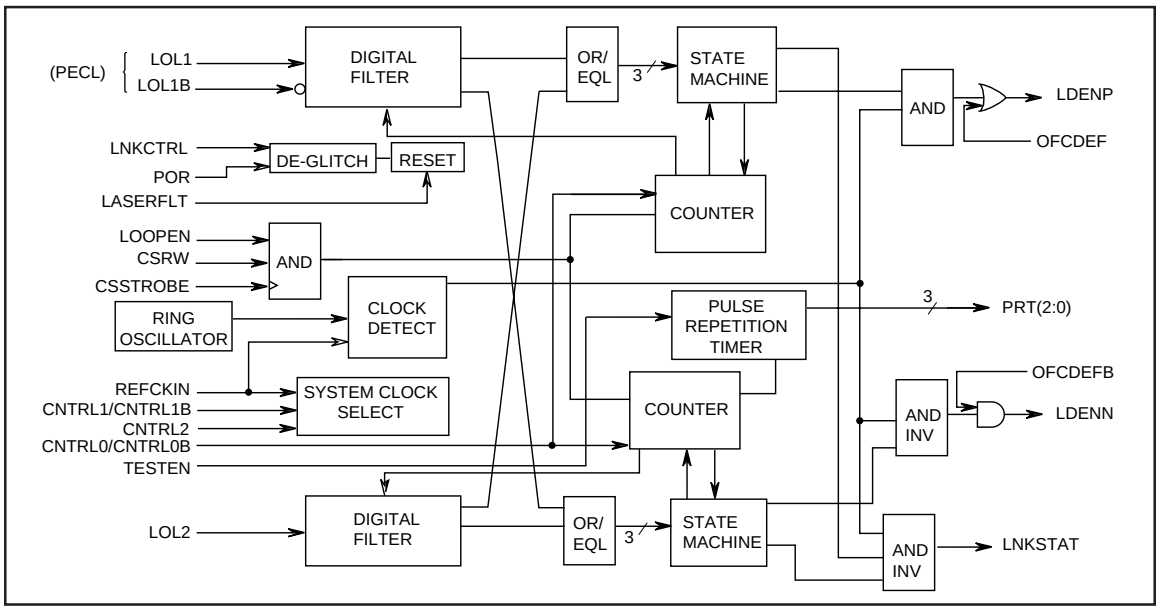
CIRCUIT OPERATION

Whenever the fiber data link is disrupted (by a cut fiber or a disconnected connector), the S2036 detects the disruption and forces the transceiver into a repetitive pulsing mode of operation with a very low duty cycle. The link returns to normal operation only when the device detects that the disruption has been repaired and the proper reconnection handshake has taken place between the two transceivers in the link.

As seen in the module block diagram in Figure 2, two loss-of-light control paths are provided and both must be satisfied before the laser can be activated. Each path has a separate digital filter, state machine, and a counter. Two loss-of-light detectors each feed a digital filter. The output of each filter is “OR/EQUALed” to produce an interval Loss-of-Light (LOL) signal. If the REFCKIN is too fast or too slow, the clock detector causes the laser to be deactivated. Two laser driver control outputs are independently capable of disabling the laser drive circuitry. They are of opposite polarity to prevent voltage control problems from accidentally activating the laser. The link status output signals the user system when the link is inactive.

A power-on-reset signal is used to synchronize the counters and state machines. Three user system control lines, Laser Fault, Link Control and Loopback Enable, force the S2036 to disable the laser drive circuitry and turn off the laser.

Figure 2. Functional Block Diagram



The two state machines are independent and identical, and contain the logic to detect when the optical link becomes open due to a disconnection or break. They also preside over the link reconnection handshake when it detects that the link is reconnected.

OFC Time Periods

The OFC system uses a repetitive pulsing technique (i.e., laser activated for t microseconds every T seconds) during the time that a link is open in order to reduce the maximum possible exposure to a value which allows for classification as a Class 1 laser product. The maximum average power level per pulse is a function of the wavelength, pulse duration (t), and pulse repetition frequency (PRF = 1/T).

To function correctly, each short-wavelength optical link port must contain a transmitter/receiver unit that has implemented the OFC system with compatible OFC interface timings. The timing values that are consistent with the stated maximum transmitter receptacle power and current (1990) IEC laser safety restrictions for a Class 1 system are shown in Table 1.

These time periods, when used according to the OFC interface specification described in this section, should result in a laser product which conforms to current (1990) emission requirements for Class 1 classification worldwide. Note, however, that classification of a laser product must always be verified with measurements and calculations and not assumed.

The connection and disconnection handshake timing is shown in Figures 5 and 6. The connection handshake is performed at link initialization or at the automatic recovery from intentional or accidental interruption of the optical path. The Pulse duration, t, is chosen to meet the maximum average power level while allowing for the propagation delay through both fibers and the light detection and laser turn-on delay of the complete transceiver system. This margin is shown as t_{setH}. Similarly, the Stop time t_S is set at either 2t or 4t to assure that the detected pulse originates from a properly functioning OFC node. This is accomplished by the detection of loss of light for a time t_{setL} prior to the end of the Stop time. In Figure 5, the Master node is the one whose 10.1 second timer expires first after the reconnection is complete.

Figure 6 illustrates the reaction of the system to the disruption of one fiber (the one between the Master transmitter and the Slave receiver). Since the other fiber is still intact in this example, the Master transmitter is shown as again having its 10.1 second timer expire first, but then resynchronizing to the received pulse from the Slave transmitter.

Safety Documentation/Usage Restrictions

Shortwave laser transceiver products incorporating the OFC system in order to assure Class 1 compliance shall include the following two usage restrictions as part of the product's user, maintenance, and safety documentation:

Table 1. Selectable OFC Time Periods

Symbol	Description	25 Mbyte/s	50/100 Mbyte/s	Units
CNTRL0/0B	Counter Control 0	Low	High	—
t	Pulse duration time	617	154	µsec
T	Pulse repetition time	10.1	10.1	sec
t_S	Stop time	1234	617	µsec
t_{LDENon}	LOL1 & LOL2 inactive to LDENP/N	2–4	2–4	µsec
$t_{LDENoff}$	LOL1 or LOL2 active to LDENP/N	20–40	20–40	µsec
t_{ldon}	Laser turn–on time	LDENon + Laser activation time		—
t_{ldoff}	Laser turn–off time	LDENoff + Laser deactivation time		—
t_{pdf1}	Propagation delay, fiber 1			—
t_{pdf2}	Propagation delay, fiber 2			—

a)The laser product shall be used in point-to-point optical links only. The OFC safety system is incompatible with other types of link connections (i.e., multiple input or output links). Failure to comply with this usage restriction may result in incorrect operation of the link and points of access that may emit laser radiation above the limit for Safety Class 1 systems established by one or more national or international laser safety standards.

b)Normal operation of the point-to-point optical link requires that the laser product shall be connected only to another Fibre Channel compatible laser product that includes the OFC safety system. In addition, each of these products must be certified as Safety Class 1 laser products according to the laser safety regulations and/or standards in existence at the time of manufacture.

The certification ensures that each of the products will function correctly in the event of a fault in one of the safety control systems.

It is the responsibility of the interface designer tassure that the redundancy and freedom from single point failure sensitivity incorporated in the Fibre Channel standard and the design of the S2036 are fully implemented in the final laser product. These implementation criteria shall include but are not limited to:

a)Biasing of the LDENP/N signal lines with 10KΩ resistors external to the S2036 assures that the non-operating state of the laser is forced if the S2036 is removed or destroyed while the system is operating.

b)Use of the redundant control signals (CNTRL0B and CNTRL1B) to assure safe operation or no operation in the event of a single point failure of any control signal.

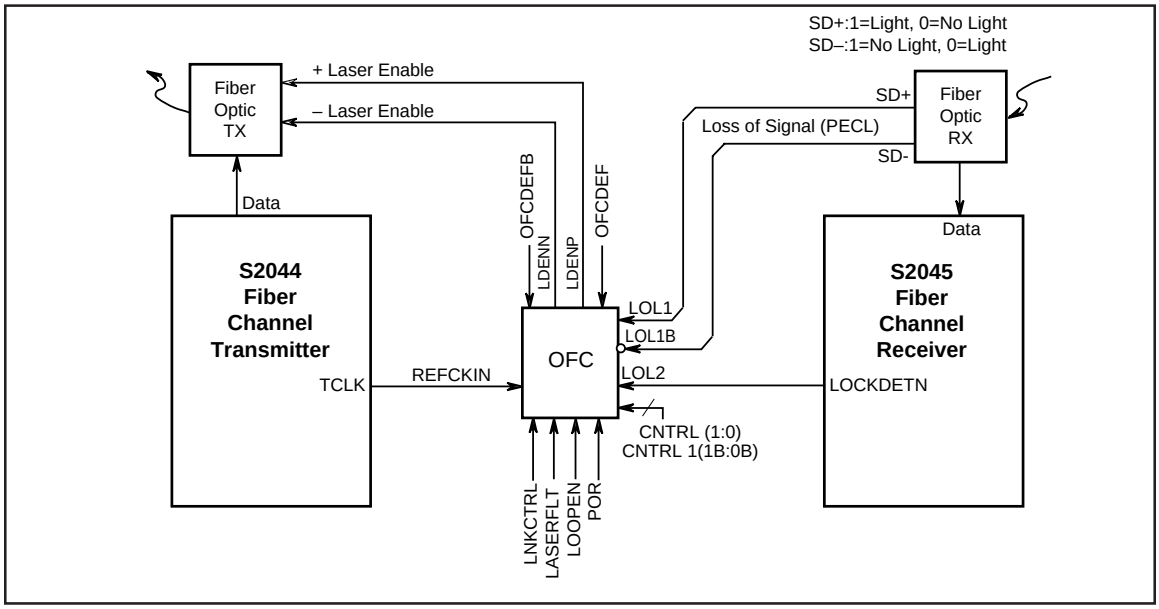
WARNING! IMPORTANT!

The S2036 is equipped with an overrride function to permit activation of the attached laser during module level testing. This function is operable with the TESTEN held in the active high state and OFCDEF held High and OFCDEFB held Low only. It is the responsibility of the manufacturer to isolate these inputs from accidental activation by the end user. Failure to do so may void the certification of the module or the OEM system for Laser Safety Class 1 operation.

Digital Filter

The digital filters integrate the incoming signals to improve their reliability. The filters sample at a faster rate when acquiring a light-present signal and at a slower rate when dropping a light-present signal, while maintaining the correct handshake timing.

Figure 3. OFC Connections



State Machine

The state machine is implemented per the Fibre Channel FC-PH document, Paragraph 6.2.3 and annex I. The OFC time periods are user-selectable to comply with the operating frequency of the serial link. The selectable OFC time periods are seen in Table 1. The pulse repetition time is fixed for both 25, 50, and 100 Mbyte applications to 10.1 seconds.

The inputs to the state machine are the loss of light indicators (DC and AC) and the power-on reset. The timing of the state machine transitions is controlled by the decode times. The timing of the laser control signals will not necessarily be synchronous to the system clock because of the long counter times involved.

Link Initialization

Following a power-on-reset cycle, the OFC device will be in the Stop State as defined in the Fibre Channel Standard. The default state for the internal loopback control is loopback active. A Control/Status Write cycle is required together with a logic high on the LOOPEN input in order to place the OFC in the Reconnect State allowing the repetitive pulsed output operation. The required timing for this write cycle is shown in Figure 5.

Reference Clock Select

The reference clock is user-selectable to be 53 MHz or 26 MHz. The reference clock input is divided by four if a 53-MHz clock is used, or by two for a 26-MHz clock so that all state machine and counter clocks operate at 13 MHz. Refer to Figure 3 and Figures 7 through 10 for suggested connections.

Clock Detect

The clock detect circuitry compares the reference clock input and the ring oscillator. If the ring oscillator and the reference clock frequencies do not compare as selected by CTRL2, CTRL1/1B, and CTRL0/0B, the laser is disabled to prevent it from staying on or increasing the laser duty cycle.

De-Glitch Logic

The de-glitch logic debounces the power-on reset and the link control pin to eliminate potential glitching of the laser control lines.

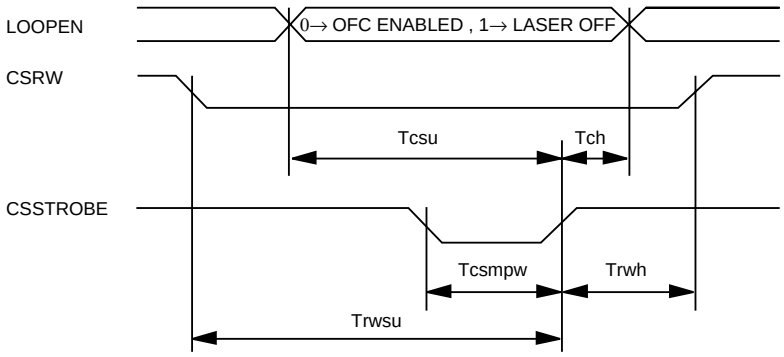
Counter

The two counter blocks are redundant functions which generate the selected decode timing used by the state machines. (See Table 1 for OFC time periods.) One of the counters is used as the lower part of the 10.1 sec pulse repetition timer.

Pulse Repetition Timer

The pulse repetition timer generates the 10.1 sec decode timer used by the state machines. In test mode it is broken up into three counter stages which is output on the PRT<0> pin.

Figure 4. Loopback Enable Write Access



Symbol	Description	Min	Max	Units
Trwsu	CSRW setup time before CSSTROBE rising edge	5		ns
Trwh	CSRW hold time after CSSTROBE rising edge	5		ns
Tcsu	LOOPEN setup time before CSSTROBE rising edge	5		ns
Tch	LOOPEN hold time after CSSTROBE rising edge	5		ns
Tcsmpw	CSSTROBE minimum pulse width	15		ns

Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
POR	TTL	I	4	Active low power-on reset signal, which is sampled by the deglitching circuitry.
CSRW	TTL	I	6	Control/status read/write input. Must be low to enable the clocking of the Loopback Enable signal.
REFCLKIN	TTL	I	2	53-MHz or 26-MHz clock used as the master clock for the state machine and the counters. This clock is monitored by the ring oscillator for correct frequency. This pin should be tied to TCLK of the S2044.
CNTRL0	TTL	I	23	Counter control 0. Controls the counter values that determine the decode time periods. It should be set to low for 617 µs laser pulses and high for 154 µs laser pulses. (See Table 1.) It is also used during device testing to verify the ring oscillator circuitry.
CNTRL0B	TTL	I	10	Counter control 0B. A backup for CNTRL0. Should be independently driven to the same logic state. The full use of this pin prevents the unwanted generation of a 617-µs pulse due to a single-point failure of CNTRL0 to logic low. A false low on CNTRL0 or a false high on CNTRL0B will result in a reset of the S2036 and selects the ring oscillator to TESTOUT when TESTEN is low. A false high on CNTRL0 will result in 154 µs pulses.
CNTRL1	TTL	I	22	Counter control 1. This pin, together with the CNTRL2 pin, selects the reference clock frequency. If the reference clock is 53 MHz, this pin must be high, and CNTRL2 must be low. if the reference clock is 26 MHz, this pin and CNTRL2 must both be low.
CNTRL1B	TTL	I	9	Counter control 1B. This pin is a backup for CNTRL1 and should be independently driven to the same logic state.
CNTRL2	TTL	I	25	Counter control 2. This pin is used with CNTRL1 to select the reference clock frequency and should be set to Low.
TESTCK	TTL	I	28	This clock input is used in test to replace the ring oscillator when OFCDEF and OFCDEFB are both High or Low.
LOL1 LOL1B	PECL	I	11 12	Loss of Light 1. Active low. When low, indicates that an optical signal is **not** present at the input to the fiber optic receiver. These pins must be tied to the Loss of Signal pin of the fiber optic receiver for a DC loss of signal function. (See Figure 3.)
LOL2	TTL	I	13	Loss of Light 2. Active high. When high, indicates that an optical signal is **not** present at the input to the fiber optic receiver. This pin must be tied to the S2044 LOCKDETN signal for an AC loss of signal function. (See Figure 3.)

Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
LOOPEN	TTL	I	8	Loopback enable, active High. When high, deactivates the laser diode enable pins (both LDENP and LDENN) regardless of the state of the state machine. It is enabled by the CSRW and clocked by the TCLK of the S2044/45 devices. Once the laser is turned off, only the OFC system can turn it back on by performing a link reconnection handshake.
LASERFLT	TTL	I	24	Laser fault signal, active High. When high, this pin will deactivate the laser diode enable pins (both LDENP and LDENN) regardless of the state of the state machine. Asserts LNKSTAT. Once the laser is turned off, only the OFC system can turn it back on by performing a link reconnection handshake.
LNKCTRL	TTL	I	3	Link control input, active High. When high, this pin will deactivate the laser diode enable pins (both LDENP and LDENN) regardless of the state of the state machine. It is deglitched to filter spurious transitions of the laser diode enabled signals. Once the laser is turned off, only the OFC system can turn it back on by performing a link reconnection handshake.
CSSTROBE	TTL	I	7	Control/Status strobe input, used to clock the Loopback Enable signal. It is intended to be tied to the TCLK pin of the S2044. The Loopback Enable signal is clocked on the rising edge of CSSTROBE.
TESTEN	TTL	I	14	Active high Test Enable input. Internal pull-down resistor attached. This pin forces the pulse repetition counter to be broken up into five individual counters for test purposes and disables the LDENN output and selects TESTCK to TESTOUT when OFCDEF and OFCDEFB are both High or Low.
OFCDEF	TTL	I	5	Positive laser diode enable forced input. Active High. Internal pull-down resistor attached. Overrides the OFC control of the positive laser diode enable and forces the laser to be enabled for test, when TESTEN is High.
OFCDEFB	TTL	I	26	Negative laser diode enable forced input. Active Low. Internal pull-up resistor attached. Overrides the OFC control of the negative laser diode enable and forces the laser to be enabled for test, when TESTEN is High.
LNKSTAT	TTL	O	21	Link status output. High = Link inactive. Indicates to the system when the link is inactive due to a loss of signal condition detected by the OFC system. Active during LOOPBACK mode. Asserted when LASERFLT signal is asserted.
TESTOUT	TTL	O	27	Test output signal. Outputs TESTCK input when TESTEN is high and OFCDEF and OFCDEFB are both high or low, or outputs ring oscillator divided by 4 when TESTEN is low and CNTRL0 is low and CNTRL0B is high. Otherwise, outputs high impedance.

Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
LDENP	TTL	O	16	Positive laser diode enable output, active High. Output of the state machine and should be tied to the positive enable pin of the laser diode transmitter. Each of the laser diode enable pins are independently capable of disabling the laser drive circuitry (via separate control paths). The enable pins are of opposite polarity to prevent voltage control problems from accidentally activating the laser.
LDENN	TTL	O	17	Negative laser diode enable output, active Low. Output of the state machine and should be tied to the negative enable pin of the laser diode transmitter. Each of the laser diode enable pins are independently capable of disabling the laser drive circuitry (via separate control paths). The enable pins are of opposite polarity to prevent voltage control problems from accidentally activating the laser.
PRT2 PRT1 PRT0	TTL	O	18 19 20	Pulse repetition time outputs. In normal operating mode, this bus monitors the output of the LOL2 and LOL1 digital filters (on PRT2 and PRT1, respectively). Logic high represents loss of light. PRT0 monitors the internal reset of the S2036. In TESTEN mode, PRT2 and PRT1 monitor the laser on output of state machines 2 and 1, while PRT0 monitors the end of the counter chain (REFCLK/4096 or REFCLK/9192).
VDD	+5V	–	1	Power supply (+5V)
GND	0V	–	15	Ground

Figure 5. OFC Transceiver Connection Handshake Timing

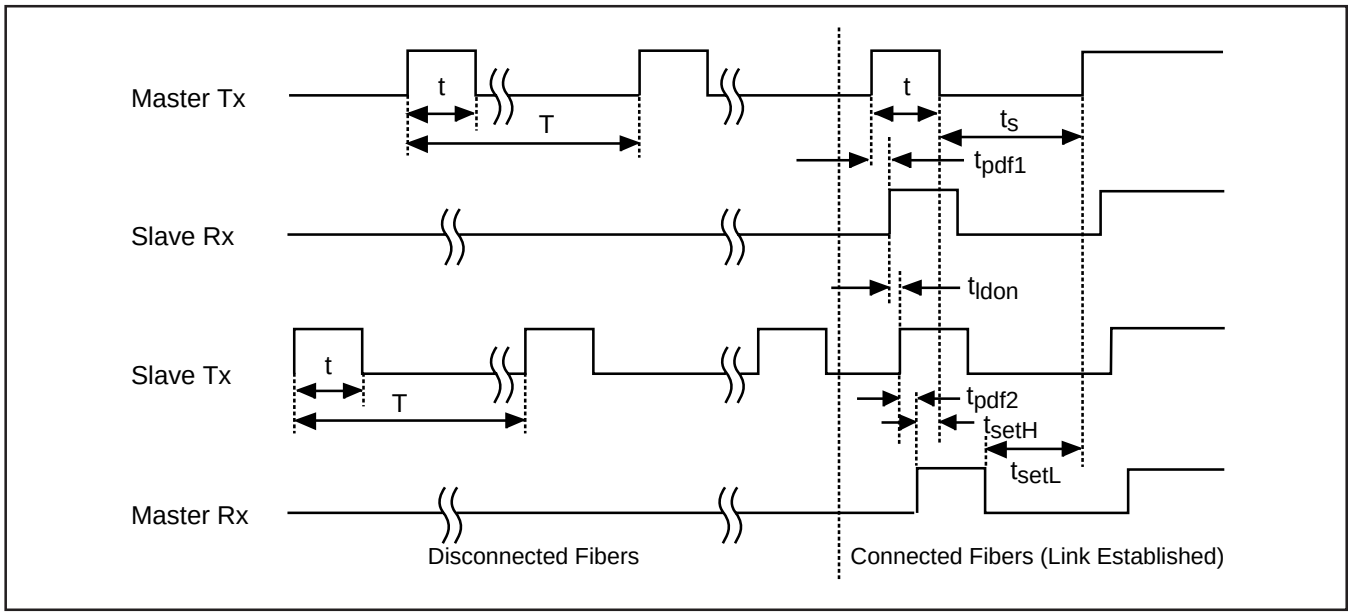


Figure 6. OFC Transceiver Disconnect Handshake Timing

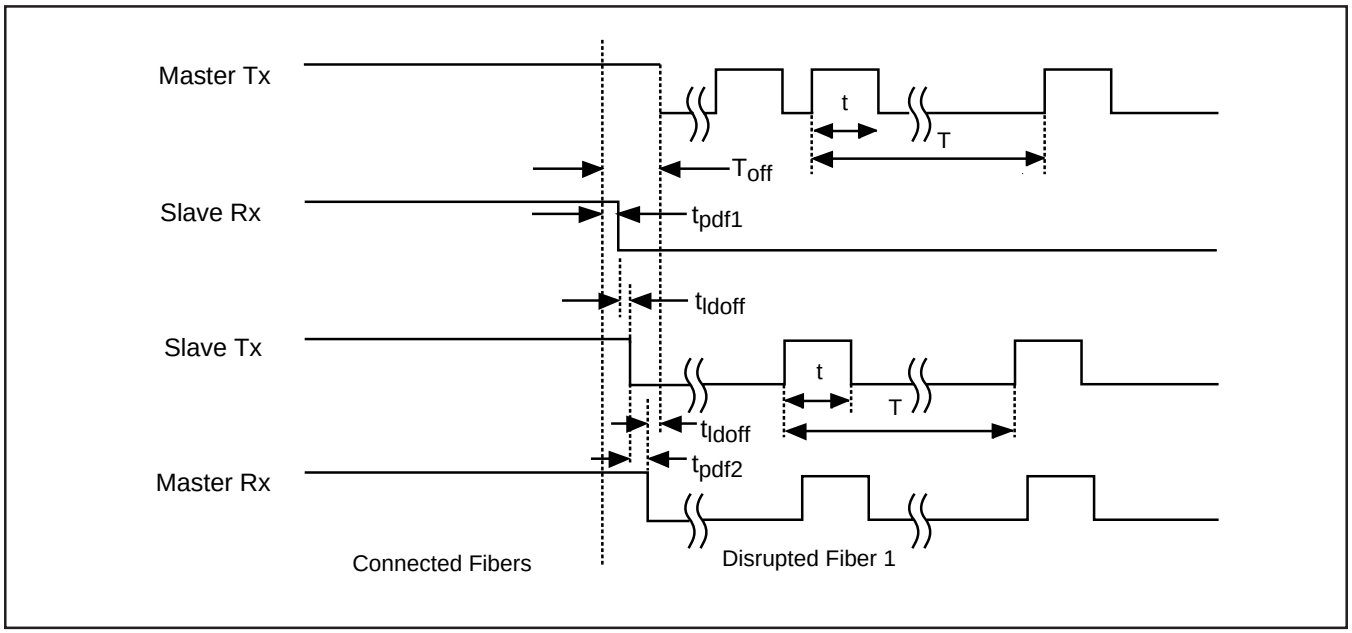
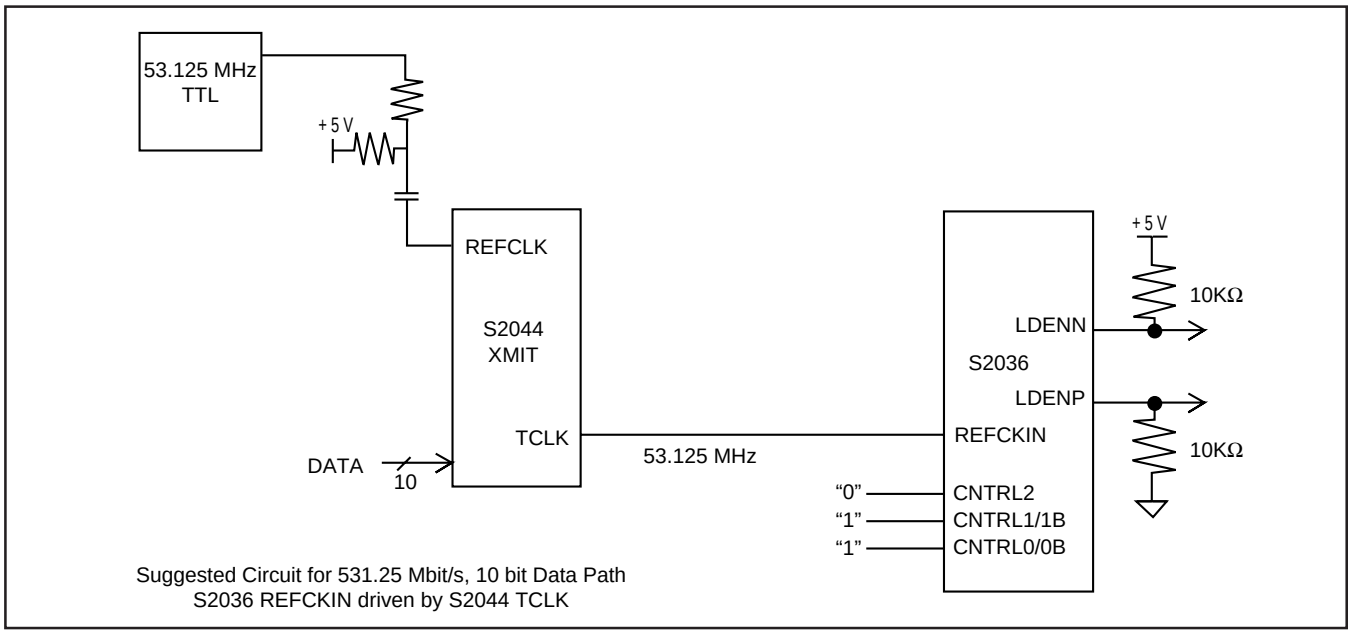


Figure 7. Suggested Circuit for 531.25 Mbit/s Operation with S2044 in 10-Bit Mode



APPLICATIONS SUGGESTIONS

REFCKIN Connection Options

The S2036 can be used with the S2044 or S2045 with only the addition of attenuating resistors for the reference clock source. Figure 7 shows the connection of the reference clock with the S2044 operating in the 10 bit mode at 531 Mbit/s data rate. The clock trace lengths should be minimized.

Figures 8–10 illustrate representative (but not exhaustive) combinations of CNTRL inputs and REFCLKIN drive sources.

Figure 8. Suggested Circuit for 1062.5 Mbit/s Operation with S2044 in 20-Bit Mode

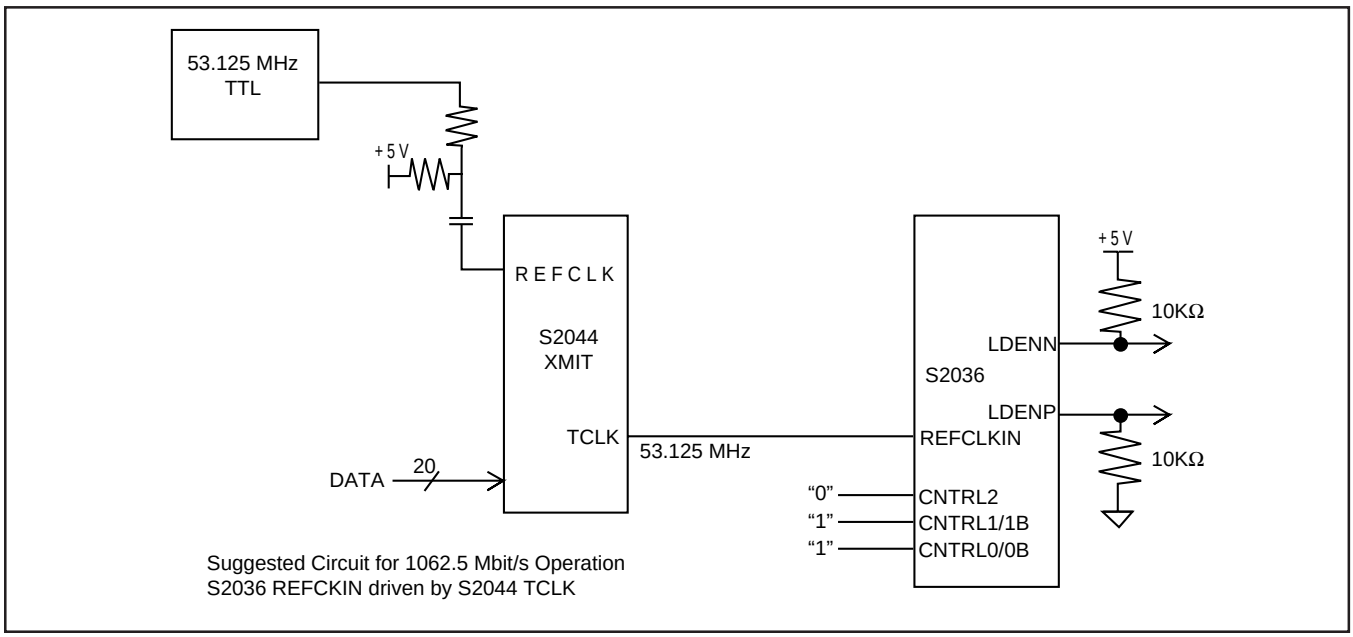


Figure 9. Suggested Circuit for 531.25 Mbit/s Operation with S2044 in 20-Bit Mode

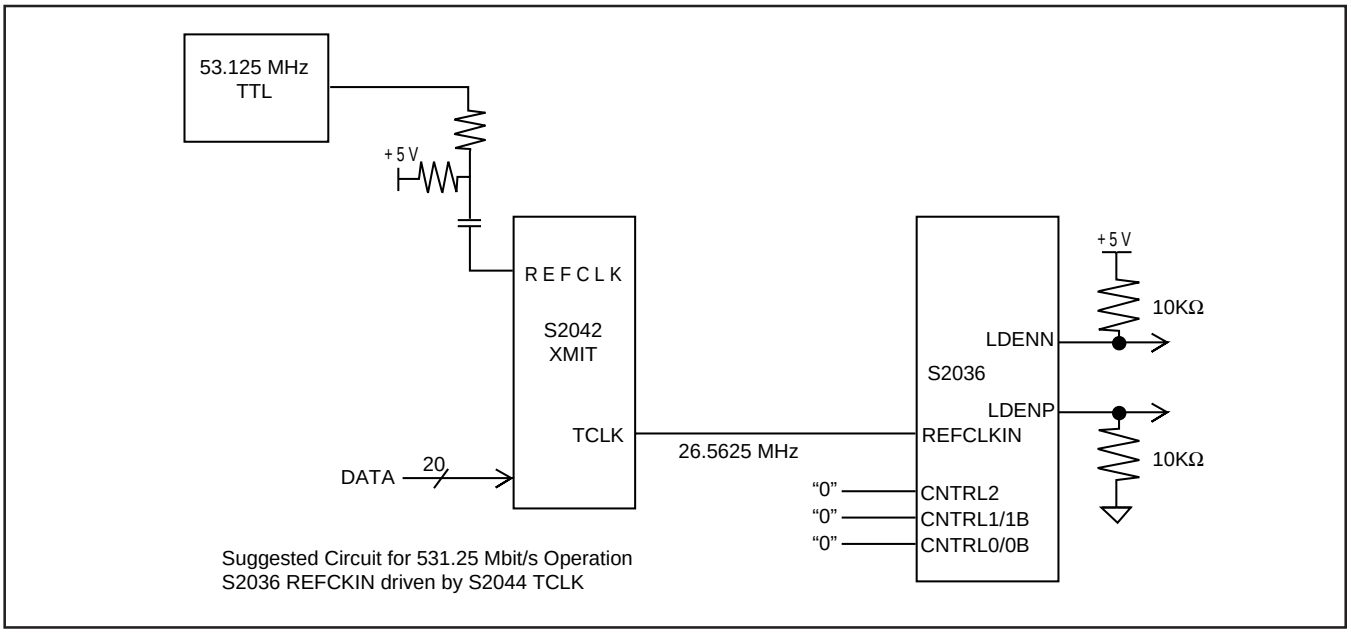
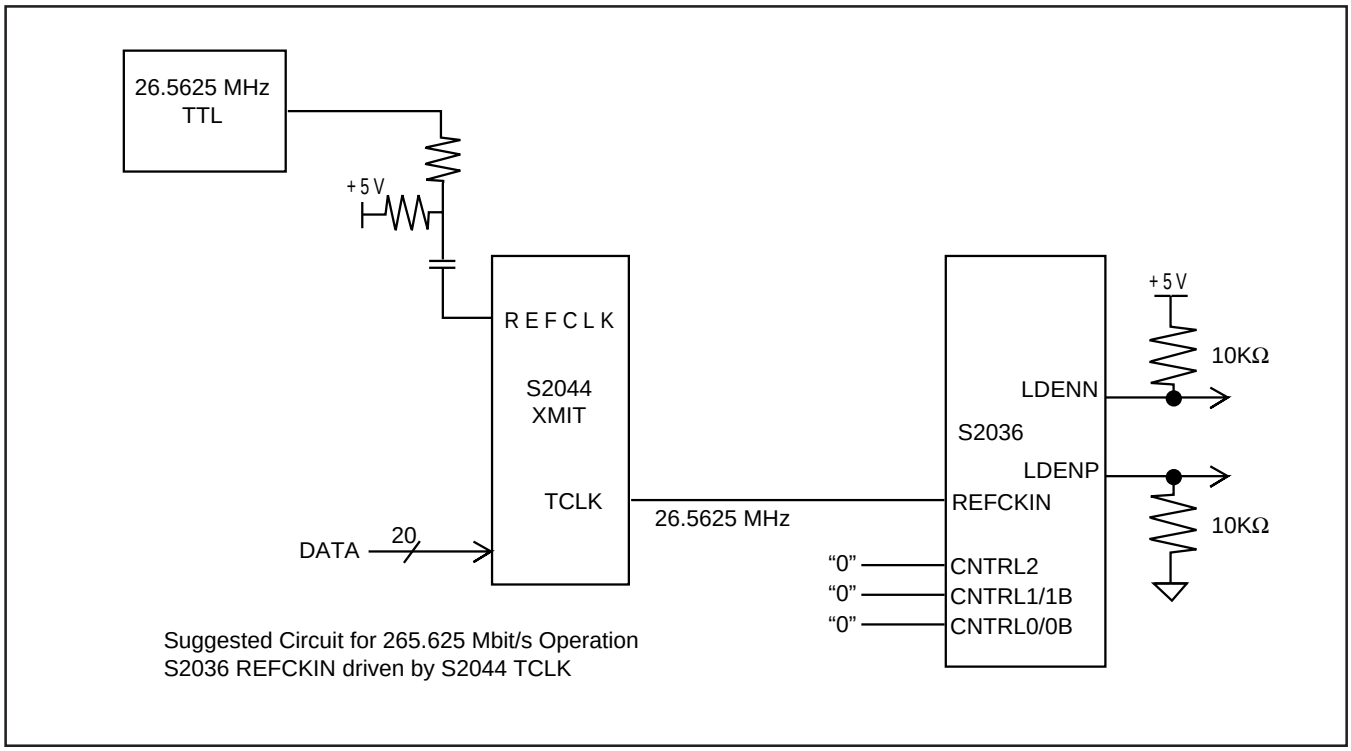


Figure 10. Suggested Circuit for 265.625 Mbit/s Operation with S2044 in 10-Bit Mode



LOL1/1B Single-Ended Application

The LOL1/LOL1B inputs are defined as PECL differential inputs. The macro design allows either input to be set to a fixed voltage in a range from 1.25V to 3.75V, and thus used as a threshold voltage for the other input. If the LOL1B input were connected to a resistor voltage divider providing ~1.5V, the LOL1 input can then be considered a single-ended TTL input. A suitable divider can be formed with a 33KW resistor and a 13KW resistor. For a Vcc of 5.0V, this would provide a threshold of 1.4V. If the TTL input levels of VIHmin = 2.0V and VILmax = 0.8V are assumed, the 1.4V threshold gives a minimum of 600mV of margin. The macro requires 300mV for reliable switching, so this threshold gives a 2x margin at worst case TTL input levels.

Figure 11. LOL1/1B Single-Ended TTL Input

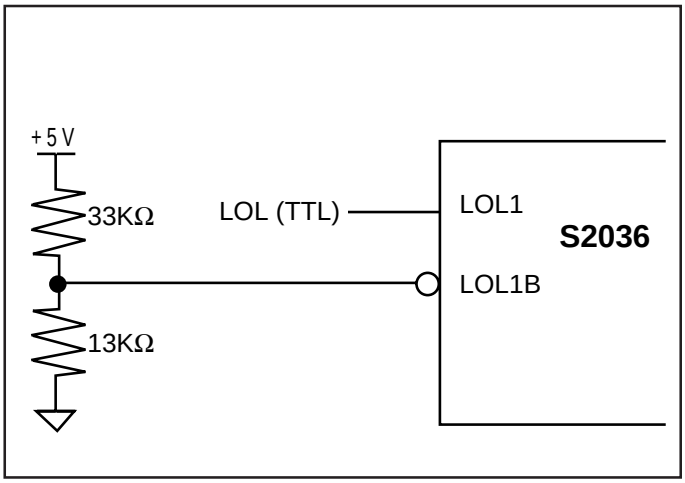
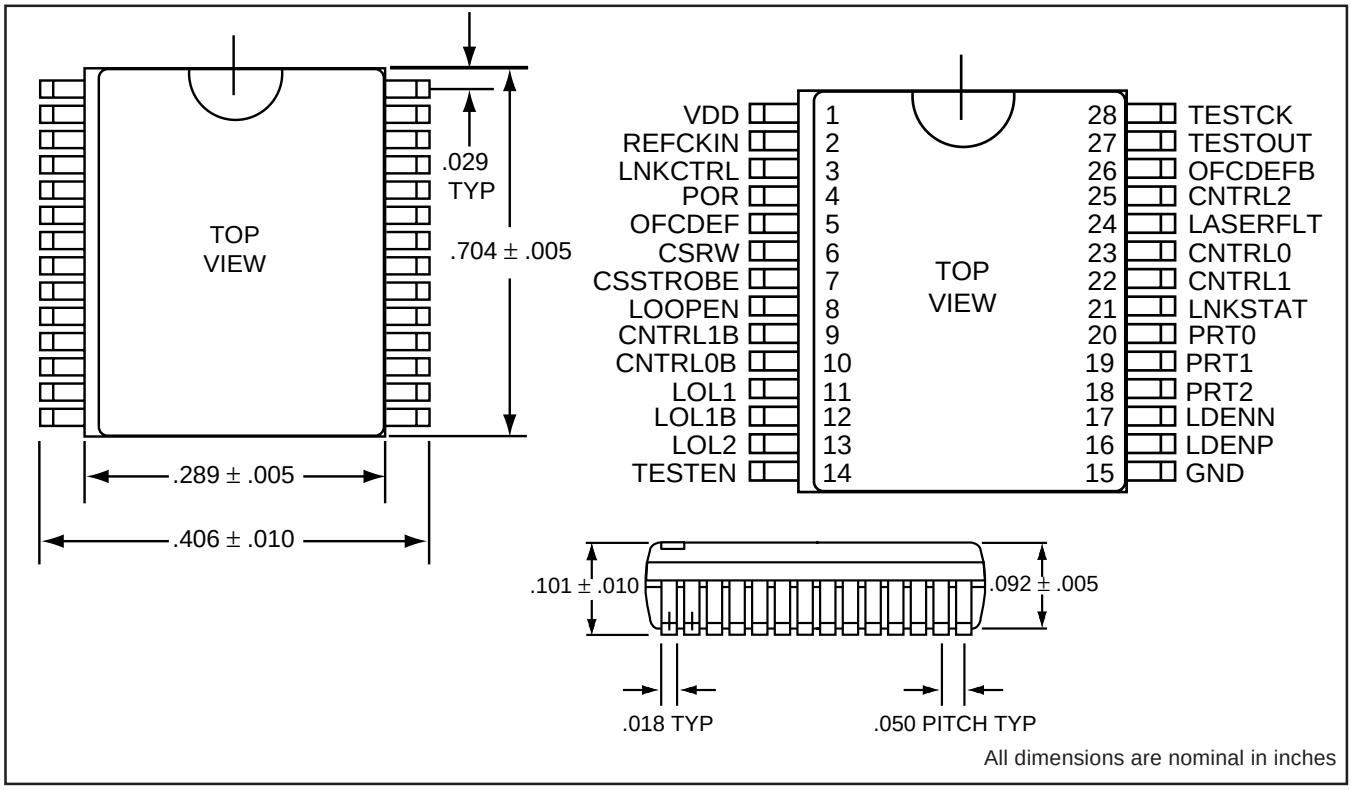


Figure 12. 28-Pin Package and Pinout



Absolute Maximum Ratings

Supply Voltage V_{DD}	7.0V	
TTL Input Voltage	V_{DD} + 0.3V	
Operating Junction Temperature T_J	+150°C	
Storage Temperature	-55° to +150°C	
Input Pin Current	-10mA to 10mA	25°C
Lead Temperature	300°C	10 sec.

Recommended Operating Conditions

Parameter	MIN	NOM	MAX	Unit
Supply Voltage (V_{DD})	4.75	5.0	5.25	V
Operating Temperature	0 ambient		70 ambient	°C
Junction Temperature			130	°C
Supply Current (I_{DD})		14	19	mA

PECL Input DC Characteristics V_{DD} = 4.75V to 5.25V

Symbol	Conditions	MIN	TYP	MAX	Unit
V_{IH}				V_{DD} – 600	mV
V_{IL}		V_{DD} – 2000			mV
V_{ID}		250[5]	500	1400	mV
I_{IH}				20	µA
I_{IL}		-1			µA

TTL Input/Output DC Characteristics

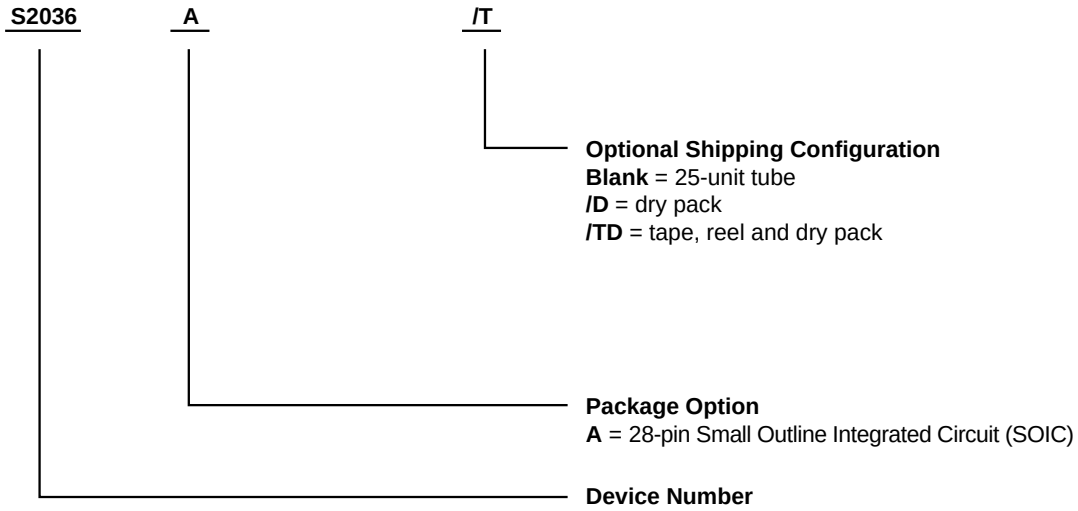
Symbol	Parameter	Test Conditions	COMM. 0° TO 70°C			Unit
			MIN	TYP[1]	MAX	
V_{IH}[2]	Input voltage HIGH	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}[2]	Input voltage LOW	Guaranteed input LOW voltage for all inputs			0.8	V
V_{OH}	Output voltage HIGH	V_{DD} = Min, I_{OH} = -4mA for TESTOUT -8mA for all other outputs	2.4			V
V_{OL}	Output voltage LOW	V_{DD} = Min, I_{OL} = 4 mA for TESTOUT 8 mA for all other outputs			0.4	V
I_{OZH}	Output “off” current HIGH	V_{DD} = Max, V_{OUT} = 2.4V	-10		10	µA
I_{OZL}	Output “off” current LOW	V_{DD} = Max, V_{OUT} = 0.4V	-10		10	µA
I_{IH}	Input current HIGH	V_{DD} = Max, V_{IN} = V_{DD} MAX			see note 3	µA
I_{IL}	Input current LOW	V_{DD} = Max, V_{IN} = 0V	see note 4			µA

1. Typical limits are at 25°C, V_{DD} = 5.0V.
2a. These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.
2b. Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for PECL testing.
3a. I_{IH} (min) = 36µA; I_{IH} (max) = 142µA for OFCDEF, TESTEN.
3b. I_{IH} (max) = 1µA for all other inputs.
4a. I_{IL} = -1µA for REFCKIN, LNKCTRL, POR, CSRW, CSSTROBE, LOOPEN, CNTRL1B, CNTRL0B, LOL2, CNTRL1, CNTRL0, LASERFLT, CNTRL2, TESTCK.
4b. I_{IL} (min) = -115µA; I_{IL} (max) = -33µA for OFCDEFB.
5. Not production tested.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations.
The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**



Example: S2036A
28-pin SOIC package, shipped in the standard tube, dry packed.

ISO 9001 CERTIFIED

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