REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23										
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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DRAWING APPROVAL DATE
92-03-10

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, PROCESSOR INTERFACE CIRCUIT, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88642
A	67268	

SHEET 1

DESC FORM 193
JUL 91

5962-E450

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Clock speed
01	P1754	Processor interface with system configuration inputs	20 MHz
02	P1754	Processor interface with system configuration inputs	30 MHz
03	P1754	Processor interface with system configuration inputs	40 MHz
04	P1754	Processor interface	20 MHz
05	P1754	Processor interface	30 MHz
06	P1754	Processor interface	40 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
T	See figure 2 (64-lead, 1.665" x .630" x .190"), dual-in-line package with gull-wing leads
U	See figure 2 (68-terminal, .955" x .955" x .115"), leaded chip carrier package with straight leads
X	See figure 2 (64-lead, 1.665" x .630" x .190"), dual-in-line package
Y	See figure 2 (68-terminal, .955" x .955" x .115"), leaded chip carrier package with gull-wing leads
Z	See figure 2 (68-pin, 1.160" x 1.160" x .290"), pin grid array package

1.3 Absolute maximum ratings.

Supply voltage range, V_{CC}	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Input current range	-30 mA to +5 mA
Current applied to any output	150 mA
Maximum power dissipation (P_D) 1/	1.5 W
Lead temperature range (soldering 10 seconds)	300°C
Thermal resistance, Θ_{JC}:	
Cases X and T	8°C/W
Cases Y and U	5°C/W
Case Z	6°C/W

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Operating power dissipation (P_D) (outputs open):	
Device types 01 and 04	0.25 W maximum
Device types 02 and 05	0.30 W maximum
Device types 03 and 06	0.35 W maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outline(s). The case outline(s) shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input high voltage	V_{IH}			1,2,3	All	2.0	V_{CC}+ 0.5	V
Input low voltage	V_{IL}			1,2,3	All	-0.5	0.8	V
Input clamp diode voltage	V_{CD}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1,2,3	All		-1.2	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V	I_{OH} = -8.0 mA	1,2,3	All	2.4		V
			I_{OH} = -300 µA			V_{CC}-0.2		V
Output low voltage, except A_0 - A_{15}	V_{OL}	V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V	I_{OL} = 8.0 mA	1,2,3	All		0.5	V
			I_{OL} = 300 µA				0.2	V
Output low voltage, A_0 - A_{15}	V_{OL}	V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V	I_{OL} = 20 mA	1,2,3	All		0.5	V
			I_{OL} = 300 µA				0.2	V
Input high current, except IB_0 - IB_{15}, parity/IB_{16}, SING ERR, A_0/EXT AD_0 A_1/EXT AD_1, STRBA	I_{IH}	V_{IN} = V_{CC}, V_{CC} = 5.5 V		1,2,3	All		10	µA
Input high current, IB_0-IB_{15}, parity/IB_{16}, A_0/EXT AD_0, A_1/EXT AD_1	I_{IH}			1,2,3	All		50	µA
Input high current, STRBA, SING ERR	I_{IH}	V_{IN} = V_{CC}, V_{CC} = 5.5 V		1,2,3	All		500	µA
Input low current, except IB_0 - IB_{15}, parity/IB_{16}, SING ERR, A_0/EXT AD_0 A_1/EXT AD_1, STRBD, $\overline{\text{TEST ON}}$	I_{IL}	V_{IN} = GND, V_{CC} = 5.5 V		1,2,3	All		-10	µA
Input low current, IB_0-IB_{15}, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1	I_{IL}			1,2,3	All		-50	µA
Input low current, STRBD, $\overline{\text{TEST ON}}$	I_{IL}			1,2,3	All		-500	µA

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output 3-state current	I_{OZH}	$V_{OUT} = 2.4\ V$, $V_{CC} = 5.5\ V$	1,2,3	All		50	µA
Output 3-state current	I_{OZL}	$V_{OUT} = 0.5\ V$, $V_{CC} = 5.5\ V$	1,2,3	All		-50	µA
Quiescent power supply current (CMOS input levels)	I_{CCQC}	$V_{IN} < 0.2\ V$ or $> V_{CC}-0.2\ V$, $f = 0$ MHz, outputs open, $V_{CC} = 5.5\ V$	1,2,3	All		10	mA
Quiescent power supply current (TTL input levels)	I_{CCQT}	$V_{IN} = 3.4\ V$, $f = 0$ MHz, all inputs, outputs open, $V_{CC} = 5.5\ V$	1,2,3	All		50	mA
Dynamic power supply current	I_{CCD}	$V_{IN} = 0\ V$ to V_{CC}, $tr = tf = 2.5$ ns typically, outputs open, $V_{CC} = 5.5\ V$	1,2,3	01,04		40	mA
				02,05		50	mA
				03,06		60	mA
Output short circuit current 2/	I_{OS}	$V_{OUT} = GND$, $V_{CC} = 5.5\ V$	1,2,3	All	-25		mA
Input capacitance	C_{IN}	See 4.3.1c, inputs only	4	All		10	pF
Output/bi-directional capacitance	C_{OUT}	See 4.3.1c, outputs, (including I/O buffers)	4	All		15	pF
Functional tests		See 4.3.1d, $V_{CC} = 4.5\ V$, $5.5\ V$	7,8	All			
Time from external ready to ready data valid	$TEX\ RDY-(RDYD)_V$	See figure 4, $V_{CC} = 4.5\ V$ 3/	9,10,11	01,04		16	ns
				02,05		14	ns
				03,06		12	ns
Time from clock read to ready data valid	$TC-(RDYD)_V$		9,10,11	01,04		28	ns
				02,05		22	ns
				03,06		16	ns
Time from strobe address high to address bus valid	$TSTRBA_H-(A)_V$		9,10,11	01,04		29	ns
				02,05		21	ns
				03,06		19	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Time from information bus address to address bus valid	$TIBA_V$-$(A)_V$	See figure 4, V_{CC} = 4.5 V 3/	9,10,11	01,04		31	ns
				02,05		22	ns
				03,06		20	ns
Time from falling clock to read low	$TFC(R)_L$		9,10,11	01,04		24	ns
				02,05		18	ns
				03,06		12	ns
Time from strobe data high to read high	$\overline{TSTRBD}_H$ - $(R)_H$		9,10,11	01,04		24	ns
				02,05		18	ns
				03,06		12	ns
Time from strobe data low to write low	$\overline{TSTRBD}_L$- $(W)_L$		9,10,11	01,04		26	ns
				02,05		20	ns
				03,06		15	ns
Time from strobe data high to write high	$\overline{TSTRBD}_H$- $(W)_H$		9,10,11	01,04		26	ns
				02,05		20	ns
				03,06		15	ns
Time from information bus data in to memory parity error low	$TIBD_{IN}$- $\overline{(ME\ PA\ ER)}_L$		9,10,11	01,04		22	ns
				02,05		17	ns
				03,06		12	ns
Time from information bus address in to external address error	$TIBA_{IN}$- $\overline{(EX\ AD\ ER)}$		9,10,11	01,04		30	ns
				02,05		25	ns
				03,06		20	ns
Time from strobe data low to start-up run valid	$\overline{TSTRBD}_L$ - $(STRT\ ROM)_V$		9,10,11	01,04		26	ns
				02,05		20	ns
				03,06		15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Time from falling clock to information bus valid	TFC-(IB OUT)$_V$	See figure 4, V_{CC} = 4.5 V 3/	9,10,11	01,04		30	ns
				02,05		25	ns
				03,06		25	ns
Time from rising edge of clock to timer clock	TC-(TIMER CLK)		9,10,11	01,04		30	ns
				02,05		25	ns
				03,06		20	ns
Time from information bus data to parity valid	TIB IN$_V$-(IB16)		9,10,11	01,04		25	ns
				02,05		20	ns
				03,06		18	ns
Extended address setup time	TEXT AD (CLKB3)		9,10,11	01,04	10		ns
				02,05	10		ns
				03,06	10		ns
Time from external ready data to ready data valid	$\overline{\text{TEX RDY1}}$-(RDYD)$_V$		9,10,11	01,04		28	ns
				02,05		24	ns
				03,06		21	ns
Time from falling clock to SCR SCR enable; case types T and X only	TFC-(SCR EN)		9,10,11	01,04		30	ns
				02,05		24	ns
				03,06		24	ns
Time from STRBD high to SCR enable; case types T and X only	$\overline{\text{TSTRBD}}_H$-(SCR EN)		9,10,11	01,04		30	ns
				02,05		24	ns
				03,06		24	ns

1/ Unless otherwise specified, all testing shall be conducted under worst-case conditions.
2/ Only one output may be shorted at a time.
3/ All measurements of delay times on active signals are related to the 1.5 V levels.

Device types	04, 05, 06							
Case outlines	T and X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	17	IB_8	33	A_{15}	49	A_0/EXT AD_0
2	SCR EN	18	IB_9	34	A_{14}	50	TC
3	$\overline{\text{TEST ON}}$	19	GND	35	A_{13}	51	CPU CLK
4	V_{CC}	20	IB_{10}	36	A_{12}	52	STRBA
5	$\overline{\text{RESET}}$	21	IB_{11}	37	A_{11}	53	$\overline{\text{STRBD}}$
6	TEST END	22	IB_{12}	38	A_{10}	54	STRB EN
7	TIMER CLK	23	IB_{13}	39	A_9	55	EX RDY
8	EX RDY1	24	IB_{14}	40	A_8	56	RDYD
9	IB_0	25	IB_{15}	41	A_7	57	R/$\overline{W}$
10	IB_1	26	IB_{16}	42	A_6	58	GND
11	IB_2	27	$\overline{\text{ME PA ER}}$/RAM DIS	43	A_5	59	M/$\overline{IO}$
12	IB_3	28	EX AD ER/SING ERR	44	A_4	60	$\overline{\text{MEMW}}$
13	IB_4	29	$\overline{\text{INTA}}$	45	A_3	61	$\overline{\text{MEMR}}$
14	IB_5	30	STRT ROM	46	GND	62	$\overline{\text{IOW}}$
15	IB_6	31	V_{CC}	47	A_2	63	$\overline{\text{IOR}}$
16	IB_7	32	GND	48	A_1/EXT AD_1	64	V_{CC}

FIGURE 1. Terminal connections.

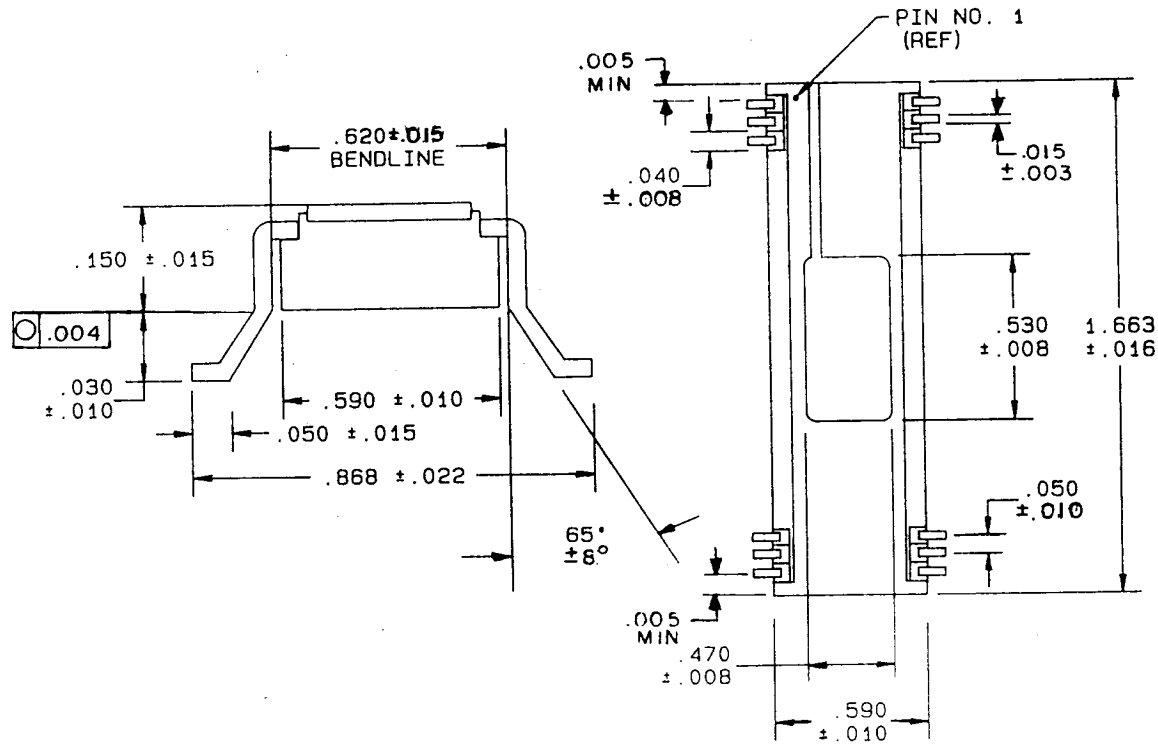
Device types	01, 02, 03							
Case outlines	U and Y							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	$\overline{\text{EX RDY1}}$	35	A_{15}	52	SC_4
2	SC_0	19	IB_8	36	A_{14}	53	SC_3
3	SC_1	20	IB_9	37	A_{13}	54	TC
4	$\overline{\text{TEST ON}}$	21	GND	38	A_{12}	55	CPU CLK
5	$\overline{\text{RESET}}$	22	IB_{10}	39	A_{11}	56	STRBA
6	TEST END	23	IB_{11}	40	A_{10}	57	STRBD
7	TIMER CLK	24	IB_{12}	41	A_9	58	$\overline{\text{STRB EN}}$
8	SC_2	25	IB_{13}	42	A_8	59	EX RDY
9	V_{CC}	26	IB_{14}	43	A_7	60	RDYD
10	IB_0	27	IB_{15}	44	A_6	61	R/$\overline{\text{W}}$
11	IB_1	28	PARITY/IB_{16}	45	A_5	62	GND
12	IB_2	29	ME PA ER/RAM DIS	46	A_4	63	M/IO
13	IB_3	30	$\overline{\text{EX AD ER/SING ERR}}$	47	A_3	64	$\overline{\text{MEMW}}$
14	IB_4	31	INTA	48	GND	65	MEMR
15	IB_5	32	STRT ROM	49	A_2	66	$\overline{\text{IOW}}$
16	IB_6	33	V_{CC}	50	A_1/EXT AD_1	67	IOR
17	IB_7	34	GND	51	A_0/EXT AD_0	68	V_{CC}

FIGURE 1. Terminal connections - Continued.

Device types	01, 02, 03							
Case outline	Z							
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
B1	V_{CC}	L2	GND	K11	EX RDY	A10	GND
B2	IB_{14}	K2	SC_2	K10	STRB EN	B10	A_8
C1	IB_{13}	L3	TIMER CLK	J11	$\overline{\text{STRBD}}$	A9	A_9
C2	IB_{12}	K3	TEST END	J10	STRBA	B9	A_{10}
D1	IB_{11}	L4	$\overline{\text{RESET}}$	H11	CPU CLK	A8	A_{11}
D2	IB_{10}	K4	TEST ON	H10	TC	B8	A_{12}
E1	IB_9	L5	SC_1	G11	SC_3	A7	A_{13}
E2	IB_8	K5	SC_0	G10	SC_4	B7	A_{14}
F1	$\overline{\text{EX RDY1}}$	L6	V_{CC}	F11	A_0/EXT AD_0	A6	A_{15}
F2	IB_7	K6	$\overline{\text{IOR}}$	F10	A_1/EXT AD_1	B6	GND
G1	IB_6	L7	$\overline{\text{IOW}}$	E11	A_2	A5	V_{CC}
G2	IB_5	K7	MEMR	E10	GND	B5	STRT ROM
H1	IB_4	L8	$\overline{\text{MEMW}}$	D11	A_3	A4	$\overline{\text{INTA}}$
H2	IB_3	K8	M/IO	D10	A_4	B4	EX AD ER
J1	IB_2	L9	GND	C11	A_5	A3	$\overline{\text{ME PA ER}}$
J2	IB_1	K9	R/W	C10	A_6	B3	IB_{16}/PARITY
K1	IB_0	L10	RDYD	B11	A_7	A2	IB_{15}

FIGURE 1. Terminal connections - Continued.

Device types 04, 05, and 06



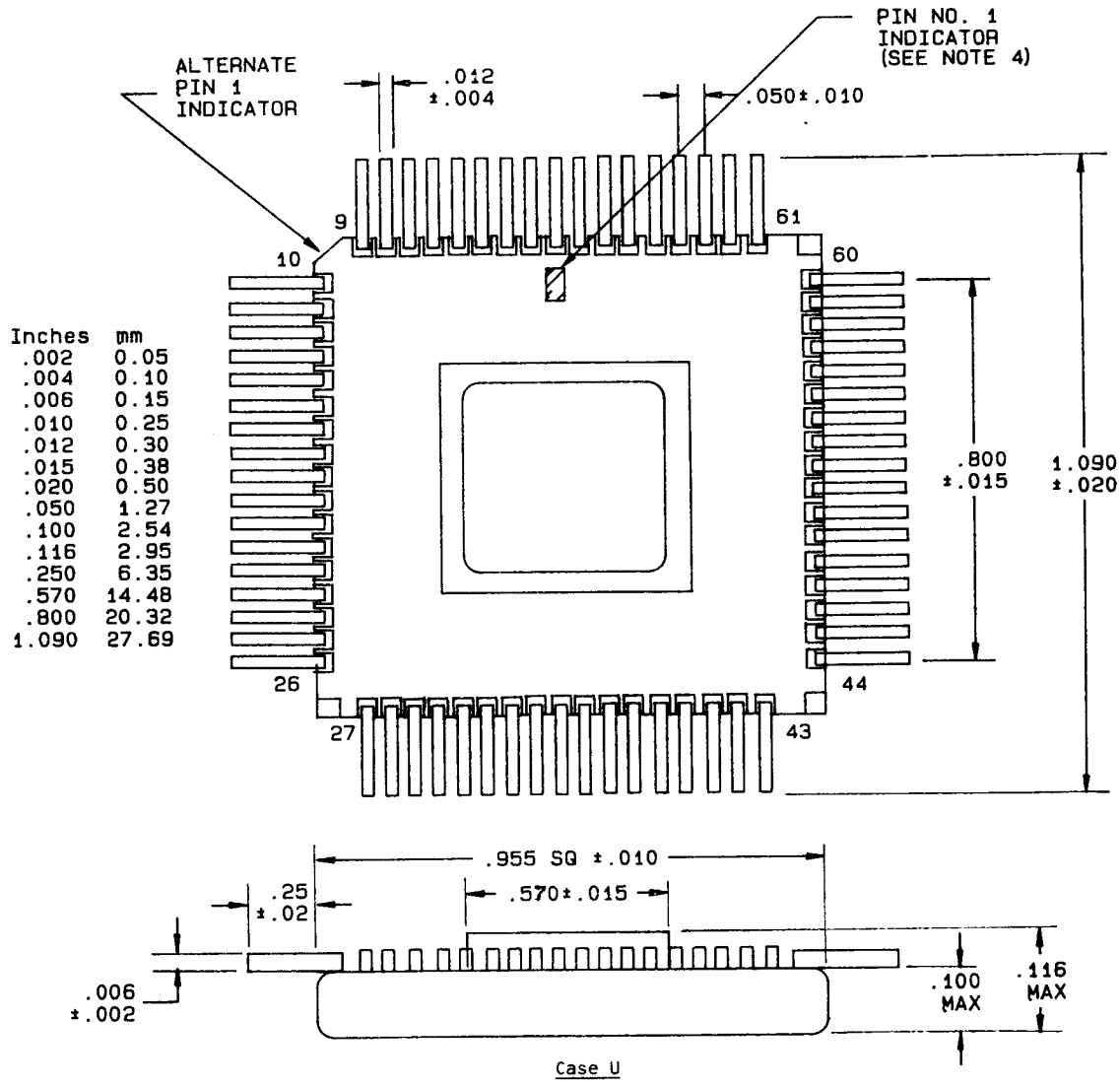
Inches	mm	Inches	mm
.003	0.08	.040	1.01
.004	0.10	.050	1.27
.005	0.13	.150	3.81
.008	0.20	.470	11.93
.010	0.25	.530	13.46
.015	0.38	.590	14.98
.016	0.41	.620	15.74
.022	0.55	.868	22.04
.030	0.76	1.663	42.24

Case T

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.51 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

FIGURE 2. Case outlines.

Device types 01, 02, and 03



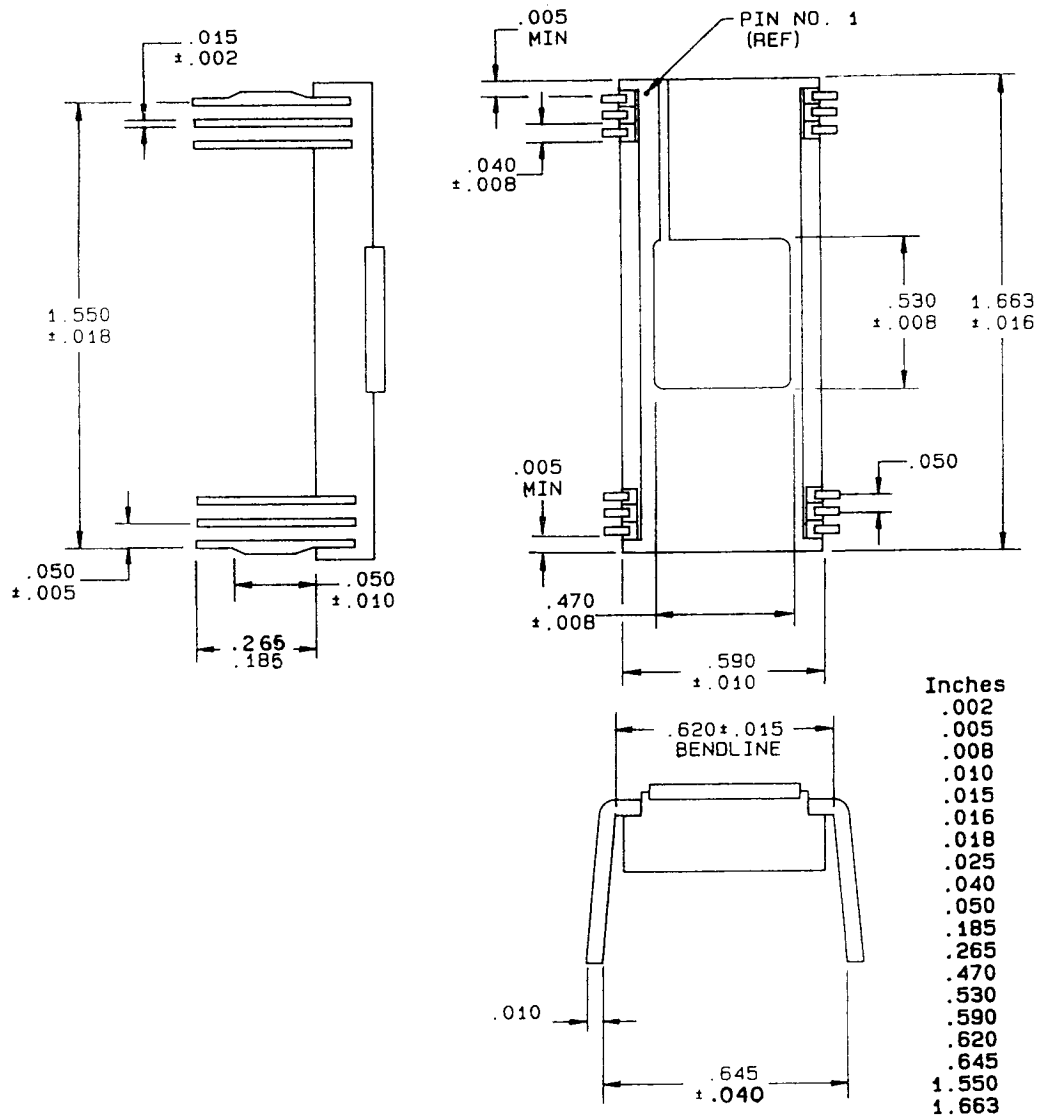
Inches	mm
.002	0.05
.004	0.10
.006	0.15
.010	0.25
.012	0.30
.015	0.38
.020	0.50
.050	1.27
.100	2.54
.116	2.95
.250	6.35
.570	14.48
.800	20.32
1.090	27.69

Case U

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.51 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Pin 1: Indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5. Corners indicated as notched may be either notched or square (with radius).

FIGURE 2. Case outlines - Continued.

Device types 04, 05, and 06



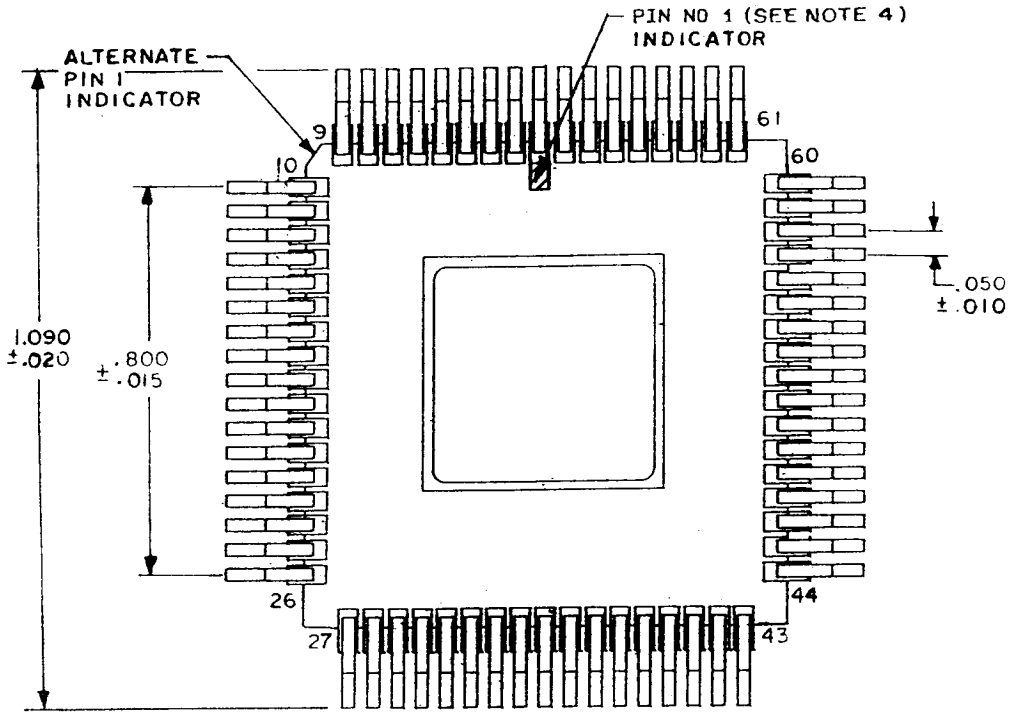
Inches	mm
.002	0.05
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.40
.018	0.45
.025	0.63
.040	1.01
.050	1.27
.185	4.70
.265	6.73
.470	11.93
.530	13.46
.590	14.98
.620	15.74
.645	16.38
1.550	39.37
1.663	42.24

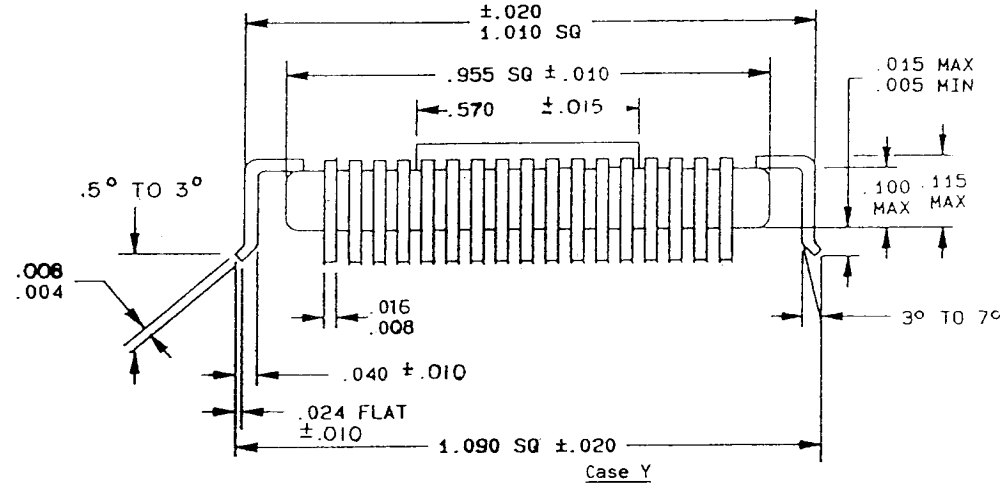
Case X

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.51 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

FIGURE 2. Case outlines - Continued.

Device types 01, 02, and 03





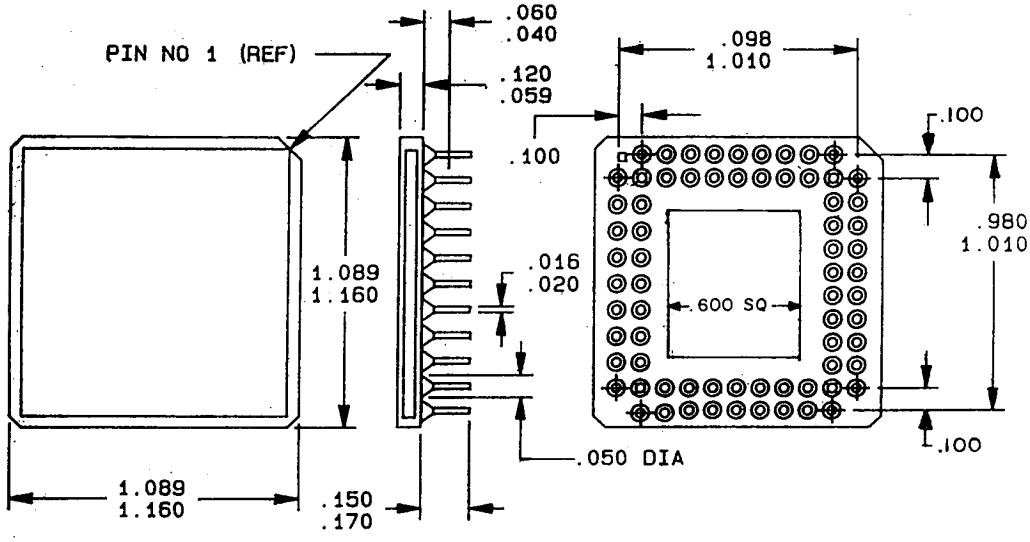
Case Y

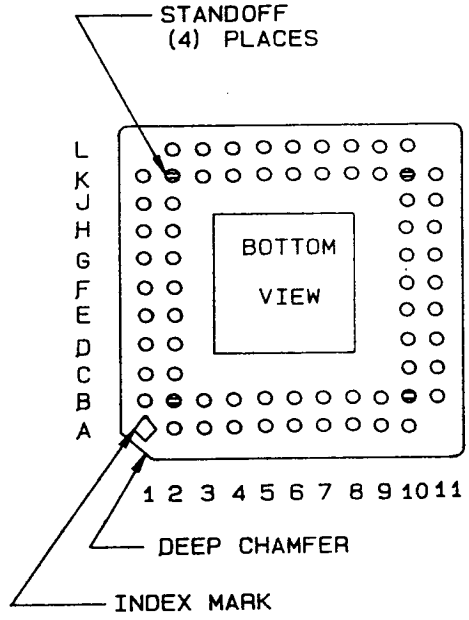
Inches	mm
.004	0.10
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.41
.020	0.51
.024	0.61
.040	1.02
.050	1.27
.100	2.54
.115	2.92
.570	14.48
.800	20.32
.955	24.26
1.010	25.65
1.090	27.68

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.51 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Pin 1: Indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5. Corners indicated as notched may be either notched or square (with radius).

FIGURE 2. Case outlines - Continued.

Device types 01, 02, and 03





Inches	mm	Inches	mm
.010	0.25	.120	3.04
.016	0.41	.150	3.81
.020	0.50	.170	4.32
.040	1.01	.600	15.24
.050	1.27	.980	24.89
.059	1.49	1.010	25.65
.060	1.52	1.089	27.66
.100	2.54	1.160	29.46

Case Z

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.51 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Pin 1: Indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.

FIGURE 2. Case outlines - Continued.

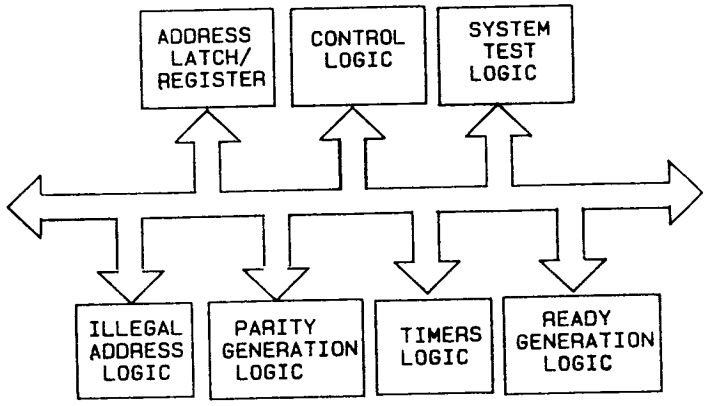
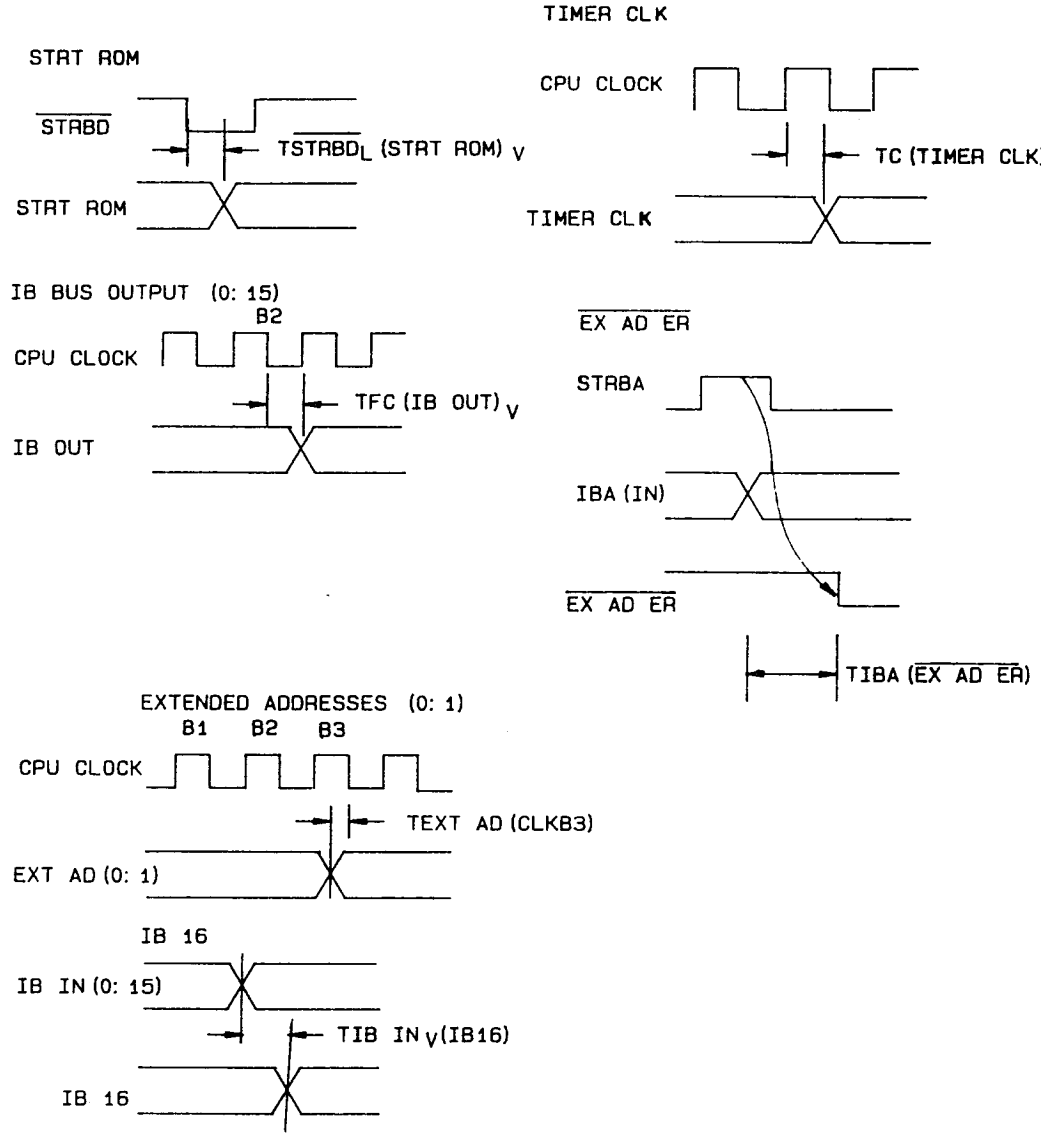


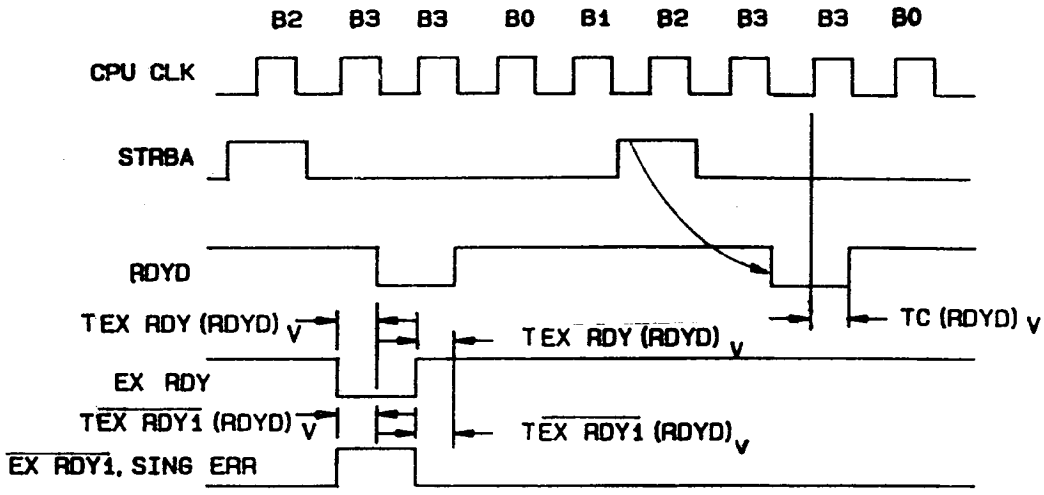
FIGURE 3. Functional block diagram.



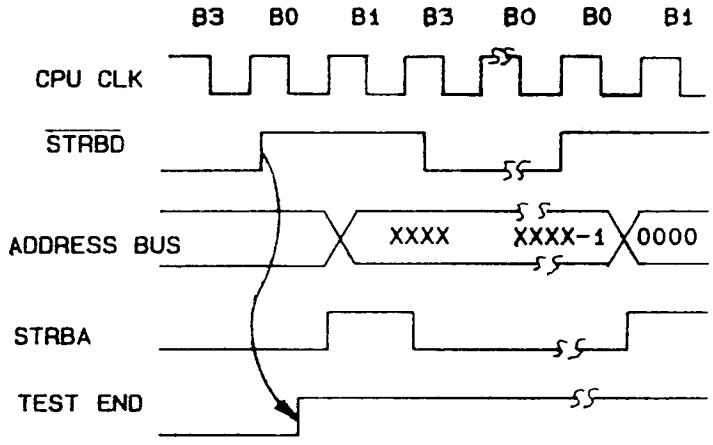
NOTE: All timing measurements on active signals relate to 1.5 V levels.

FIGURE 4. Switching waveforms and test circuit.

RDYD TIMING



TEST END TIMING (NOTE 1)

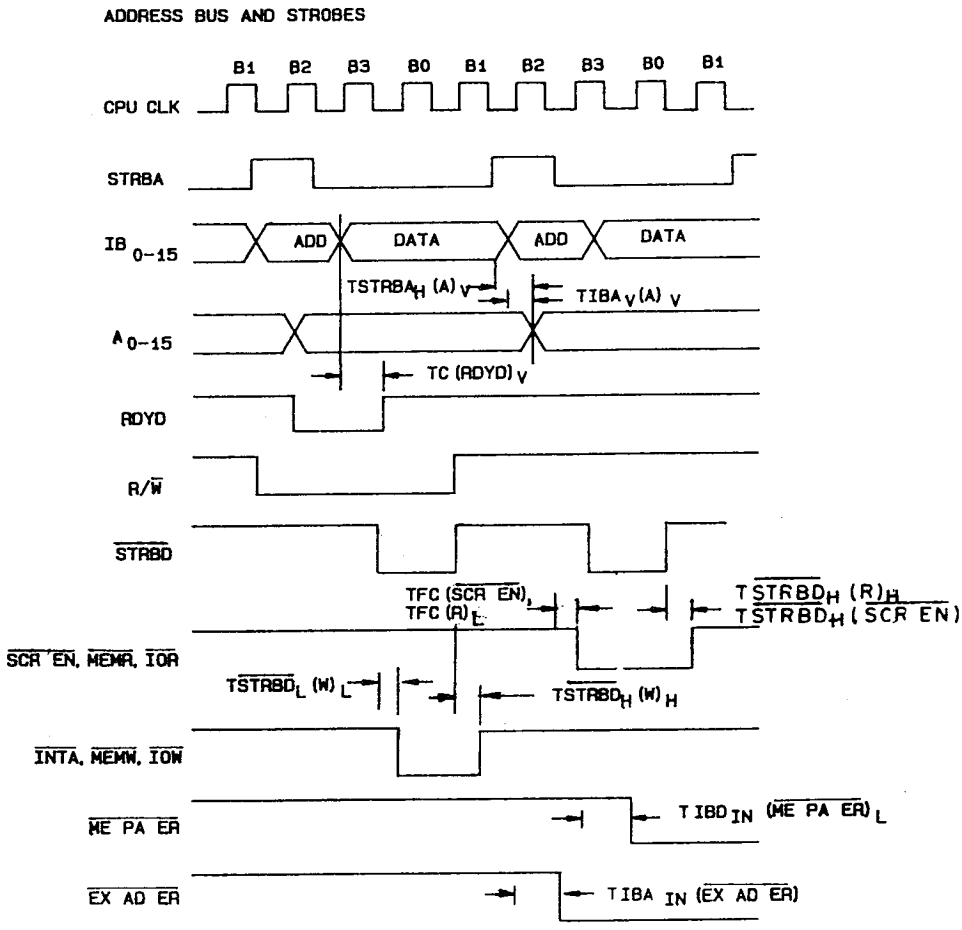


NOTES:

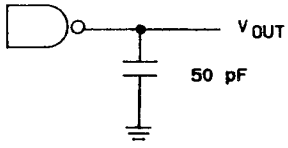
1. The last two instructions executed during system test are: XIO RA, 1F44, 0 and JC 7, 0000 hex, 0. After execution of the IOW bus cycle, the XIO proceeds by filling the instruction pipe with two memory read bus cycles where the opcode 7070 hex and 0000 hex are entered to the processor. As from the end of STRBD in the second cycle, TEST END is asserted. At this point, the execution of IC starts by first issuing two fetch cycles from the "old PC" (from addresses XXXX & XXXX+1). The data will be taken from system memory (because TEST END is asserted) but both the address and data are irrelevant. Following that, IC will start filling the pipe from address 0000 hex and 0001 hex, now from the system memory to start user's program execution.

2. All timing measurements on active signals relate to 1.5 V levels.

FIGURE 4. Switching waveforms and test circuit - Continued.



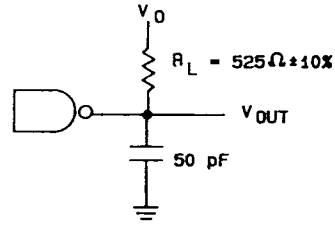
Standard output (non three-state)



Switching time test circuits

Parameter	V_O	V_{MEA}
TPLZ	≥ 3 V	0.5
TPHZ	0 V	V_{CC} - .5V
TPXL	$V_{CC}/2$	1.5 V
TPXH	$V_{CC}/2$	1.5 V

Three-state



NOTE: All timing measurements on active signals relate to 1.5 V levels.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 2, 7, 8A
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Additional electrical subgroups for group C periodic inspections	-----

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECT, telephone (513) 296-6022.

6.5 Pin descriptions. See table III.

6.6 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

TABLE III. Pin descriptions.

Mnemonic	Name	Description
CPU CLK	CPU Clock	A single phase input clock signal (0-40 MHz, 40% to 60% duty cycle).
STRBA	Strobe Address	An active high input which latches the contents of IB(0:15) into the address latches.
$\overline{\text{STRBD}}$	Strobe Data	An active low input which is used for writing or reading data to or from the device and also to produce the external memory and I/O strobes.
TIMER CLK	Timer Clock	A 100 kHz output (fixed frequency) based on the programmed operating frequency of the CPU clock.
$\overline{\text{MEMW}}$	Memory Write Strobe	An active low output produced in memory write cycles.
$\overline{\text{MEMR}}$	Memory Read Strobe	An active low output produced in memory read cycles.
$\overline{\text{IOW}}$	I/O Write Strobe	An active low output produced in output write cycles.
$\overline{\text{IOR}}$	I/O Read Strobe	An active low output produced in input read cycles.
$\overline{\text{INTA}}$	Interrupt Acknowledge Strobe	An active low output produced after any interrupt, corresponding to an output write to address 1000 (Hex).
$\overline{\text{SCR EN}}$	System Configuration	An active low output (in 64 pin only) produced any time an input read from address 8410 (Hex), read system configuration is executed.
$\overline{\text{STRB EN}}$	Strobe Enable	An active low input, enabling the active state of the address outputs and the MEMR, MEMW, IOR, and IOW outputs. When at a logic "1" (if enabled by bits EST, EAD of the control register) it will correspondingly enable the three-state state of the above signals.
IB(0:15)	Information Bus (0:15)	A bidirectional time multiplexed bus. It is an input during the address phase of any bus cycle and also during the data phase when writing. It is an output during the data phase when reading from the device.
IB16	Information Bus 16	A bidirectional line. It is an output during write cycles and an input during read cycles. It is used to implement the parity function at the system level.
A(0:1)/ EXT AD(0:1), A(2:15)	Address Bus (0:15)	An active high output bus. Contains the address of the current bus cycle as latched by the end of STRBA. In system configurations including the MMU function, the only active lines during memory are A(4:15). In this case, A(2:3) are high impedance (don't care) and A(0:1) turn into inputs called Extended Addresses, EXT ADR (0:1). In this case these two lines supplied by the MMU, will be used to operate the programmable ready generation during bus cycles.
M/$\overline{\text{IO}}$	Memory I/O	An input qualifier indicating the nature of the current bus cycle.

TABLE III. Pin descriptions - Continued.

Mnemonic	Name	Description
R/$\overline{W}$	Read/Write	An input qualifier indicating the nature of the current bus cycle, either Read (1) or Write (0).
$\overline{RESET}$	External Reset	An active low input used to initialize the devices's hardware.
$\overline{TEST\ ON}$	System Test Enable	An active low input used to enable the execution of the System Test built into the device, immediately after completion of the 5962-87665 initialization and before fetching any instruction from the user program.
TEST END	System Test End	An active high output indicating whether the system test in the device has been completed. Whenever the system test is disabled by the TEST ON signal, the TEST END output will be at a logical "1" immediately after RESET is removed.
STRT ROM	Start Up ROM	An output following the execution of the ESUR and DSUR, I/O commands as defined in MIL-STD-1750A. It will be at the logical "1" level after executing ESUR and at the logical "0" level after executing DSUR. Initially, it defaults to a logical "1".
RDYD	Ready Data	An active high output to be connected to the 5962-87665 input to control the bus cycle termination.
EX RDY	External Ready Data	An active high input which at logical "0" overrides the internal RDYD generation and forces it to a logical "0".
$\overline{EX\ RDY1}$	External Ready Data	An active low input which at logical "1" overrides the internal RDYD generation and forces it to a logical "0".
$\overline{ME\ PA\ ER}$/ RAM DIS	Memory Parity Error	An active low output indicating a parity error when reading from memory. It becomes an active high output called RAM DISABLE for handshaking with the 5962-89505 when the device is programmed to support EDAC.
$\overline{EX\ AD\ ER}$/ SING ERR	Illegal Address Error	An active low output indicating an illegal address error when referencing memory or I/O. It becomes an active high input called SINGLE ERROR for handshaking with the 5962-89505 when the device is programmed to support EDAC.
TC	Terminal Count	An active high output indicating a Bus time out or a watchdog trigger.
SC0-SC4	System Configuration	Inputs (for case outlines U, Y, and Z only) which are buffered onto IB0-IB4 when executing an I/O read from I/O address 8410 (Hex), system configuration.
GND	Ground	0 volts system ground.
VCC	Power Supply	5 volts ± 10% power supply.