



SRAM

512K x 8 SRAM

ULTRA HIGH SPEED-PLASTIC SRAM
REVOLUTIONARY PINOUT

MILITARY TEMPERATURE

OPERATING RANGE -55°C to +125°C

FEATURES

- Ultra High Speed, 83MHz Asynchronous Operation
- Extended Testing Over -55°C to +125°C
- Fully Static, No Clocks
- Data Retention Functionality Testing (Contact Factory)
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible
- Plastic 36 pin PSOJ is fully compatible with the Ceramic 36 pin SOJ
- Single +5V Power Supply +/- 10%
- 3.3V Future Offering
- Industrial and Military Temperature Range
- Cost Efficient Plastic Packaging

OPTIONS MARKING

• Timing

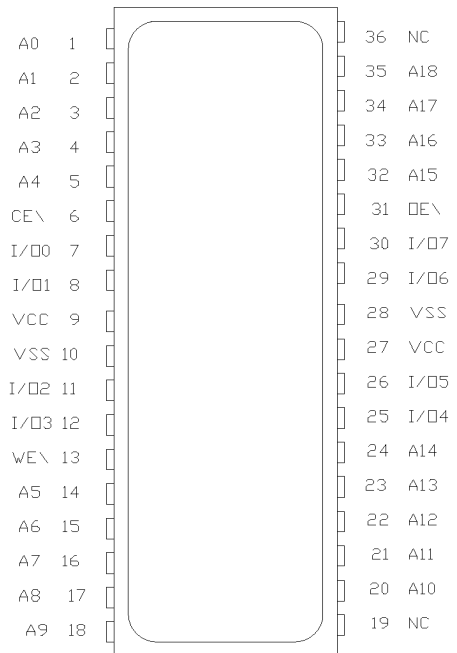
12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20

• Package(s)

Plastic SOJ	ECJ	No. 503
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PIN ASSIGNMENT (Top View)

36-Pin PSOJ



GENERAL DESCRIPTION

The AS5C512K8DJ offers the convenience and reliability of the AS5C512K8DJ SRAM and has the cost advantage of a durable plastic.

The AS5C512K8DJ is tested to military specifications. When a device is operated beyond commercial temperatures the overall characteristics of the device will change. ASI ensures that this device will behave in an expected manner in military applications due to the extensive characterizations performed to meet military standards.

ASI certifies that the AS5C512K8DJ will retain data in Data Retention Mode under operating conditions characterized during test conditions. This is a crucial point for systems that operate under extreme temperature

conditions.

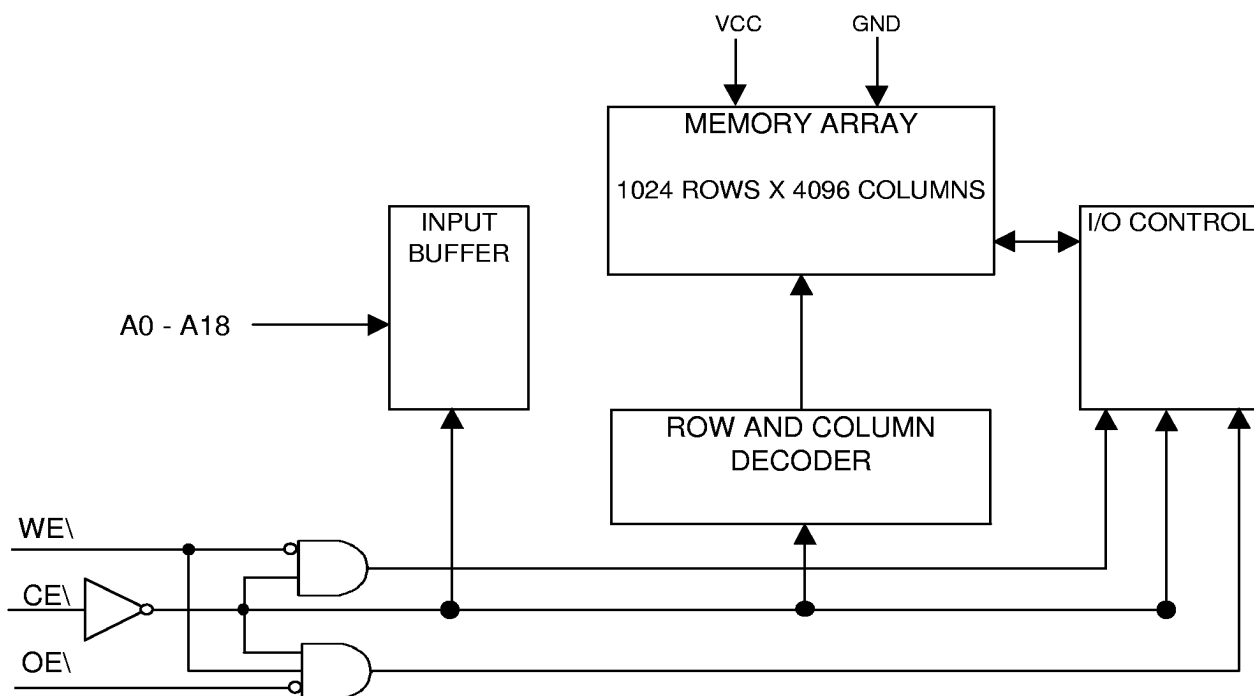
For flexibility in high-speed memory applications, ASI offers chip enable (CE\) and output enable (OE\) capabilities.

These features can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

The AS5C512K8DJ is PSOJ footprint compatible with SMD 5692-95600.

**FUNCTIONAL BLOCK DIAGRAM****TRUTH TABLE**

MODE	OE\	CE\	WE\	I/O	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

X = Don't Care

PIN FUNCTIONS

A0 - A18	Address Inputs
WE\	Write Enable
CE\	Chip Enable
OE\	Output Enable
I/O ₀ - I/O ₇	Data Inputs/Outputs
V _{CC}	Power
V _{SS}	Ground
NC	No Connection



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss

Vcc-5V to +7.0V

Storage Temperature (Plastics)-65°C to +150°C

Short Circuit Output Current (per I/O).....20mA

Voltage on any Pin Relative to Vss.....-5V to Vcc+1 mA

Junction Temperature**+150°C

Power Dissipation1 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the

device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. ** Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%) - Military Temps

SYMBOL	DESCRIPTION	CONDITIONS	-12		-15		-17		-20		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I _{CC}	Power Supply Current: Operating	CE\ ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/1 RC OUTPUTS OPEN		220		215		205		195	mA	3
I _{SBT1}	Power Supply Current: Standby	CE\ ≥ V _{IH} ; V _{CC} = MAX f = MAX = 1/1 RC OUTPUTS OPEN		65		55		50		50	mA	
I _{SBC}		CE\ ≥ V _{CC} -0.2V; V _{CC} = MAX V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{CC} -0.2V; f = 0		10		10		10		10	mA	
V _{IH}	Input High (Logic 1) Voltage		2.2	V _{CC} +5	2.2	V _{CC} +5	2.2	V _{CC} +5	2.2	V _{CC} +5	V	1
V _{IL}	Input Low (Logic 0) Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8		1,2
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	-5	5	-5	5	-5	5	-5	5	μA	
I _{LO}	Output Leakage Current	Output(s) disabled 0V ≤ V _{OUT} ≤ V _{CC}	-5	5	-5	5	-5	5	-5	5	μA	
V _{OH}	Output High Voltage	I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V	1
V _{OL}	Output Low Voltage	I _{OL} = 8 mA		0.4		0.4		0.4		0.4	V	1
V _{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V	1

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T A ≤ 85°C; Vcc = 5V ±10%) - Industrial Temps

SYMBOL	DESCRIPTION	CONDITIONS	-12		-15		-17		-20		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I _{CC}	Power Supply Current: Operating	CE\ ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/1 RC OUTPUTS OPEN		210		205		195		185	mA	3
I _{SBT1}	Power Supply Current: Standby	CE\ ≥ V _{IH} ; V _{CC} = MAX f = MAX = 1/1 RC OUTPUTS OPEN		50		50		50		50	mA	
I _{SBC}		CE\ ≥ V _{CC} -0.2V; V _{CC} = MAX V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{CC} -0.2V; f = 0		10		10		10		10	mA	
V _{IH}	Input High (Logic 1) Voltage		2.2	V _{CC} +5	2.2	V _{CC} +5	2.2	V _{CC} +5	2.2	V _{CC} +5	V	1
V _{IL}	Input Low (Logic 0) Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8		1,2
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	-2	2	-2	2	-2	2	-2	2	μA	
I _{LO}	Output Leakage Current	Output(s) disabled 0V ≤ V _{OUT} ≤ V _{CC}	-2	2	-2	2	-2	2	-2	2	μA	
V _{OH}	Output High Voltage	I _{OH} = -4.0mA	2.4		2.4		2.4		2.4		V	1
V _{OL}	Output Low Voltage	I _{OL} = 8 mA		0.4		0.4		0.4		0.4	V	1
V _{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V	1

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes 5) ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-17		-20			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle Time	^t RC	12		15		17		20		ns	
Address access time	^t AA		12		15		17		20	ns	
Chip Enable access time	^t ACE		12		15		17		20	ns	
Output hold from address change	^t OH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^t LZCE	2		2		2		2		ns	4, 6, 7
Chip disable to output in High-Z	^t HZCE		6		7		8		8	ns	4, 6, 7
Chip Enable to power-up time	^t PU	0		0		0		0		ns	4
Chip disable to power-down time	^t PD		12		15		17		20	ns	4
Output Enable access time	^t AOE		6		7		8		8	ns	
Output Enable to output in Low-Z	^t LZOE	0		0		0		0		ns	4, 6, 7
Output disable to output in High-Z	^t HZOE		6		7		8		8	ns	4, 6, 7
WRITE Cycle											
WRITE cycle time	^t WC	12		15		17		20		ns	
Chip Enable to end of write	^t CW	9		10		11		12		ns	
Address valid to end of write	^t AW	9		10		11		12		ns	
Address setup time	^t AS	0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		ns	
WRITE pulse width (OE\ High)	^t WP1	9		10		11		12		ns	
WRITE pulse width (OE\ Low)	^t WP2	12		13		14		15		ns	
Data setup time	^t DS	6		7		7		8		ns	
Data hold time	^t DH	0		0		0		0		ns	
Write disable to output in Low-Z	^t LZWE	2		2		2		2		ns	4, 6, 7
Write Enable to output in High-Z	^t HZWE		6		7		8		8	ns	4, 6, 7

**AC TEST CONDITIONS**

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

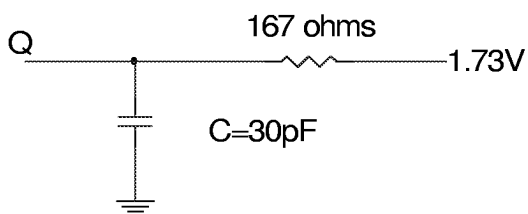


Fig. 1 Output Load Equivalent

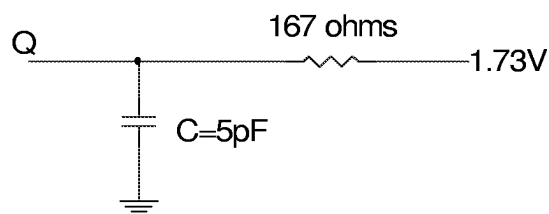


Fig. 2 Output Load Equivalent

CAPACITANCE

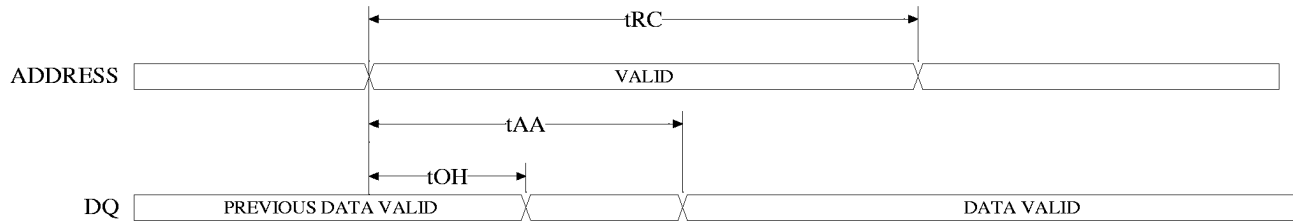
DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Output Capacitance	T _A = 25°C; 1 = MHz	C _I	8	pF	4
Input Capacitance	V _{CC} = 5V	C _O	8	pF	4

NOTES

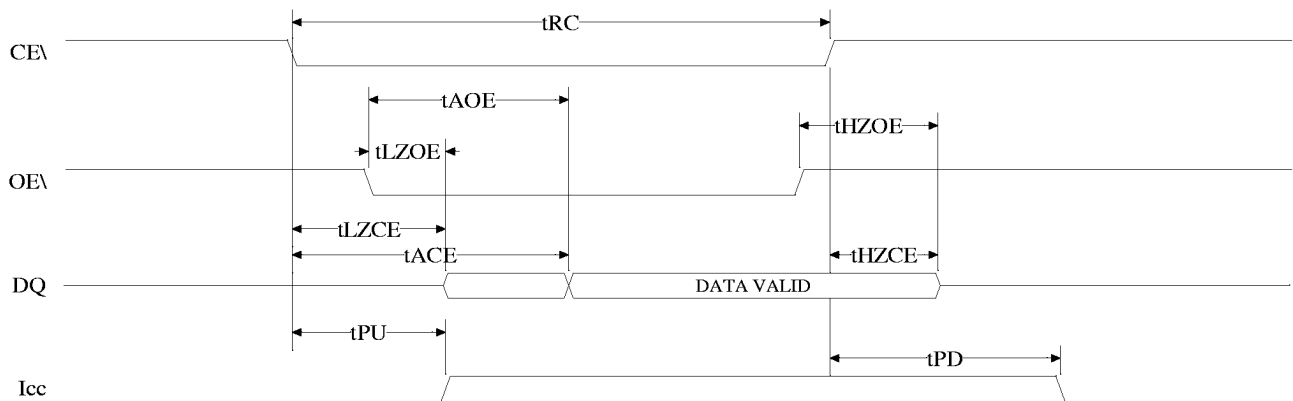
1. All voltages referenced to V_{ss} (GND).
2. -2V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. 'LZCE, 'LZWE, 'LZOE, 'HZCE, 'HZOE and 'HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, 'HZCE is less than 'LZCE, and 'HZWE is less than 'LZWE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. 'RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable (OE\) is inactive (HIGH).
14. Output enable (OE\) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

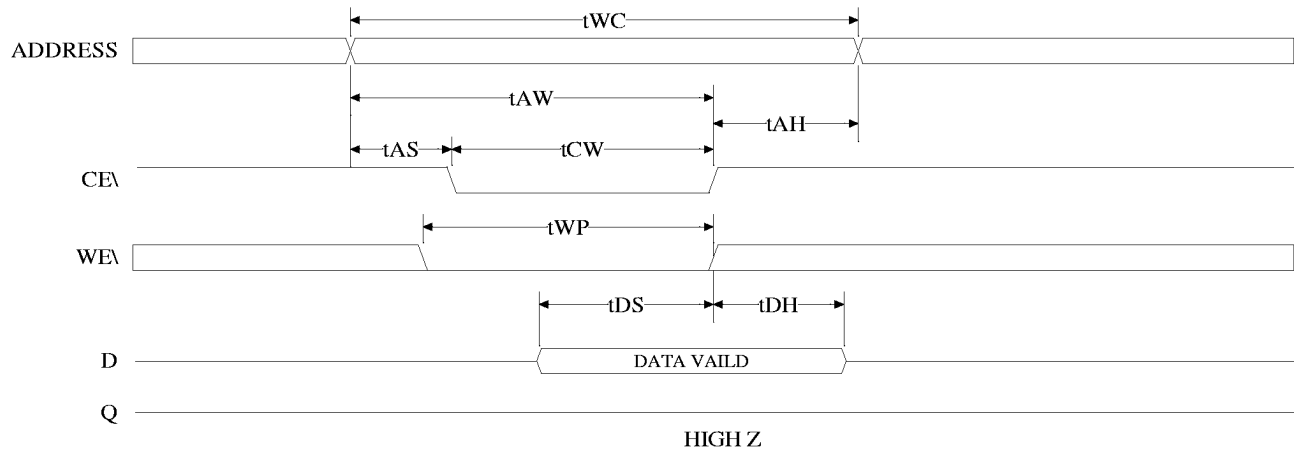
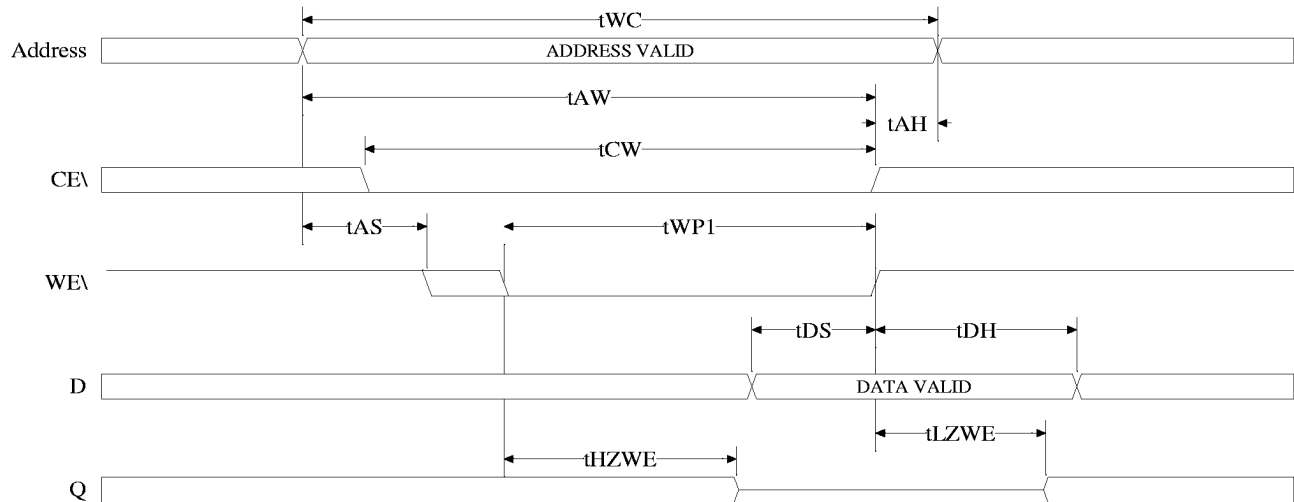


READ CYCLE NO. 1 ^{8,9}
(Address Controlled, $\text{CS}\backslash = \text{OE}\backslash = V_{\text{IL}}$, $\text{WE}\backslash = V_{\text{IH}}$)



READ CYCLE NO. 2 ^{7,8,10}
($\text{WE}\backslash = V_{\text{IH}}$)



**WRITE CYCLE NO. 1 ¹²
(Chip Enabled Controlled)****WRITE CYCLE NO. 2 ^{12, 13}
(Write Enabled Controlled)**



WRITE CYCLE NO. 3 ^{7, 12, 14}
(Write Enabled Controlled)

