CM8870C/CM8871C/CM8872C

Microcircuits

CMOS DTMF Integrated Receivers

FEATURES

- Full DTMF receiver
- Less than 35 mW power consumption
- Industrial temperature range
- Uses quartz crystal or ceramic resonators
- Adjustable acquisition and release times
- 18-pin DIP, 18-pin SOIC, 20 pin PLCC
- CM8870C
  - — Power down mode
  - — Inhibit mode
- CM8871C
  - — Power down mode
  - — Buffered oscillator output (OSC 3) to drive other devices
- CM8872C
  - — Inhibit mode
  - — Buffered oscillator output (OSC 3) to drive other devices

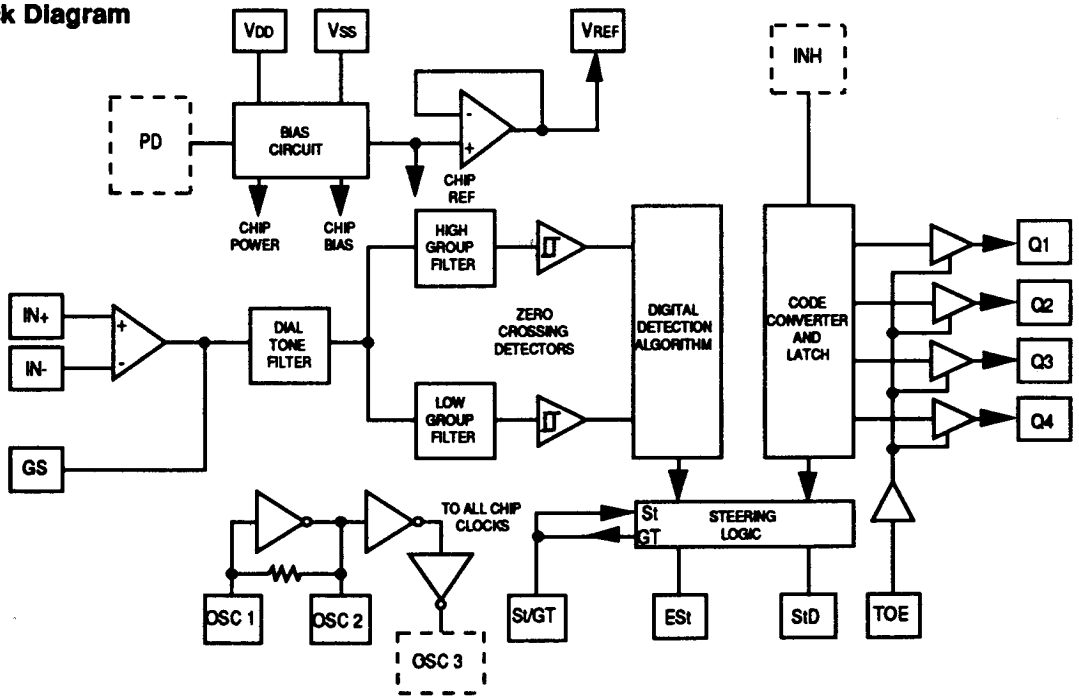
GENERAL DESCRIPTION

The CMD CM8870 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM8870 decoder uses digital counting techniques for the detection and decoding of all 16DTMF tone pairs into a 4-bit code. The CM8870 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal or ceramic resonator as an external component.

APPLICATIONS

- PABX
- Central office
- Mobile radio
- Remote control
- Remote data entry
- Call limiting
- Telephone answering systems
- Paging systems

Block Diagram



Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Power Supply Voltage (V_{DD}-V_{SS})	V_{DD}	6.0V Max
Voltage on any Pin	Vdc	V_{SS}-0.3, V_{DD}+0.3
Current on any Pin	I_{DD}	10 mA Max
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	TS	-65°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ±5%, T_A = -40°C to +85°C unless otherwise noted.

Parameter		Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltage		V_{DD}	4.75		5.25	V	
Operating Supply Current		I_{DD}		3.0	7.0	mA	
Standby Supply Current		I_{DDQ}			100	µA	PD=V_{DD}
Power Consumption		P_O		15	35	mW	f=3.579 MHz; V_{DD}=5.0V
Low Level Input Voltage		V_{IL}			1.5	V	V_{DD}=5.0V
High Level Input Voltage		V_{IH}	3.5			V	V_{DD}=5.0V
Input Leakage Current		I_{IH}/I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD} (Note 11)
Pull Up (Source) Current on TOE		I_{SO}		6.5	20	µA	TOE=0V, V_{DD}=5.0V
Input Impedance, (IN+, IN-)		R_{IN}	8	10		MΩ	@ 1KHz
Steering Threshold Voltage		Vtst	2.2		2.5	V	V_{DD}=5.0V
Low Level Output Voltage		V_{OL}			0.03	V	V_{DD}=5.0V, No Load
High Level Output Voltage		V_{OH}	4.97			V	V_{DD}=5.0V, No Load
Output Low (Sink) Current		I_{OL}	1.0	2.5		mA	V_{OUT}=0.4V
Output High (Source) Current		I_{OH}	0.4	0.8		mA	V_{OUT}=4.6V
Output Voltage	V_{REF}	V_{REF}	2.4		2.7	V	V_{DD}=5.0V, No Load
Output Resistance	V_{REF}	R_{OR}		10		KΩ	

Operating Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ±5%, T_A = -40°C to +85°C unless otherwise noted.
Gain Setting Amplifier

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current	I_{IN}			±100	nA	V_{SS} < V_{IN} < V_{DD}
Input Resistance	R_{IN}	10			MΩ	
Input Offset Voltage	V_{OS}			±25	mV	
Power Supply Rejection	PSRR	50			dB	1KHz (Note 12)
Common Mode Rejection	CMRR	40			dB	-3.0V < V_{IN} < 3.0V
DC Open Loop Voltage Gain	A_{VOL}	32			dB	
Open Loop Unity Gain Bandwidth	fc	0.3			MHz	
Output Voltage Swing	V_O	4.0			Vp-p	R_L ≥ 100KΩ to V_{SS}
Tolerable Capacitive Load (GS)	C_L			100	pF	
Tolerable Resistive Load (GS)	R_L			50	KΩ	
Common Mode Range	V_{cm}	2.5			Vp-p	No Load

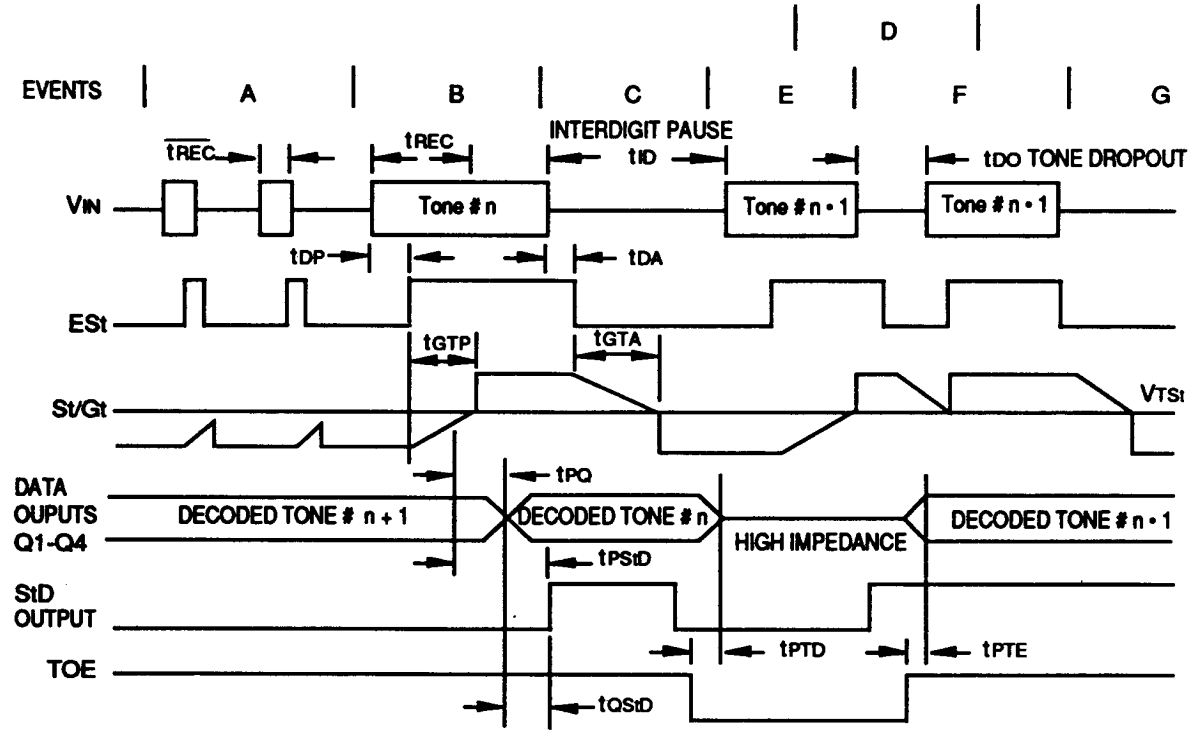
AC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ±5%, T_A = -40°C to +85°C, f_{CLK} = 3.579545 MHz using test circuit (Fig. 1) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Valid Input Signal Levels		-29		+1	dBm	1,2,3,4,5,8
(each tone of composite signal)		27.5		869	mV_{RMS}	
Positive Twist Accept				10	dB	2,3,4,8
Negative Twist Accept				10	dB	
Freq. Deviation Accept Limit				1.5%±2 Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit		±3.5%			Nom.	2,3,5
Third Tone Tolerance			-16		dB	2,3,4,5,8,9,13,14
Noise Tolerance			-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance			+22		dB	2,3,4,5,7,8,9
Tone Present Detection Time	t_{DP}	5	8	14	mS	Refer to
Tone Absent Detection Time	t_{DA}	0.5	3	8.5	mS	Timing Diagram
Min. Tone Duration Accept	t_{REC}			40	mS	(User Adjustable)
Max. Tone Duration Reject	t_{REC}	20			mS	Times shown are
Min. Interdigit Pause Accept	t_{ID}			40	mS	obtained with
Max. Interdigit Pause Reject	t_{DO}	20			mS	circuit in Fig. 1
Propagation Delay (St to Q)	t_{PQ}		6	11	µS	TOE = V_{DD}
Propagation Delay (St to StD)	t_{PStD}		9	16	µS	
Output Data Set Up (Q to StD)	t_{QStD}		3.4		µS	
Propagation Delay (TOE to Q) Enable	t_{PTE}		50		nS	R_L = 10KΩ
Propagation Delay (TOE to Q) Disable	t_{PTD}		300		nS	C_L = 50pF
Crystal/Clock Frequency	f_{CLK}	3.5759	3.5795	3.5831	MHz	
Clock Output (OSC 2) Capacitive Load	C_{LO}			30	pF	

Notes:

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias V_{REF}.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.

Timing Diagram



Explanation of Events

A) Tone bursts detected, tone duration invalid, outputs not updated.

B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.

C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

D) Outputs switched to high impedance state.

E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

VIN	DTMF composite input signal.
ESt	Early Steering Output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1-Q4	4-bit decoded tone output.
StD	Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE	Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
$\overline{tREC}$	Maximum DTMF signal duration not detected as valid.
tREC	Minimum DTMF signal duration required for valid recognition.
tID	Minimum time between valid DTMF signals.
tDO	Maximum allowable drop-out during valid DTMF signal.
tDP	Time to detect the presence of valid DTMF signals.
tDA	Time to detect the absence of valid DTMF signals.
tGTP	Guard time, tone present.
tGTA	Guard time, tone absent.

Functional Description

The CMD CM8870 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC or 20-pin PLCC package configuration. The CM8870's internal architecture consists of a bandsplit filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The CM8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives Vc to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \simeq 0.67\ RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the CM8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and V_{REF} biasing the input at $^1/_2 V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

Clock Circuit

The internal clock circuit is completed with the addition of a standard color burst crystal or ceramic resonator having a resonant frequency of 3.579545 MHz. The CM8871C and CM8872C have a buffered oscillator output (OSC3) that can be used to drive clock inputs of other devices such as a microprocessor or other CM887X's as shown in Figure 7. The CM8870C has no OSC3 pin (except for the PLCC package version), however multiple CM8870C's can be connected as shown in Figure 8 such that only one crystal or resonator is required.

Pin Function Table

Name	Description	
IN+ IN-	Non-inverting input Inverting input	Connections to the front-end differential amplifier
GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.	
VREF	Reference voltage output (nominally VDD/2). May be used to bias the inputs at mid-rail.	
INH	Inhibits detection of tones representing keys A,B,C,D.	
OSC 3	Digital buffered oscillator output.	
PD	Power down	Logic high powers down the device and inhibits the oscillator
OSC 1 OSC 2	Clock input Clock output	3.579545 MHz crystal connected between these pins completes internal oscillator.
VSS	Negative power supply (Normally connected to 0V).	
TOE	Three-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up.	
Q1 Q2 Q3 Q4	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.)	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below VTSt.	
ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
St/GT	Steering input/guard time output (bidirectional). A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Fig. 2.)	
VDD	Positive power supply	

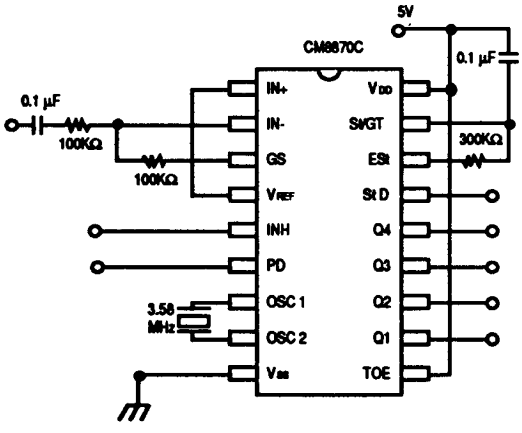


Figure 1. Single Ended Input Configuration

FLOW	FHIGH	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = Logic Low, H = Logic High, Z = High Impedance

Figure 2. Functional Decode Table

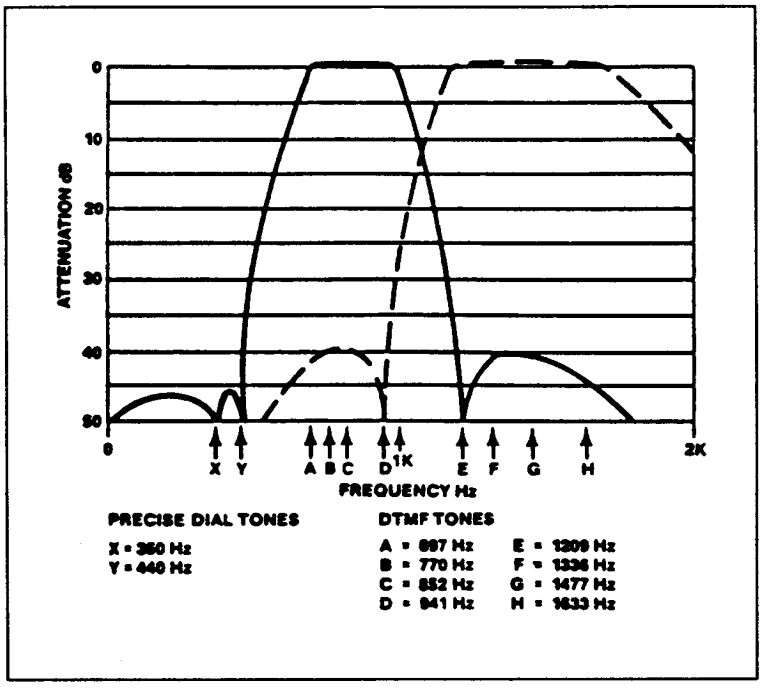


Figure 3. Typical Filter Characteristic

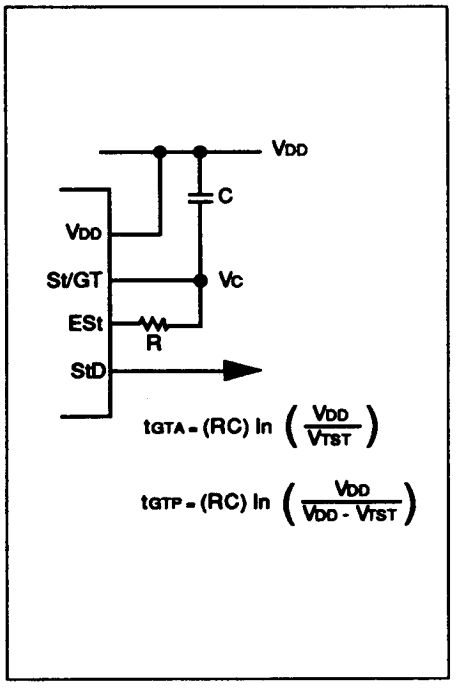


Figure 4. Basic Steering Circuit

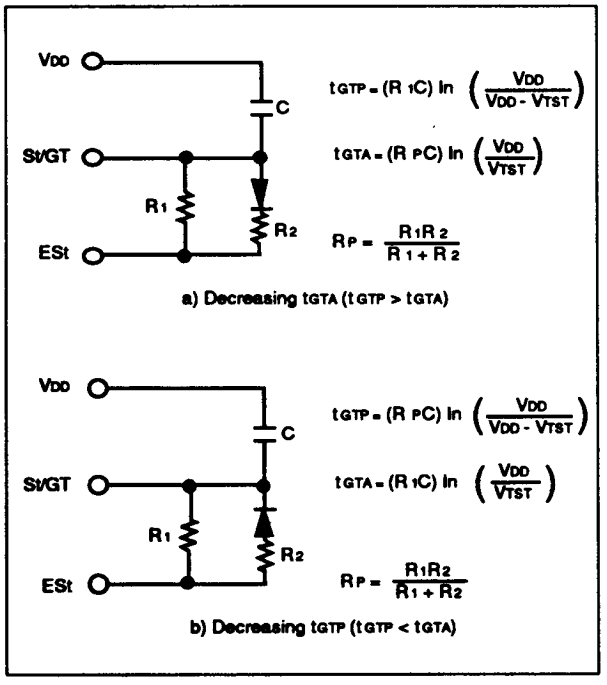


Figure 5. Guard Time Adjustment

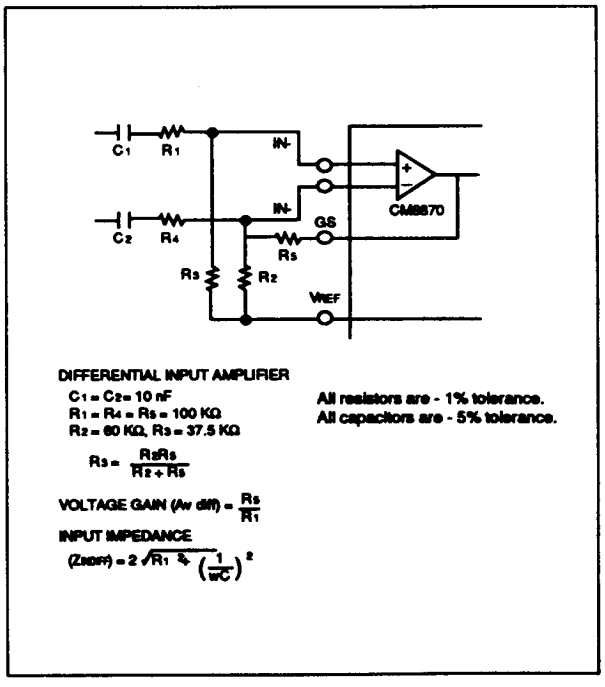


Figure 6. Differential Input Configuration

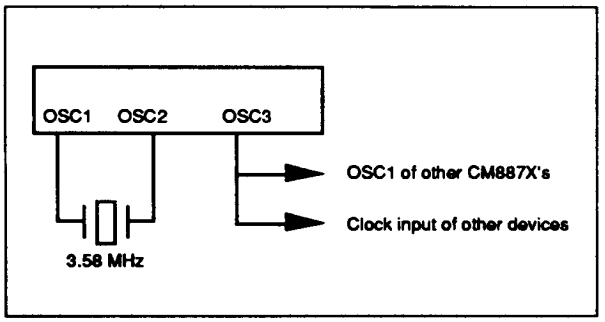


Figure 7. CM8871C/CM8872C Crystal Connection

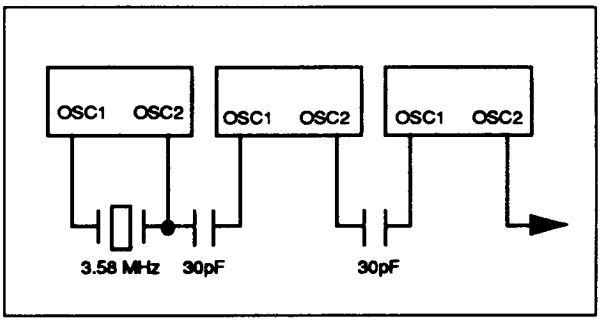
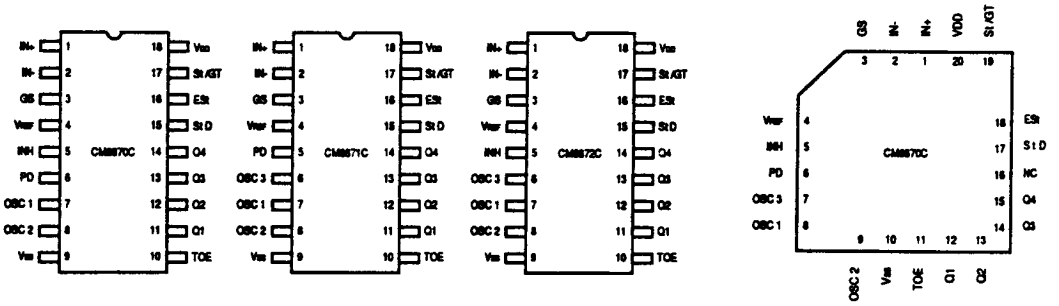


Figure 8. CM8870C Crystal Connection

Pin Configuration



Ordering Information

CM8870C D I

Product Identification Number

Package

P - Plastic E - Leaded Chip Carrier S - SOIC
C - Ceramic L - Leadless Chip Carrier
D - Cerdip X - Dice

Temperature/Processing

None - 0°C to +70°C, ±5% P.S. Tol.
I - -40°C to +85°C, ±5% P.S. Tol.