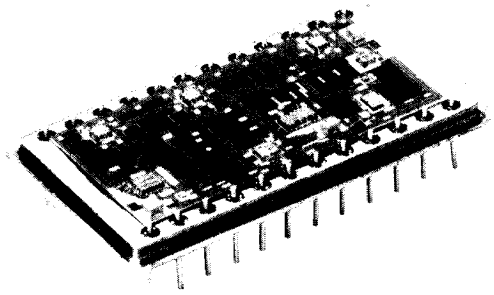
12 BIT HYBRID D/A CONVERTER
Input Register With Strobe; 5μs Voltage Settling Time



DESCRIPTION

The key feature of the DAC-SL D/A converter is the input register which can be used to store the digital input. The DAC-SL is complete with an internal reference, feedback resistors, and an output amplifier included in a hermetically sealed 24 pin double DIP metal case. The input is TTL compatible and voltage ranges are pin programmable. An external reference can be used so that the output can track a system reference.

APPLICATIONS

The DAC-SL is used in applications which can take advantage of its input register and relatively fast settling time. It is a rugged, high reliability device; standard processing is based on MIL-STD-883 except for burn-in, which is an option. Applications areas include medical instrumentation, CRT displays, and avionics systems. The DAC-SL can be used in remotely located and hard to access equipment because of its small size and high MTBF.

FEATURES

- *STROBED REGISTER STORES DIGITAL INPUT*
- *CODING:*
  Complementary Binary
  Complementary Offset Binary
- *VOLTAGE RANGES:*
  ±5V, ±10V, 0 to +10V
- *LINEARITY ERROR:*
  ±0.0125% F.S.R.

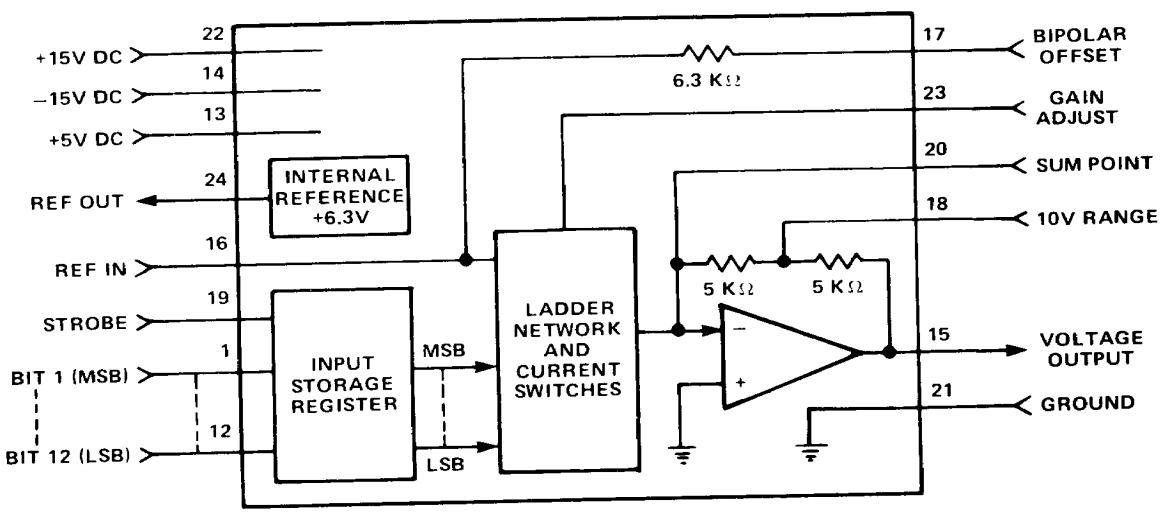


FIGURE 1. DAC-SL BLOCK DIAGRAM

DAC-SL SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages.

PARAMETER	UNITS	VALUE DAC-SL-11	DAC-SL-12
RESOLUTION	Bits	12	12
ACCURACY (USING INTERNAL REFERENCE)			
Linearity Error	% F.S. Range	±0.025 max	±0.0125 max
Linearity Tempco	ppm F.S.R./°C	±1.5 typ; ±3 max	±1.0 typ; ±2 max
Gain Error*	% F.S. Range	±0.4%	±0.2%
Gain Tempco	ppm F.S.R./°C	±20 typ; ±40 max	±15 typ; ±30 max
Offset Error*	% F.S. Range	±0.1 max	±0.05 max
Offset Tempco	ppm F.S.R./°C	±5 typ; ±8 max	±3 typ; ±5 max
Differential Linearity Error	LSB	±1.0 typ; ±2 max	±½ typ; ±1 max
Monotonic to	Bits	11	12
*Gain and Offset errors can be trimmed to zero.			
DYNAMIC CHARACTERISTICS			
Update Rate	MHz	3 max	
Settling Time to 0.01% F.S.R.			
F.S. Change on ±10V Range	µs	5 typ; 10 max	
F.S. Change on ±5V or 0 to +5V Ranges	µs	3 typ; 6 max	
LSB Change, All Ranges	µs	1.5 typ; 3 max	
Slew Rate	V/µs	15 typ; 10 min	
OUTPUT			
Voltage Ranges	V	±5, ±10, 0 to +10	
Max Current	mA	10 typ; 5 min	
DC Input Impedance	Ω	0.1 max	
DIGITAL INPUT (TTL COMPATIBLE)			
Input Voltage Levels	V	Logic "0": 0 to +0.8 Logic "1": +2 to +5.5	
Max Voltage Without Damage	V	7	
12 Parallel Data Bits			
Pulse Shape		Positive true pulse, 20 ns min, must remain valid until strobe returns to logic high	
Coding		Unipolar: Complementary Binary Bipolar: Complementary Offset Binary Also Complementary Two's Complement if the MSB Complement is provided.	
Loading		Logic "0": −400µA at 0.4V Logic "1": +20µA at 2.7V	
Strobe for Input Register			
Pulse Shape		Negative pulse, 20 ns min, leading edge simultaneous with or follows leading edge of parallel bits. Logic "0" = track digital input Logic "1" = hold data bits	
Loading		Logic "0": −720µA at 0.4V Logic "1": +40µA at 2.7V	
REFERENCE			
Internal Reference			
Voltage	V	6.3 ± 0.3	
Voltage Drift	ppm/°C	20 max	
Current Output	mA	0.1 max	
Output Impedance	Ω	20	
Reference Input			
Voltage	V	+6.3 ± 5%	
Current Requirement	mA	1.2	
POWER SUPPLIES			
Voltage	V	+15 ± 3%	−15 ± 3%
Max Voltage Without Damage	V	+18	−18
Current	mA	15 typ 25 max	5 typ 10 max
Power Supply Rejection Ratio	% F.S.R./% P.S.	.02 typ .05 max	.002 typ .01 max
Power Consumption	W	0.45 typ; 0.75 max	
TEMPERATURE RANGES (AMBIENT)			
Operating −1 Option	°C	−55 to +125	
Storage	°C	−65 to +125	
PHYSICAL CHARACTERISTICS			
Size (24 Pin Double DIP)	inch	0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5 cm)	
Weight	oz	0.4 typ (11.3g)	

PARAMETER	UNITS	VALUE		
POWER SUPPLIES				
Voltage	V	+15 ± 3%	−15 ± 3%	+5 ± 3%
Max Voltage Without Damage	V	+18	−18	+7
Current	mA	15 typ 25 max	5 typ 10 max	30 typ 45 max
Power Supply Rejection Ratio	% F.S.R./% P.S.	.02 typ .05 max	.002 typ .01 max	

TECHNICAL INFORMATION

PIN CONNECTIONS AND VOLTAGE RANGES

In normal operation the following connections are made (see Figure 1, Block Diagram). The REFERENCE IN is tied to the REFERENCE OUT unless an external reference is used. The BIPOLAR OFFSET is tied to the SUM POINT for bipolar operation or to GND for unipolar operation. The load is connected between the VOLTAGE OUTPUT and GND. The SUM POINT should not be used as an output. On the ±10V range, the feedback is an internal connection, but on the ±5V and 0 to +10V ranges the feedback is connected externally between pin 15 and pin 18, the 10V RANGE. This feedback connection should be made as close to the load as possible to minimize the effects of line and contact impedance.

The bipolar and feedback connections which determine the voltage ranges are summarized in the following table:

VOLTAGE RANGE	BIPOLAR OFFSET CONNECTION	FEEDBACK CONNECTION
±5V	17 to 20	15 to 18
±10V	17 to 20	—
0 to +10V	17 to 21	15 to 18

CODING AND TRIM ADJUSTMENTS

Coding for the DAC-SL is shown in the bit weight table, Figure 2. The values for full scale voltage (F.S.) and 1 LSB to be used in the bit weight table are as follows:

RANGE	FULL SCALE (F.S.)	1 LSB
±5V	5.00000V	0.00244V
±10V	10.00000V	0.00488V
0 to +10V	10.00000V	0.00244V

The trim adjustment circuits shown in Figure 3 are optional. The gain and offset errors are trimmed at the factory to within the limits listed in the specifications table. If both errors are trimmed to zero, the over-all accuracy will be equal to the linearity. The 6.8 MΩ and 9 MΩ fixed resistors in Figure 3 should be located close to the converter pins to reduce noise, and the two potentiometers should have a tempco of not more than 100 ppm/°C.

To trim the offset, apply the all one's digital code, which corresponds to 0 volts output for the unipolar range, and to −F.S. for the bipolar ranges (see Figure 2). Adjust the offset potentiometer for the proper value for the output voltage.

After trimming the offset, apply the all zero's digital code to trim the gain. This code corresponds to +F.S. − 1 LSB, and the output should be adjusted to this value with the gain potentiometer.

ANALOG OUTPUT VOLTAGE		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12
+F.S. – 1 LSB	+F.S. – 1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+3/4 F.S.	+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. + 1 LSB	+ 1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. – 1 LSB	–1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
1/4 F.S.	–1/2 F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	–F.S. + 1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	–F.S.	1	1	1	1	1	1	1	1	1	1	1	1

Note: For Complementary Two's Complement coding, the bit values are identical to those for Complementary Offset Binary coding in the table, except that the MSB is reversed (MSB bits "1" become "0", and bits "0" become "1").

FIGURE 2. BIT WEIGHT TABLE

STROBE TIMING

A timing diagram for the input register STROBE is shown in Figure 4. The data bits must remain valid for at least 20 ns. The leading edge of the strobe pulse can be simultaneous with the leading edge of the data pulse, or it can be delayed. The data bits must remain valid until the strobe pulse is complete. It is possible for the data bits and strobe to begin and end together in phase.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors should be used to improve noise rejection. Connect two capacitors to ground at each of the three power supply input pins, as close to the converter as possible. One capacitor should be 1 – 10μF tantalum or electrolytic; the other should be 0.01μF ceramic for high frequency bypassing.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify preburn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 2,200,000 hours, Ground Fixed, at 25°C.

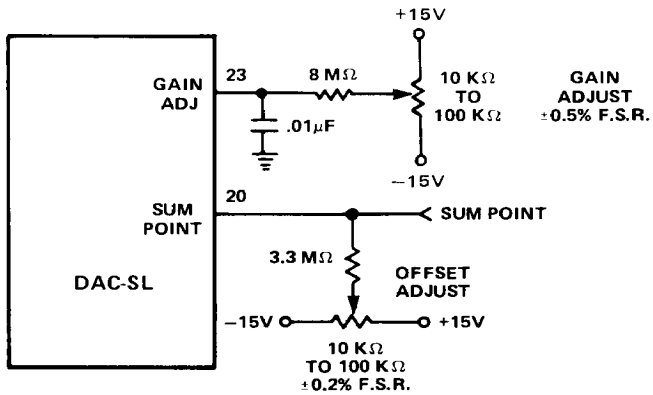


FIGURE 3. TRIM ADJUSTMENT CIRCUITS

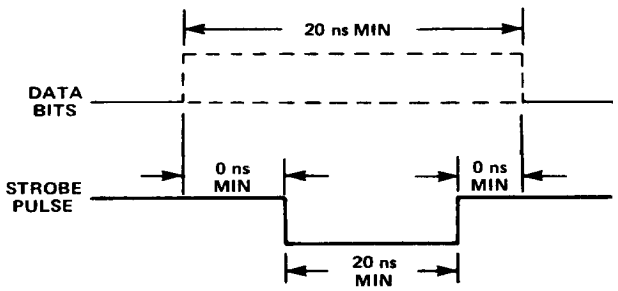
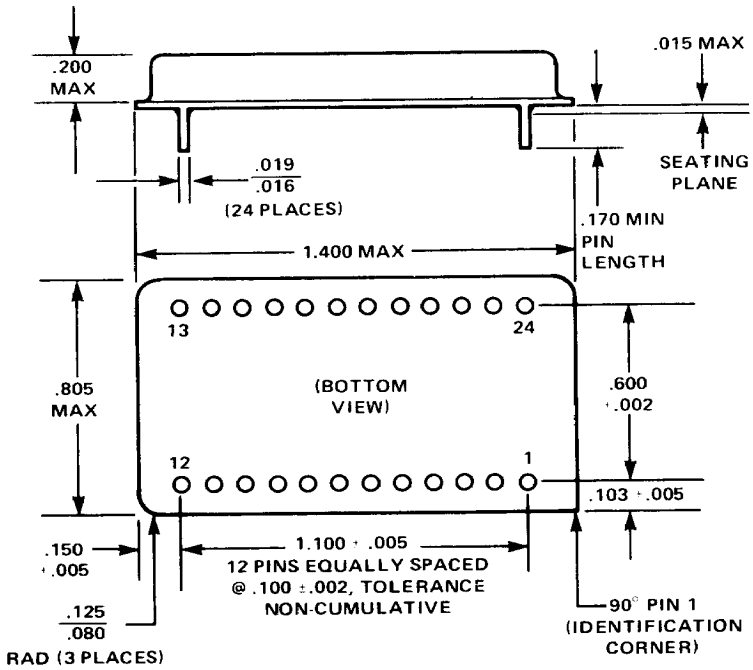


FIGURE 4. STROBE TIMING DIAGRAM

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches.
2. Load identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 1 (MSB)	13	+5V DC
2	Bit 2	14	−15V DC
3	Bit 3	15	Voltage Out
4	Bit 4	16	Ref In
5	Bit 5	17	Bipolar Offset
6	Bit 6	18	10V Range
7	Bit 7	19	Strobe
8	Bit 8	20	Sum Point
9	Bit 9	21	Ground
10	Bit 10	22	+15V DC
11	Bit 11	23	Gain Adjust
12	Bit 12 (LSB)	24	Ref Out

ORDERING INFORMATION

DAC-SL – 12 – 1 – 883B

- 883B: MIL-STD-883 Processing: 883B = Conforms to MIL-STD-883B, DDC procedures; Blank = Same, except pre burn in test and burn in are omitted.
- 1: Operating Temperature Range (Ambient): −1 = −55°C to +125°C
- 12: Linearity: 12 = 12 bits (±0.0125%); 11 = 11 bits (±0.025%)