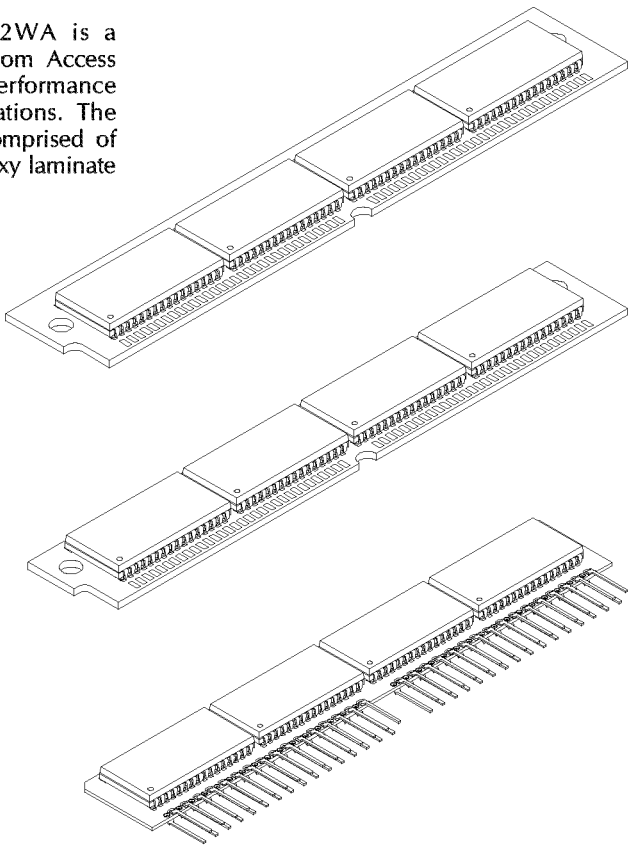
DENSE-PAC
MICROSYSTEMS

8 Megabit CMOS SRAM

DPS256X32L/DPS256X32W/DPS256X32WA

DESCRIPTION:

The DPS256X32L/DPS256X32W/DPS256X32WA is a 256K x 32 high density, high-speed Static Random Access Memory (SRAM) module, intended for high performance computers and digital signal processing applications. The DPS256X32L/DPS256X32W/DPS256X32WA is comprised of eight 256K x 4 devices surface mounted on an epoxy laminate substrate.



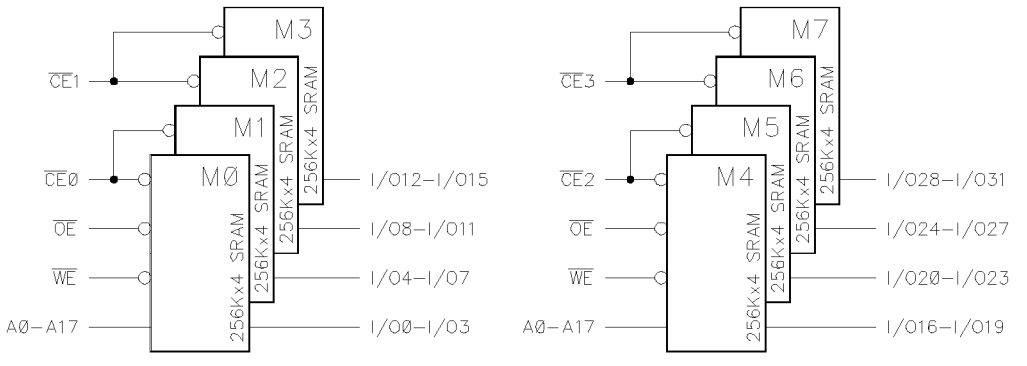
FEATURES:

- 256K X 32, 512K x 16 or 1M x 8 Configuration
- High Speed: 12*, 15, 17, 20, 25, 35ns
- All Inputs and Outputs TTL Compatible
- Fully Static Operation;
  No Clock or Refresh Required
- Equal Read Access and Write Cycle Time
- Packages: 64-Pin ZIP
  64-Pin SIMM
  64-Pin Angled SIMM

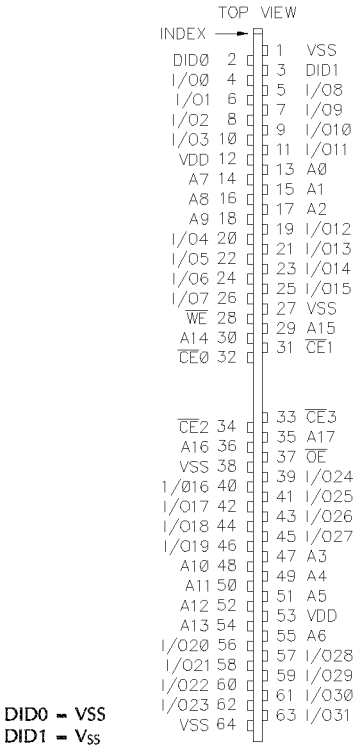
* Contact factory for availability.

PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
DID0 / DID1	Density I.D. Pins
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



DID0 = VSS
DID1 = V_{SS}

TRUTH TABLE					
Mode	$\overline{CE}$n	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

RECOMMENDED OPERATING RANGE [2]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[3]		0.8	V
T_A	Operating Temp.	0	+25	+70	°C

ABSOLUTE MAXIMUM RATINGS [4]			
Symbol	Parameter	Max.	Unit
T_{STC}	Storage Temperature	-40 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to + 85	°C
V_{DD}	Supply Voltage [2]	-0.5 to + 7.0	V
V_{ID}	Input/Output Voltage [2]	-0.5 to V_{DD} +0.5	V

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IH}	HIGH Voltage	I_{OH} = -4.0mA	2.4	-	V
V_{IL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

CAPACITANCE [5]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	50	pF	V_{IN} = 0V
C_{CE}	Chip Enable	25		
C_{WE}	Write Enable	60		
C_{OE}	Output Enable	60		
$C_{I/O}$	Data Input/Output	20		

DC OPERATING CHARACTERISTICS: Over operating ranges						
Symbol	Characteristics	Test Conditions		COMMERCIAL Min.	COMMERCIAL Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-40	+40	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$n = V_{IH}		-10	+10	µA
I_{CC}	Operating Supply Current	$\overline{CE}$n = V_{IL}, f = max., I_{OUT} = 0mA	15ns-35ns		1440	mA
			12ns*		1760	
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE}$n $\geq V_{DD}$ -0.2, f = 0mHz			80	mA
I_{SB2}	Standby Current	$\overline{CE}$n = V_{IH}, f = max.			480	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA		2.4		V

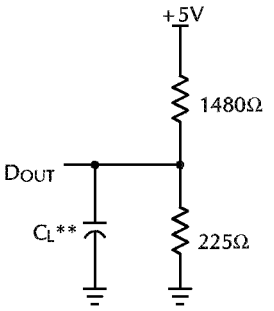
* Contact factory for availability.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C_L	Parameters Measured
1	30pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OW}, t_{OLZ} and t_{OHZ}
2	5pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OW}

Figure 1. Output Load
** Including Probe and Jig Capacitance.

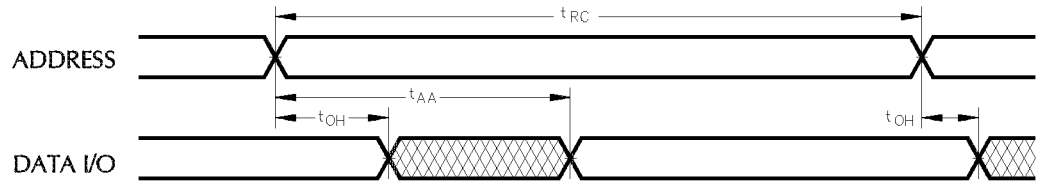


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges														
No.	Symbol	Parameter	12ns†		15ns		17ns		20ns		25ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	12		15		17		20		25		35		ns
2	t_{AA}	Address Access Time		12		15		17		20		25		35	ns
3	t_{ACS}	Chip Enable Access Time		12		15		17		20		25		35	ns
4	t_{CLZ}	Chip Enable to Output in LOW-Z [5, 7]	3		3		5		5		5		5		ns
5	t_{OE}	Output Enable to Output Valid		6		7		8		10		13		15	ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [5, 7]	0		0		0		0		0		0		ns
7	t_{CHZ}	Chip Enable to Output in HIGH-Z [5, 7]	0	6	0	7	0	8	0	12	0	15	0	15	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z [5, 7]	0	6	0	7	0	7	0	10	0	10	0	20	ns
9	t_{OH}	Output Hold from Address Change	3		3		5		5		5		5		ns

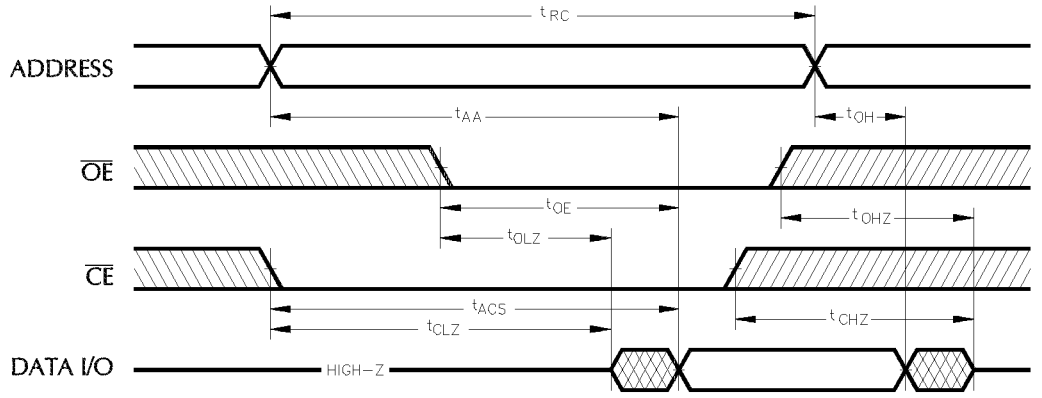
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8]															
No.	Symbol	Parameter	12ns†		15ns		17ns		20ns		25ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	12		15		17		20		25		35		ns
12	t_{CW}	Chip Enable to End of Write	10		12		14		17		20		30		ns
11	t_{AW}	Address Valid to End of Write	10		12		14		17		20		30		ns
13	t_{AS}	Address Set-up Time ‡	0		0		0		0		0		0		ns
14	t_{WP}	Write Pulse Width	10		11		14		16		20		30		ns
15	t_{WR}	Write Recovery Time	0		0		2		3		3		3		ns
16	t_{WHZ}	Write Enable to Output in HIGH-Z [5, 7]	0	6	0	7	0	7	0	8	0	10	0	15	ns
17	t_{DW}	Data to Write Time Overlap	6		7		9		12		15		20		ns
18	t_{DH}	Data Hold Time from Write Time	0		0		0		0		0		0		ns
19	t_{OW}	Output Active from End of Write [5, 7]	0		0		5		5		5		5		ns

† Contact factory for availability.
‡ Valid for both Read and Write Cycles.

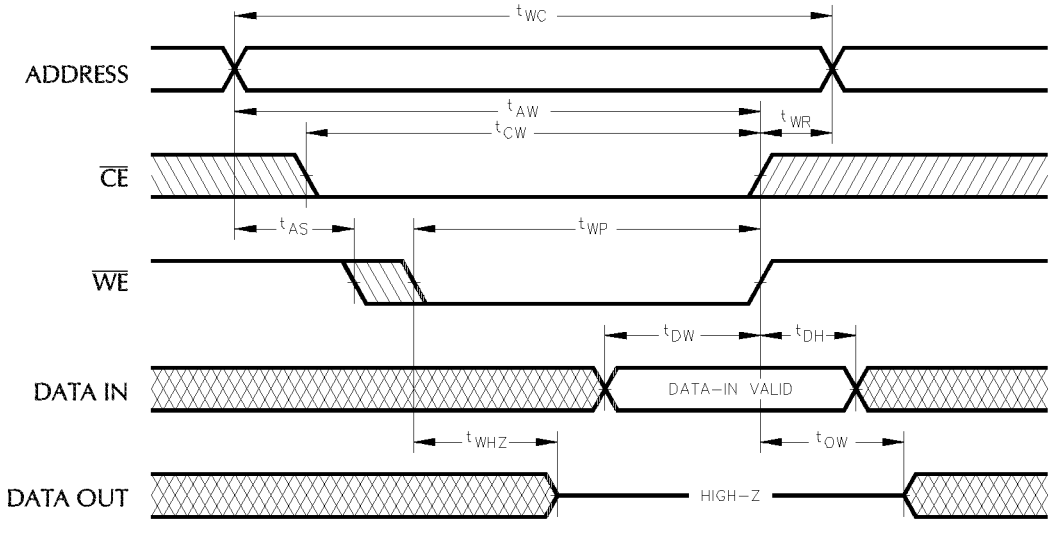
READ CYCLE 2: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



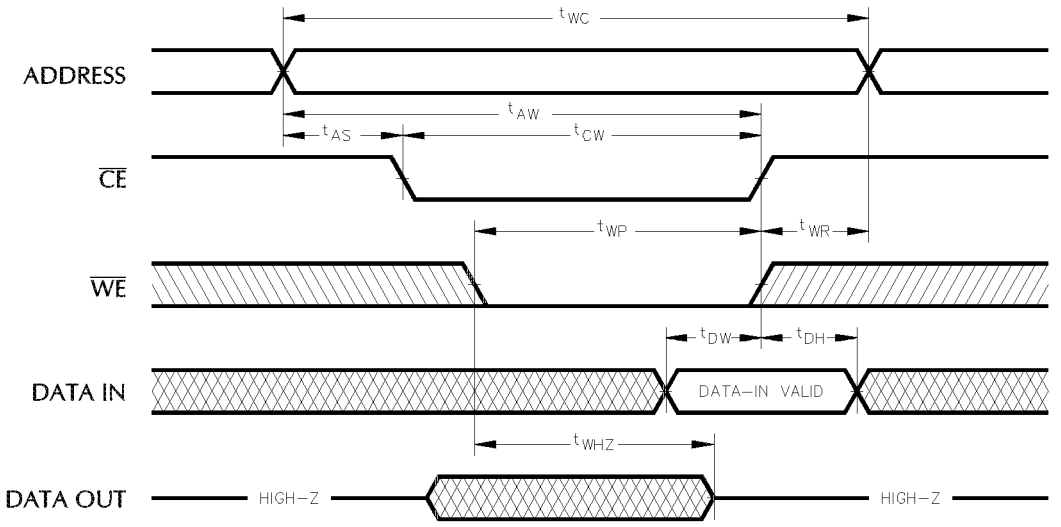
READ CYCLE 1: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. [8]



WRITE CYCLE 2: $\overline{CE}$ Controlled.



NOTES:

1. The DID0 and DID1 pins are used to identify memory density when other density versions of the JEDEC STD module can be installed in the same socket.
2. All voltages are with respect to V_{SS}.
3. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
4. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. This parameter is guaranteed and not 100% tested.
6. Transition is measured at the point of ± 500mV from steady state voltage.
7. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
8. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

ORDERING INFORMATION

DP S 256 X 32 X – XX C

PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | PACKAGE | SPEED | GRADE

GRADE:
- C COMMERCIAL 0°C to +70°C

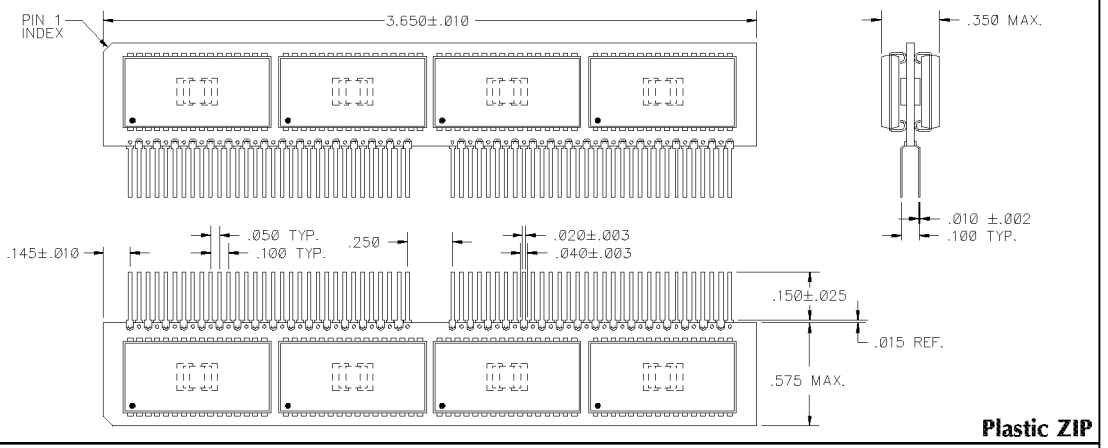
SPEED:
- 12* 12ns*
- 15 15ns
- 17 17ns
- 20 20ns
- 25 25ns
- 35 35ns

PACKAGE:
- L PLASTIC ZIP (LEADED)
- W PLASTIC SIMM (LEADLESS)
- WA ANGLED PLASTIC SIMM (LEADLESS)

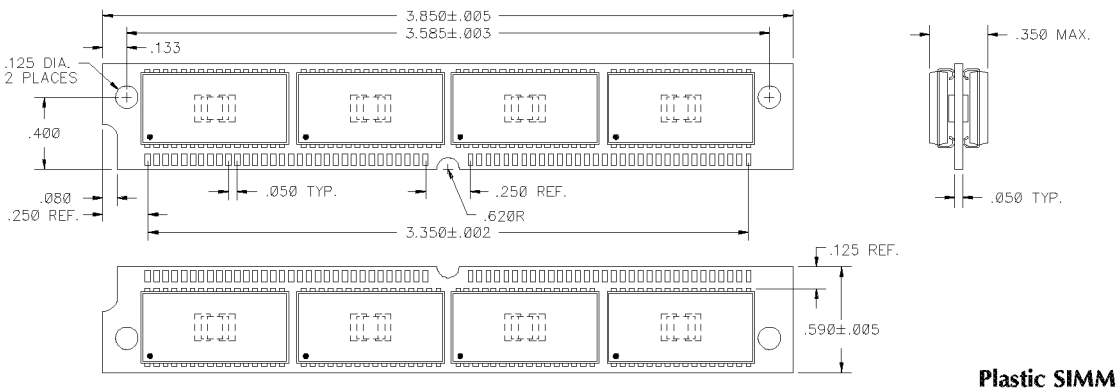
DESIG: MEMORY MODULE WITHOUT SUPPORT LOGIC

TYPE: CMOS SRAM

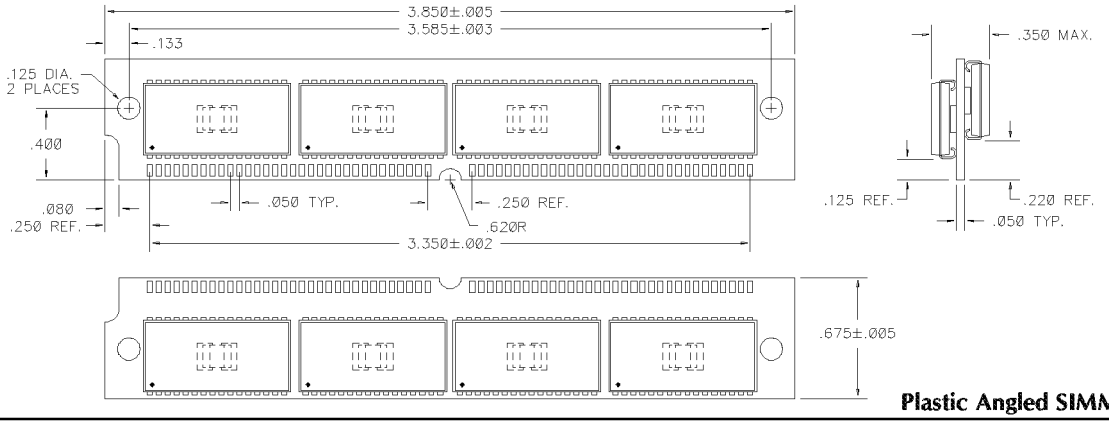
MECHANICAL DRAWINGS



Plastic ZIP



Plastic SIMM



Plastic Angled SIMM

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