HEWLETT® PACKARD

High Speed Silicon Bipolar 622 Mb/s Serial Data and Clock Recovery Circuit

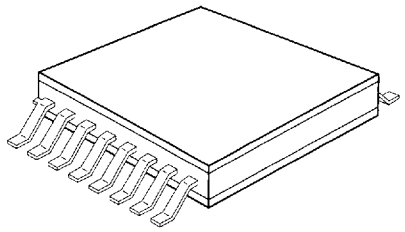
Technical Data

HDMP-2501

Features

- **Single Chip Clock Extraction and Data Retiming**
- **Designed for 622 Mb/s Applications**
- **Easy to Apply, Cost Effective**
- **Operational with Data Patterns Pseudorandom to 2^{23}-1**
- **Lock Time < 2.5 ms**
- **Low Jitter Generation < 1.7 Degrees at 622 Mb/s**
- **Auto Adjusting – No Board Level Adjustment Needed**
- **Autotracks Temperature and Voltage Changes**
- **0 to 65°C Case Temperature Range**
- **ECL Compatible I/O**
- **50 mV Minimum Signal Input Required**
- **Standard ECL -5.2V & -2.0V Power Supply**
- **Low Power Dissipation (1.4W)**
- **Hermetic Glass Metal Surface Mount Package**

HDMP-2501



Applications

- **Telecom and Datacom Switching Systems**
- **Computer Back Plane Interconnect**
- **Board to Board High Speed Data Links**

Description

The HDMP-2501 is a 622 Mb/s serial data and clock recovery circuit which is based on a Phase Locked Loop (PLL) approach for clock extraction. This chip includes a phase/frequency detector, integrator (external capacitor required), and a voltage controlled oscillator (VCO), see Figure 1. A self contained decision circuit automatically aligns the data relative to the recovered clock. Both recovered clock and retimed data outputs are available.

The digital phase detector generates a correction to the VCO ramp after each transition of the input serial data stream.

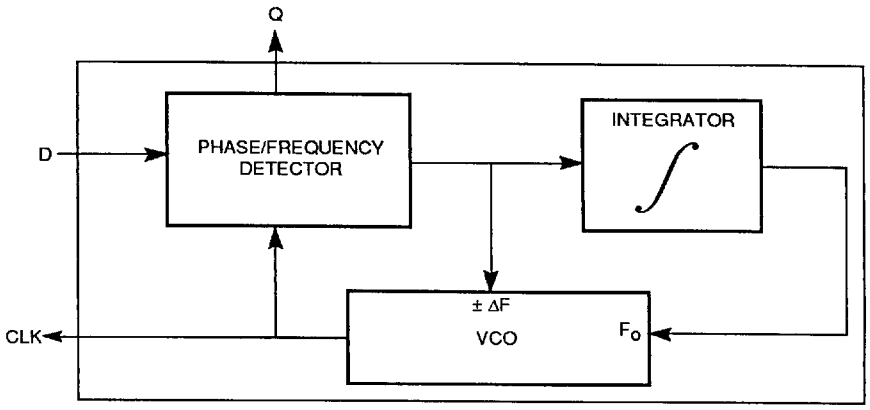
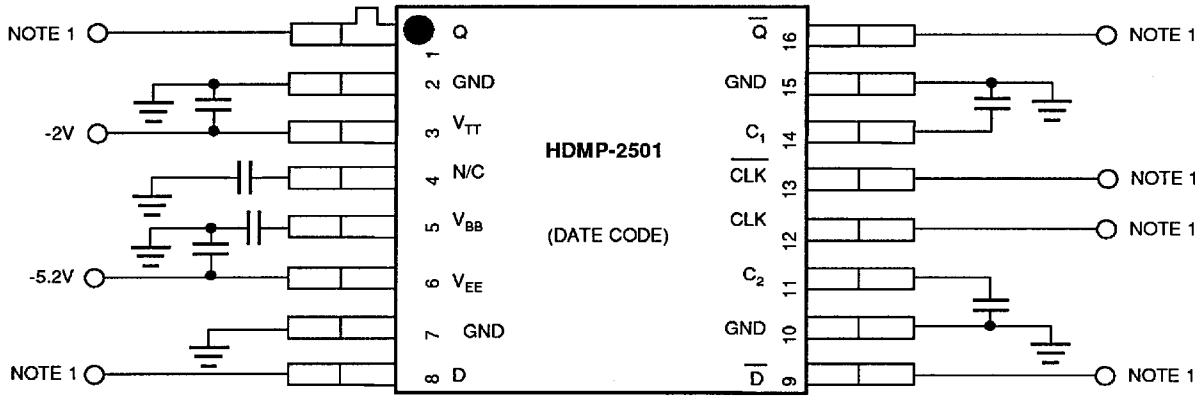


Figure 1. Functional Block Diagram

The design insures clock capture over the entire range of the VCO, and provides for fast lock-up and autotracking of the recovered clock over temperature and supply voltage changes. No external adjustment is required.

The PLL approach integrated in this design eliminates the temperature and phase variation conditions normally found with multiple device and diverse technology approaches such as surface acoustic wave devices.



NOTES:
1. PINS 1 AND 16 (Q AND $\overline{Q}$); 8 AND 9 (D AND $\overline{D}$); 12 AND 13 (CLK AND $\overline{CLK}$) MUST BE TERMINATED TO AC OR DC 50 Ω (SEE FIGURE 11).
2. CAPACITORS SHOWN ARE 0.1 µF CERAMIC CHIP TYPE AND ARE REQUIRED FOR ALL OPERATING CONDITIONS.

Figure 2. Package Connection

Table 1. HDMP-2501 Pin Connections Description

Label	Pin	Description
C_1	14	Charge pump capacitor connection. 0.1 µF typical, ground other end.
C_2	11	Charge pump capacitor connection. 0.1 µF typical, ground other end.
CLK	12	Retimed clock output AC or DC couple to 50 ohms, or DC couple to ECL.
$\overline{CLK}$	13	Retimed clock output (complimentary) AC or DC couple to 50 ohms, or DC couple to ECL.
D	8	Serial data input. ECL bias or AC couple with 0.1 µF.
$\overline{D}$	9	Serial data input (complimentary). ECL bias or AC couple with 0.1 µF
GND	2, 7, 10, 15	Ground
N/C	4	No connection to chip
Q	1	Retimed data output.
$\overline{Q}$	16	Retimed data output (compliment) AC or DC couple to 50 ohms, or DC couple to ECL.
V_{BB}	5	Internally generated bias reference voltage, typically -1.3 volts. Use bypass capacitor.
V_{EE}	6	Main power supply pin, typically -5.2 volts. Use bypass capacitor.
V_{TT}	3	Secondary power supply pin, typically -2.0 volts. Use bypass capacitor.

Absolute Maximum Ratings

T_C = 25°C, except as specified. Operation in excess of these may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{EE}	Supply Voltage	Volts	-6.0	
V_D	Data Input Voltage	Volts Pk to Pk		2.0
T_{op}	Case Operating Temperature	°C		+105
T_{stg}	Storage Temperature	°C	-60	+150
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)	°C		+300

Thermal Specifications

Symbol	Parameters	Units	Typical
θjc	Thermal Resistance (Die to Case)	°C/W	10
P_D	Power Dissipation at V_{EE} = -5.2V	Watts	1.4

DC Electrical Specifications

Symbol	Parameters	Units	Min	Typ.	Max.
V_{EE}	Supply Voltage	V	-5.46	-5.2	-4.94
I_{EE}	Supply Current	mA		230	
V_{TT}	Second Supply Voltage	V	-2.05	-2	-1.95
I_{TT}	Second Supply Current	mA		75	

AC Electrical Specifications

T_C = 25°C; V_{in} = 200 mV p-p @ 622 Mbp/s @ V_{EE} = -5.2V; V_{TT} = -2 V
Input data test sequence = PRBS @ 2^{23}-1; D and $\overline{D}$ are AC coupled (0.1 μF), 50Ω termination.
Integrating capacitors C_1 and C_2 are 0.1 μF (refer to Figure 2).

Symbol	Parameters	Units	Min.	Typ.
V_D	Minimum Data Input Voltage (pk - pk) (Ambiguity @ 10^{-7} BER)	mV		50
t_{acq}	Acquisition Lock Time	ms		2.3
t_r, t_f	Rise Time, Fall Time; Data and Clock See Figures 7 and 8	ps		200
J_g	Jitter Generation	ps (rms)		7.5
V_{CLK}	Recovered Clock Output (pk to pk)	V	0.6	0.7
V_Q	Output Voltage Swing (pk to pk) See Figure 7	V	0.6	0.7
VSWR	Data In and Out; Clock out	—		< 2:1

Theory of Operation

The retiming circuit is based on a PLL approach to timing extraction[1]. The functional block diagram is shown in Figure 1. A phase/frequency detector samples the incoming data, and generates an error signal which controls a dual input VCO. the VCO is realized as a ring oscillator in order to be integrated on the same chip.

The VCO frequency, F_O, is adjusted by feedback to a frequency approximately equal to the incoming data bit rate. The fine adjustment $\pm\Delta F$, is made by a bang-bang delay element as shown in Figure 3. The bang-bang element tracks the small variations of the incoming bit rate. The ring oscillator has a nominal delay of 800 ps with a typical usable range of ± 10%. The bang-bang fine control delay time is approximately 3 ps. The response time of the bang-bang element is about 700 ps for a full VCO update or much less than one clock cycle at 622 Mb/s.

The integrator (Figure 1) is achieved by a balanced charge-pump configuration with two off chip capacitors (pins 11 and 14).

[1]B. Lai and R. Walker, "A Monolithic 622 Mb/s Clock Extraction and Retiming Circuit", ISSCC91 Paper TPM 8.7.

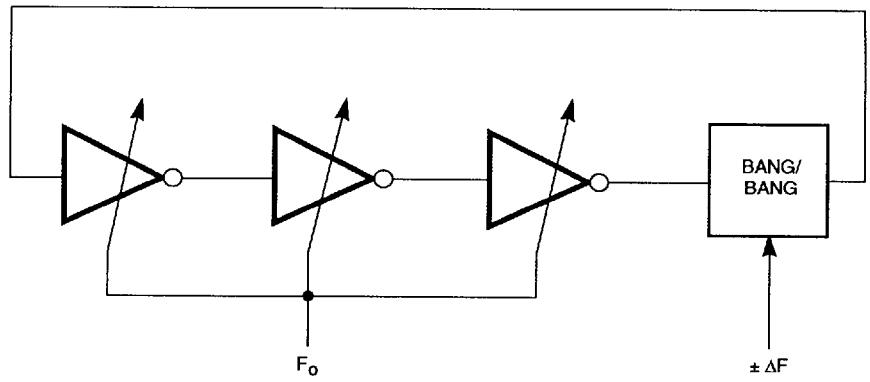
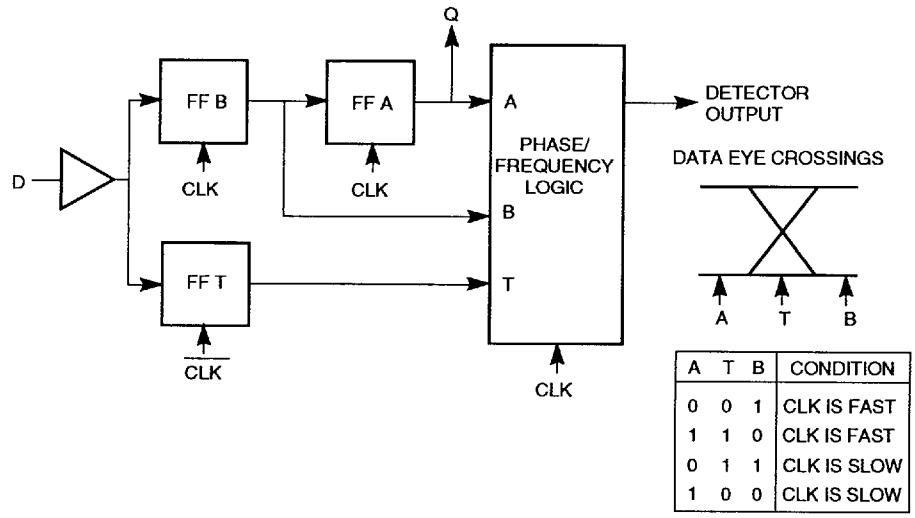


Figure 3. Ring Oscillator and Control Elements



A	T	B	CONDITION
0	0	1	CLK IS FAST
1	1	0	CLK IS FAST
0	1	1	CLK IS SLOW
1	0	0	CLK IS SLOW

Figure 4. Block Diagram of the Phase/Frequency Detector.

Phase/Frequency Detector

The phase/frequency detector is shown in Figure 4. In the sampling pattern of Figure 4, the input data is sampled at three points: the bit prior to the transition, in the vicinity of the transition, and the bit following the transition. At each transition encountered, the clock can be deduced as either fast or slow compared to the incoming data. This information is used to generate a pulse train which updates the integrator and drives the bang-bang delay element.

The phase tracking of clock to data behaves as shown in Figure 5. Each correction in the faster direction (clock phase increasing with respect to data phase) has slope $+\Delta F$, and each correction in the slower direction has slope $-\Delta F$. Over time, the VCO phase tracks the phase changes in the incoming data. Flip-flop A (Figure 4) samples at the center of the data eye and provides the decision circuit function.

Lock Capture

Initial lock acquisition behavior is highly complex and works best with high transition densities typical of pseudorandom bit patterns. Due to the phase frequency detector architecture, the acquisition behavior is different from a typical PLL.

Lock capture of repetitive data patterns becomes increasingly difficult as transition density decreases. This can cause lock acquisition times to be

significantly longer than expected or sub-harmonic false locks to occur.

The fact that false lock is weaker than true lock is essential to eliminating it. When both true and false phase locks occur, a slight displacement of the data phase relative to clock phase produces an error signal in the bang-bang detector which tends to restore it back to the original lock condition. This restoring force is represented at the integrating capacitor by a change in capacitor voltage which is in turn applied to the VCO to adjust the frequency. A simple idea to eliminate false lock is to connect a current source to the integrating capacitor (Figure 6). Its immediate effect is to ramp the capacitor voltage,

$$I_{CS} = \frac{dQ}{dt} = C\frac{dV}{dt},$$

which causes the VCO to sweep. If the capacitor charging rate is high enough to cancel out the "restoring force" current due to false lock, then false lock will be suppressed. However, the ramp current must not be so large it will suppress true lock. An estimate of true lock current can be obtained through acquisition lock time t_{acq}. For example, the HDMP-2501 with 0.1 µF integrating capacitors has a t_{acq} of approximately 2.3 mS. During this time the VCO control voltage changes about 1 Volt. Thus

$$I = C\frac{dV}{dt}(0.1\ \mu F)(\frac{1\ Volt}{2.3\ mS}) = 43\ \mu A$$

is an estimate of the ramp current.

A simple and inexpensive lock enhancement circuit is shown in Figure 7. The circuit consists of a very low frequency oscillator built from an inexpensive 555 timer chip, 3 resistors and 1 capacitor (plus a supply bypass capacitor). The time output is a 100 Hz TTL square wave applied via a large (15 kΩ) resistor to one side of the balanced HDMP-2501 integrator. Since the balanced integrator circuit uses differential pairs, the signal can be applied to only one side while the other side responds by symmetry.

To assist correct lock capture, the VCO can be forced to its center frequency by momentarily equalizing the two integration capacitor voltages (pins 11 and 14) as shown in Figure 6. The VCO then begins its lock capture from the center frequency which, by design, is close to the data frequency.

Input/Output Impedance Match

The input and output are closely matched to 50 ohms impedance. This allows easy interconnection to other circuits with minimum reflection of signals. The return loss performance is shown in Figures 10 and 11.

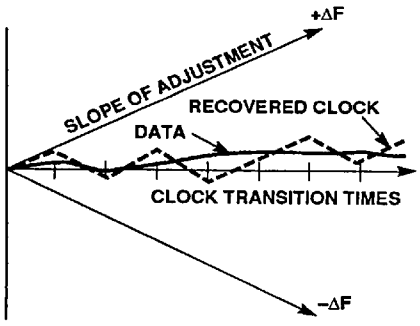


Figure 5. Clock Tracking of Data Phase.

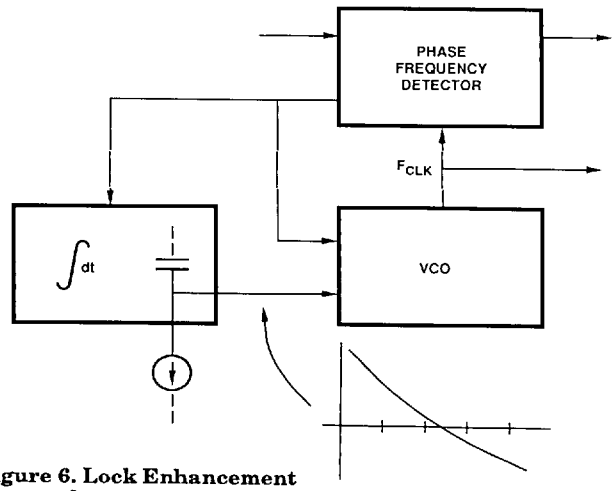


Figure 6. Lock Enhancement Approach.

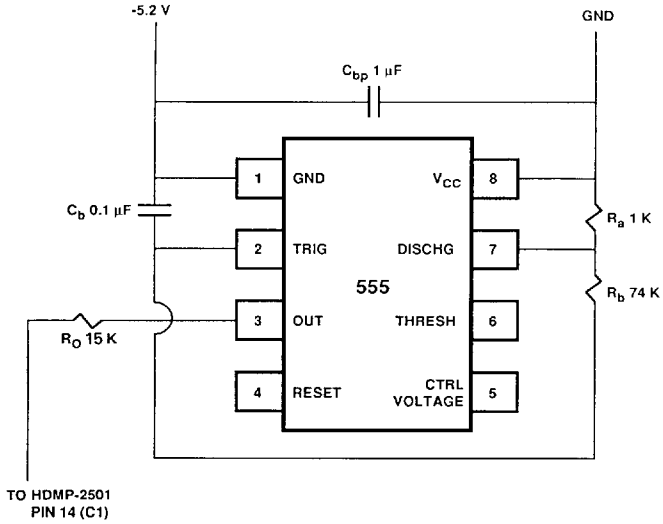


Figure 7. Practical Lock Enhancement Circuit.

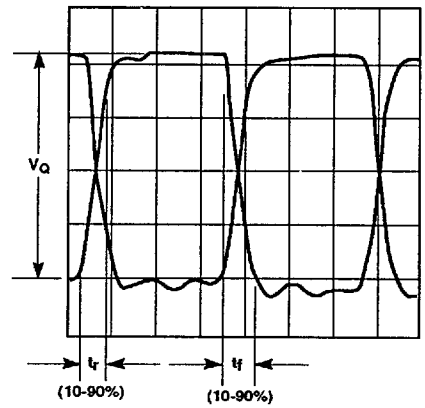


Figure 8. Typical Data Output Waveform.

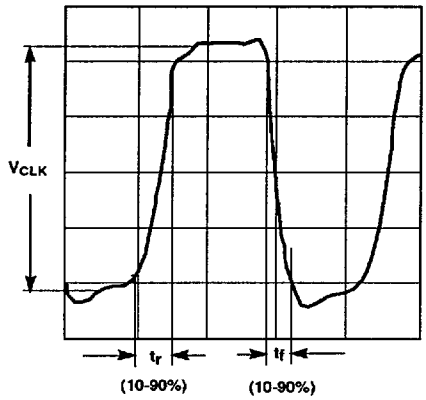


Figure 9. Typical Clock Output Waveform.

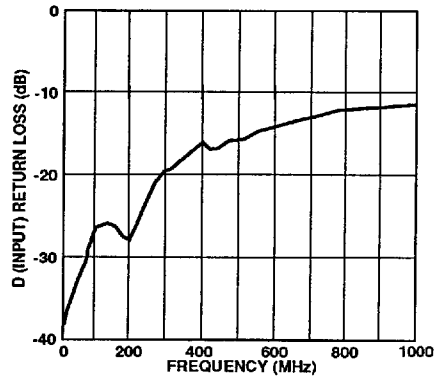


Figure 10. Typical Input Return Loss vs. Frequency.

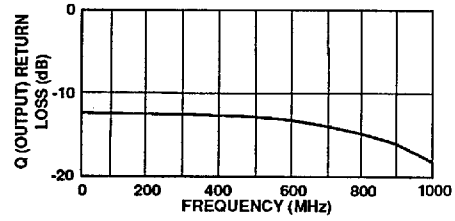


Figure 11. Typical Output Return Loss vs. Frequency.

Output Drive Level

The output driver is designed to deliver 0.8 V into 50 ohms, AC or DC coupled, as shown in Figures 12a and 12b.

The V_{OH} and V_{OL} levels of the driver are such that the peak-to-peak voltage is approximately 1.2 V unloaded centered around -1.3 V.

For driving ECL, the line can be terminated with a parallel combination of resistors as shown in Figure 12c. The equivalent termination of 50 Ω shrinks the peak-to-peak voltage down to approximately 0.8 V centered about -1.3 V. The output impedance of the driver is matched to 50 Ω. The amplitude can be increased with a larger termination resistance with minimal VSWR penalty. Nominal values for a 50 Ω interface are R_1 = 140 Ω, R_2 = 77 Ω.

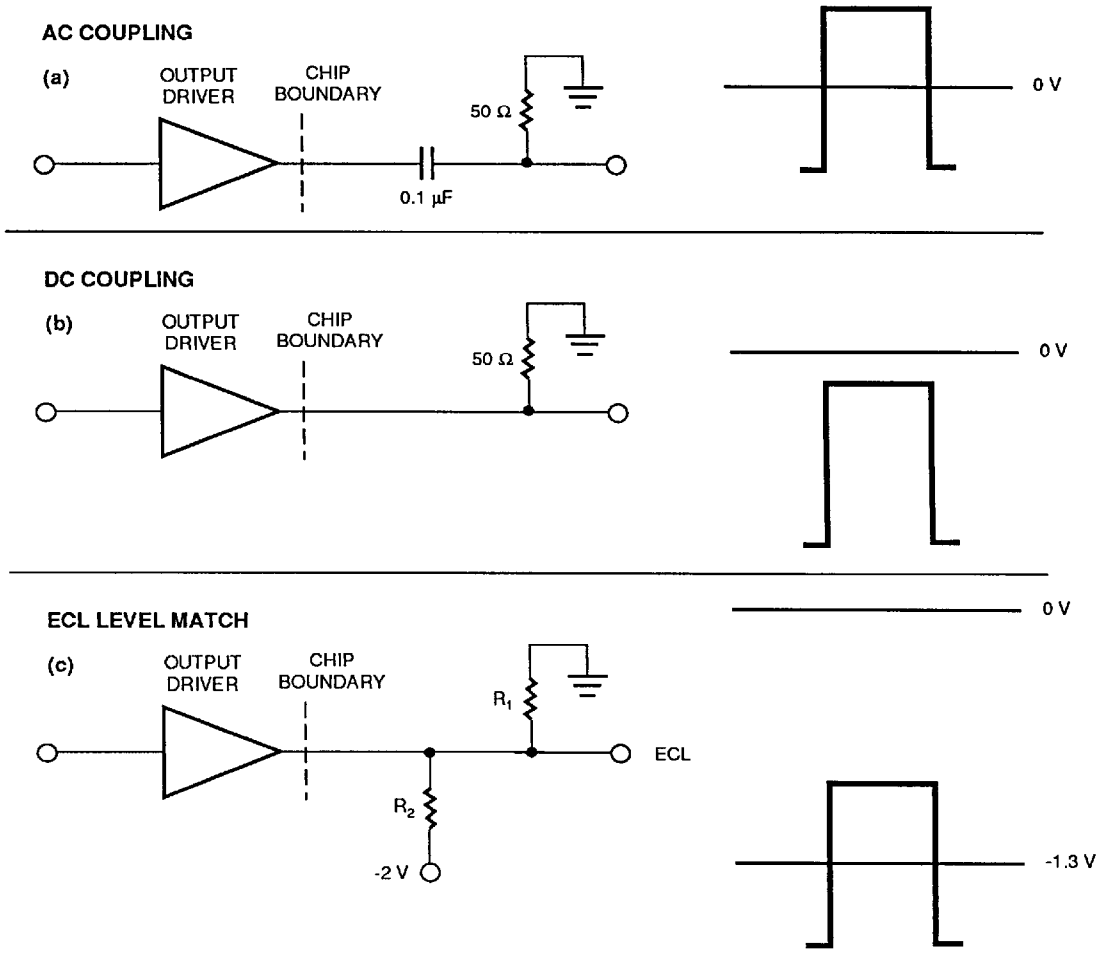


Figure 12. Output with Various Loading Conditions.

Performance vs. Supply Voltage V_{EE} Variation

The performance of the output voltage is shown in Figure 13. A 600 mV level for ECL compatibility is maintained.

VCO lock range is relatively insensitive to V_{EE} changes. The typical behavior is shown in Figure 14.

Temperature Performance

The VCO range of the HDMP-2501 is designed to accommodate variation over temperature. Figures 15 through 19 show typical performance over temperature.

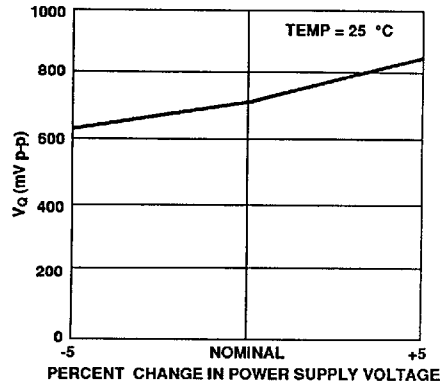


Figure 13. Output Voltage, V_Q vs. Power Supply, V_{EE}, Change.

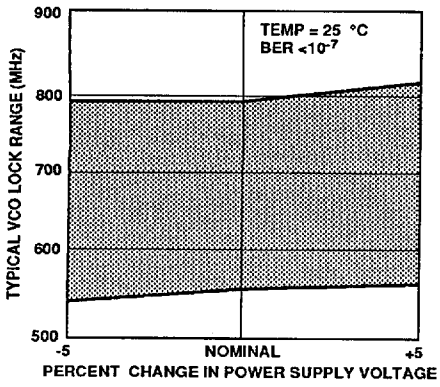


Figure 14. VCO Lock Range Variation vs. Supply Voltage, V_{EE}.

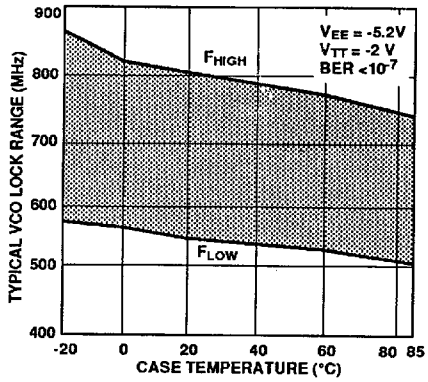


Figure 15. Typical VCO Lock Range Variation vs. Temperature.

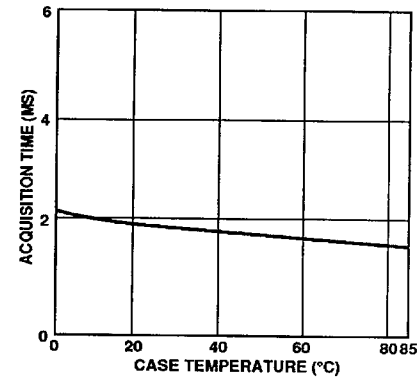


Figure 16. Typical Acquisition Time Variation vs. Temperature.

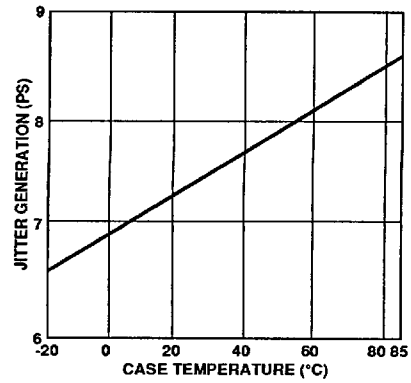


Figure 17. Typical RMS Value Jitter Generation Variation vs. Temperature with 3.5 ps Test Set Jitter.

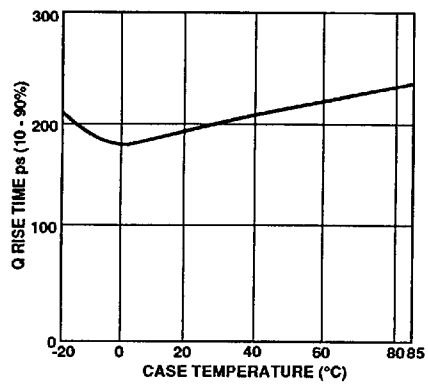


Figure 18. Typical Output Rise Time Variation vs. Temperature.

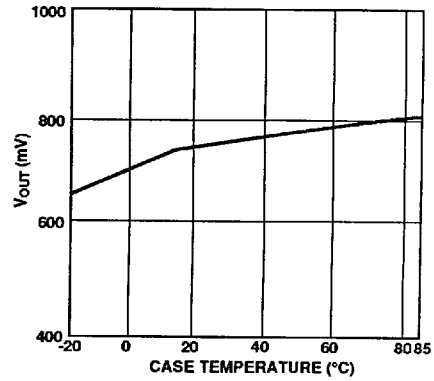


Figure 19. Typical Output Voltage Variation vs. Temperature.

Heat Sinking

Heat sinks are recommended for this part, especially for high temperature operation. When solder mounted on a board designed with the features shown in Figure 20, the thermal test card provides a thermal resistance (junction to air) θ_{JA} of approximately 40°C/W when measured in still air. The via holes shown are for thermal conduction between front side and back side metallization.

Package and Mechanical Considerations

The package is a glass metal construction designed for excellent high frequency electrical performance. The cover, base, and leads are gold plated Kovar (ASTM F-15 alloy). The mechanical outline is shown in Figure 21.

The base and cover of the package are electrically isolated and may be grounded. The base may be soldered to a printed circuit board.

NOTE: Maximum static pressure on package <30 PSI (MIL-STD-883, METHOD 1014). Care should be taken in handling and mounting so the pressure limit is not exceeded.

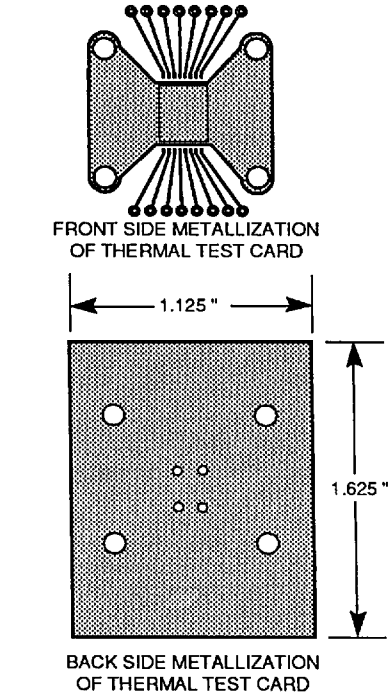


Figure 20. Circuit Mounting Configuration for Thermal Resistance Test.

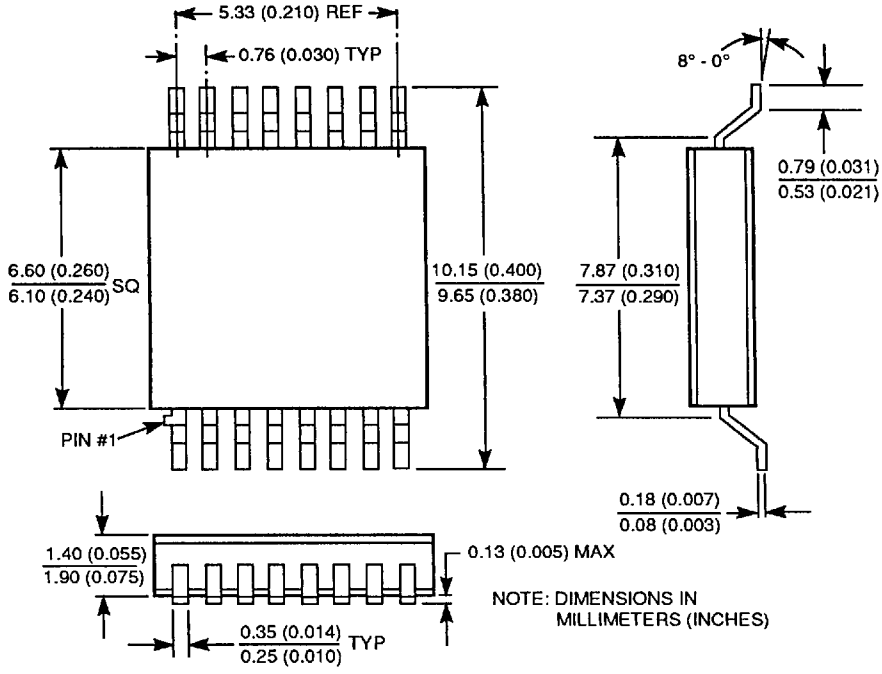


Figure 21. Outline F6.