Features

- 16-bit programmable local oscillator divider
- 14-bit programmable reference-frequency divider
- 1.5MHz to 55MHz local oscillator frequency
- 320Hz to 640kHz reference frequency using a 10.240MHz crystal
- Dual charge pump for rapid PLL locking
- PLL unlock indicator
- LPF transistor
- C^2B serial interface
- Operating voltage range: 2.0V~3.0V
- Standby mode for power saving
- Standard 24-pin SDIP package

Application

- Cordless Phone System
- Satellite Broadcast Tuners

General Description

The HT9286 is universal dual-PLL frequency synthesizer for use in cordless phone application and satellite broadcast tuner in U.S.A. The HT9286 has two PLLs with a 16-bit programmable divider to generate a 1.5MHz to 55MHz local oscillator frequency.

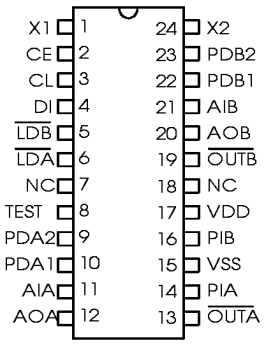
The device contains a phase detector and a dual charge pump for rapid PLL locking. It also has an unlock indication output and an uncommitted output under external control.

The PLLs share 14-bit divider to generate a 320Hz to 640kHz reference frequency using a 10.240MHz crystal.

The HT9286 can be controlled from an external microcontroller using a C^2B serial interface.

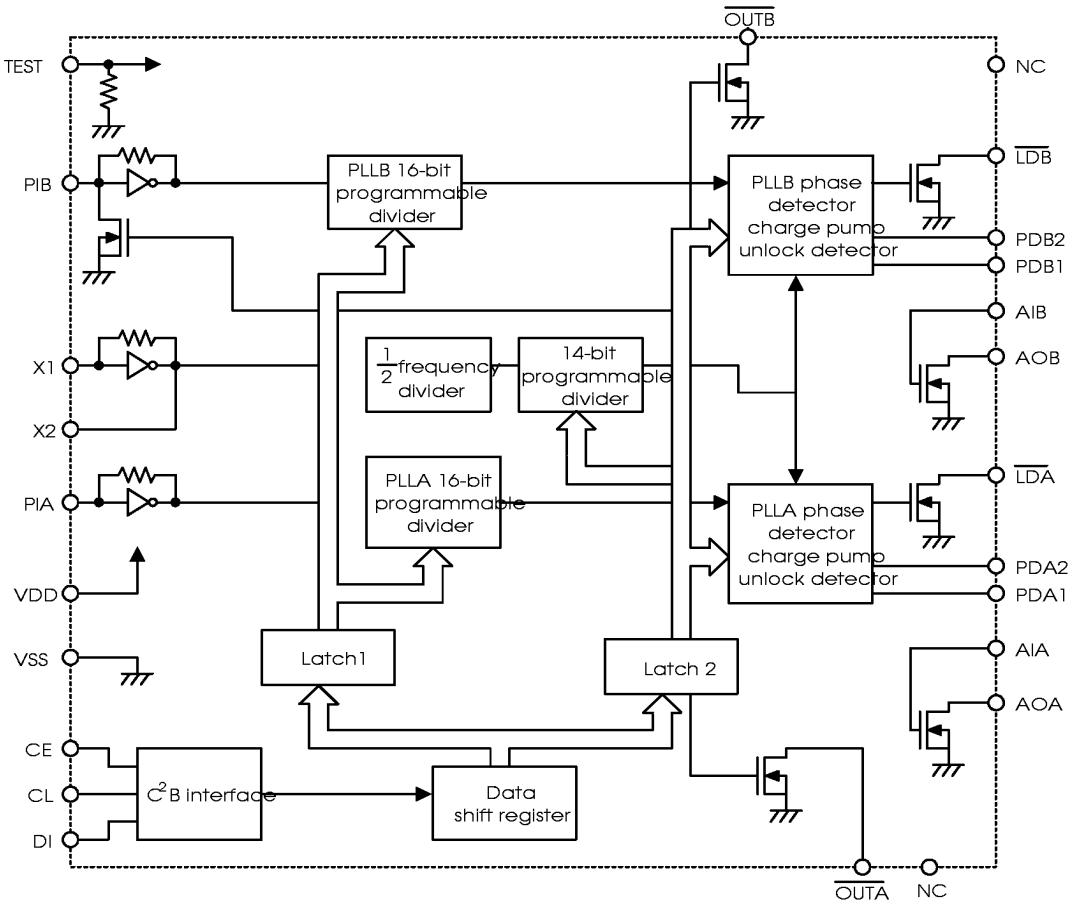
Other features include a standby mode for power saving and standard 24-pin SDIP package.

Pin Assignment



HT9286
– 24 SDIP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Function Description
1	X1	I	Crystal oscillator input.
2	CE	I	The enable pin controls the data transfer from the shift register to the latch.
3	CL	I	The clock input pin to control the data input of C^2B serial interface. Each low to high transition of the clock shifts one bit data into the shift register.
4	DI	I	The serial input data pin
5	$\overline{LDB}$	O	PLLB unlock detector output. When $\overline{LDB}$: "High", PLLB in lock state. $\overline{LDB}$: "Low", PLLB in unlock state.
6	$\overline{LDA}$	O	PLLA unlock detector output. When $\overline{LDA}$: "High", PLLA in lock state. $\overline{LDA}$: "Low", PLLA in unlock state.
7	NC	—	No connection.
8	TEST	I	Test input. When Test: "Low", Normal mode operation. Test: "High", Test mode operation.
9	PDA2	O	PLLA phase detector secondary output.
10	PDA1	O	PLLA phase detector main output.
11	AIA	I	LPF transistor A input.
12	AOA	O	LPF transistor A output.
13	$\overline{OUTA}$	O	committed output A.
14	PIA	I	PLLA local oscillator input. The output signal from VCO circuit can be A.C. coupled to this pin.
15	VSS	—	Ground
16	PIB	I	PLLB local oscillator input. The output signal from VCO circuit can be A.C. coupled to this pin.
17	VDD	—	Power supply
18	NC	—	No connection.
19	$\overline{OUTB}$	O	Uncommitted output B.
20	AOB	O	LPF transistor B output.
21	AIB	I	LPF transistor B input.
22	PDB1	O	PLLB phase detector main output.
23	PDB2	O	PLLB phase detector secondary output.
24	X2	O	Crystal oscillator output.

Absolute Maximum Ratings

Supply voltage ..... –0.3V to 7.0V
Power dissipation 160mW
Operating temperature range ..... –40°C to 85°C
Storage temperature range ..... –55°C to 125°C
CE, CL, DI, AIA and AIB input voltage range ..... –0.3V to 7.0V
XIN, PIA, PIB and TEST input voltage range ..... –0.3V to V_{DD}+0.3V
$\overline{LDA}$, $\overline{LDB}$, $\overline{OUTA}$ and $\overline{OUTB}$ output current range ..... 0mA to 3mA
AOA and AOB output current range ..... 0mA to 6mA
$\overline{LDA}$ and $\overline{LDB}$ output voltage range ..... –0.3V to 7.0V
AOA, AOB, $\overline{OUTA}$ and $\overline{OUTB}$ output volatge range ..... –0.3V to 15.0V
PDA1, PDA2, PDB1, PDB2 and X2 output voltage range ..... –0.3V to V_{DD}+0.3V

Recommended Operating Conditions

Supply voltage ..... 3V Supply voltage range ..... 2.0V to 3.3V

D.C. Characteristics (V_{DD}=2.0 to 3.3V, T_A=–40 to 85°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{DD}	Supply current	2V	Note (1)	—	3	8	mA
		3.3V	Note (1)	—	7	14	
		2V	Note (2)	—	1.5	4.5	
		3.3V	Note (2)	—	3.9	8	
V_{IL1}	CE, CL and DI low-level input voltage	2V	—	0	—	0.4	V
		3.3V	—	0	—	0.6	
V_{IH1}	CE, CL, and DI high-level input voltage	2V	—	1.5	—	5.5	V
		3.3V	—	1.7	—	5.5	
V_{OL1}	PDA1 and PDB1 low-level output voltage	—	I_O=1mA	—	—	1	V
V_{OL2}	PDA2 and PDB2 low-level output voltage	—	I_O=2mA	—	—	1	V
V_{OL3}	$\overline{OUTA}$, $\overline{OUTB}$, $\overline{LDA}$ and $\overline{LDB}$ low-level output voltage	—	I_O=2mA	0	—	1	V

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{OL4}	AOA and AOB low-level output voltage	—	I_O=0.5mA, V_{AIA}=V_{AIB}=1.2V	0	—	0.5	V
			I_O=1mA, V_{AIA}=V_{AIB}=1.3V	0	—	0.5	
V_{OH1}	PDA1 and PDB1 high-level output voltage	—	I_O=1mA	V_{DD}–1	—	—	V
V_{OH2}	PDA2 and PDB2 high-level output voltage	—	I_O=2mA	V_{DD}–1	—	—	V
V_{O1}	$\overline{LDA}$ and $\overline{LDB}$ output voltage	—	—	0	—	5.5	V
V_{O2}	AOA, AOB, $\overline{OUTA}$ and $\overline{OUTB}$ output voltage	—	—	0	—	13	V
I_{IL1}	CE, CL and DI low-level input current	—	V_I=0V	—	—	5	μA
I_{IL2}	X1 low-level input current	3.3V	V_I=0V	2	—	6.5	μA
I_{IL3}	PIA and PIB low-level input current	3.3V	V_I=0V	3.5	—	10	μA
I_{IL4}	AIA and AIB low-level input current	—	V_I=0V	—	0.01	10	μA
I_{IL5}	TEST low-level input current	3.3V	V_I=0V	—	—	5	μA
I_{IH1}	CE, CL and DI high-level input current	—	V_I=5.5V	—	—	5	μA
I_{IH2}	X1 hihg-level input current	3.3V	V_I=3.3V	2	—	6.5	μA
I_{IH3}	PIA and PIB high-level input current	3.3V	V_I=3.3V	3.5	—	10	μA
I_{IH4}	AIA and AIB high-level input current	3.3V	V_I=3.3V	—	0.01	10	μA
	TEST high-level input current			—	120	—	μA
I_{DFF1}	$\overline{LDA}$ and $\overline{LDB}$ output leakage current	—	V_O=5.5V	—	—	5	μA
I_{DFF2}	PDA1, PDB1, PDA2 and PDB2 output leakage current	—	V_O=0V or 3.3V	—	0.01	10	μA

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{I1}	X1 input frequency	—	Capacitively coupled sin wave	1	—	13	MHz
f_{I2}	PIA and PIB input amplitude	—	Capacitively coupled sin wave FA=FB=0	1.5	—	23	MHz
			Capacitively coupled sin wave FA=FB=1	20	—	55	
V_{I1}	X1 input amplitude	—	Capacitively coupled sin wave	200	—	600	mV
V_{I2}	PIA and PIB input amplitude	—	Capacitively coupled sin wave	100	—	600	mV
f_{XTAL}	Crystal oscillator frequency	—	CI<50, CL<16pF Note (3)	4	10.24	11	MHz
R_{11}	X1 internal feedback resistor	3.3V	—	—	1	—	MΩ
R_{12}	PIA and PIB internal feedback resistor	3.3V	—	—	600	—	kΩ
R_C	TEST internal pull-down resistor	3.3V	—	—	30	—	kΩ
C_I	X1, PIA and PIB input capacitance	3.3V	—	—	2.5	—	pF

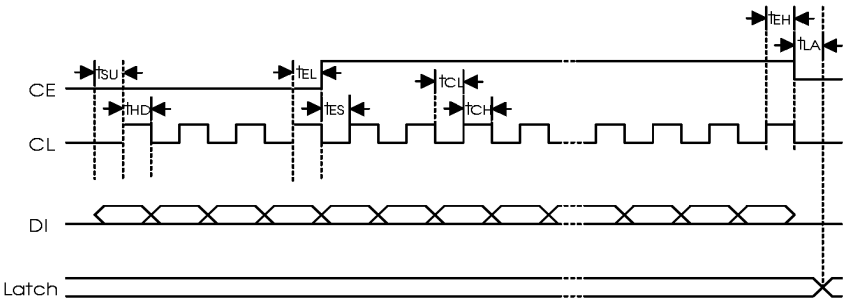
Notes:

(1) Dual PLL, both PLLA and PLLB operating, SB=0, f_{XTAL}=10.24MHz, V_{PIA}=V_{PIB}=100mV at 55MHz, all other inputs=0V, all output open.

(2) Standby mode, PLLB stopped, SB=1, f_{XTAL}=10.24MHz, V_{PIA}=100mV at 55MHz, all other inputs=0V, all output open.

(3) CI is the capacitive reactance and CL is the load capacitance.

Serial Data Input Timing



Symbol	Parameter	Condition	Min.	Max.	Unit
t_{SU}	Data setup time	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{HD}	Data hold time	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{EL}	Low-level chip enable time	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{ES}	Chip enable setup time	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{EH}	Chip enable hold time	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{CL}	Low-level clock pulse width	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{CH}	High-level clock pulse width	10.24 MHz crystal	400	—	ns
		Other crystal frequencies	$4/f_{XTAL}$	—	ns
t_{LA}	Chip enable to data latch time	10.24 MHz crystal	—	400	ns
		Other crystal frequencies	—	$4/f_{XTAL}$	ns

Function Description

PLLA and PLLB programmable dividers

The divider ratios of PLLA and PLLB are set by Mode 1 command N_A bits DA0 to DA15 and N_B bits DB0 to DB15 respectively.

Programmable reference divider

The divider ratio N_R is set by Mode 2 command bits R0 to R13. The reference frequency is given by $f_{XTAL}/2 \times N_R$.

Phase detector

The phase-detector output states as a function of the divider ratio and reference frequency is shown is table 1.

Table1. Phase-detector output states

Condition	PDA1, PDB1
$f_{I/N} > f_{ref}$	High
$f_{I/N} < f_{ref}$	Low
$f_{I/N} = f_{ref}$	High impedance

Note: f_I=from VCO output frequency
N=N_A for PLLA and N_B for PLLB

When PLLA is unlocked, $\overline{LDA}$ is pulled low and both PDA1 and PDA2 are active, PLLB operates identically to PLLA.

Mode 2 command bits UL0 and UL1 set the unlock phase-error threshold and bits UE0 and UE1 are $\overline{LDA}$ and $\overline{LDB}$ output extensions.

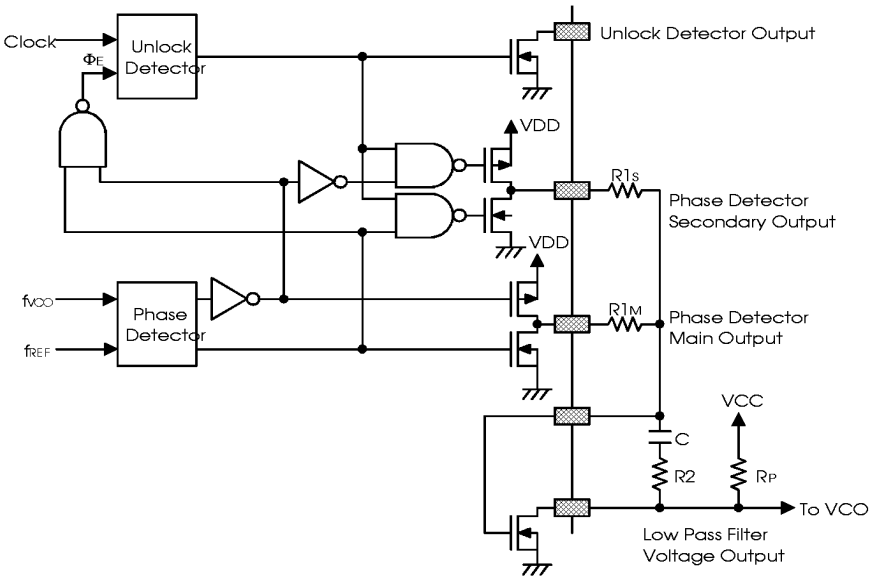
Dual charge pump

Figure 1 shows a typical dual charge-pump circuit.

The phase-detector secondary output is active after a change in frequency or the phase error causes the PLL to unlock.

In this case, the load resistance R1 becomes $R1_M$ // $R1_S$ decreasing the LPF time constant and the time required to lock the PLL.

The phase-detector secondary output is high impedance when the PLL is locked. In this case R1 becomes $R1_M$ increasing the LPF time constant and improving sideband and modulation response.



Frigure 1. Dual charge-pump circuit

Mode 1 command format and functions

The Mode 1 command comprises the data bits which determine the PLLA and PLLB programmable divider ratios.

The command format is shown in figure 2. Bits DA0 to DA15 and DB0 to DB15 determine the PLLA and PLLB programmable divider ratios respectively. Bit DA0 is the first bit received. The range of allowable divider ratios is N=256 (0100H) to 65535 (FFFFH).

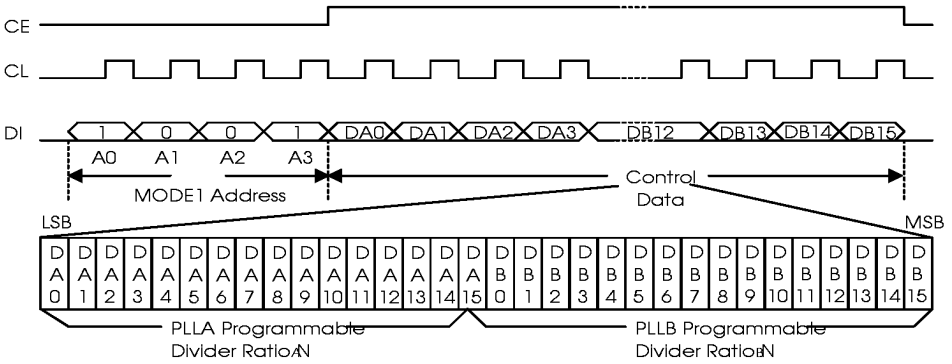


Figure 2. Mode 1 command (programmable divider data)

Mode 2 command format and functions

The Mode 2 command comprises the data bits which determine the reference frequency divider ratio and control functions.

The command format is shown in figure 3. Bit R0 is the first bit received.

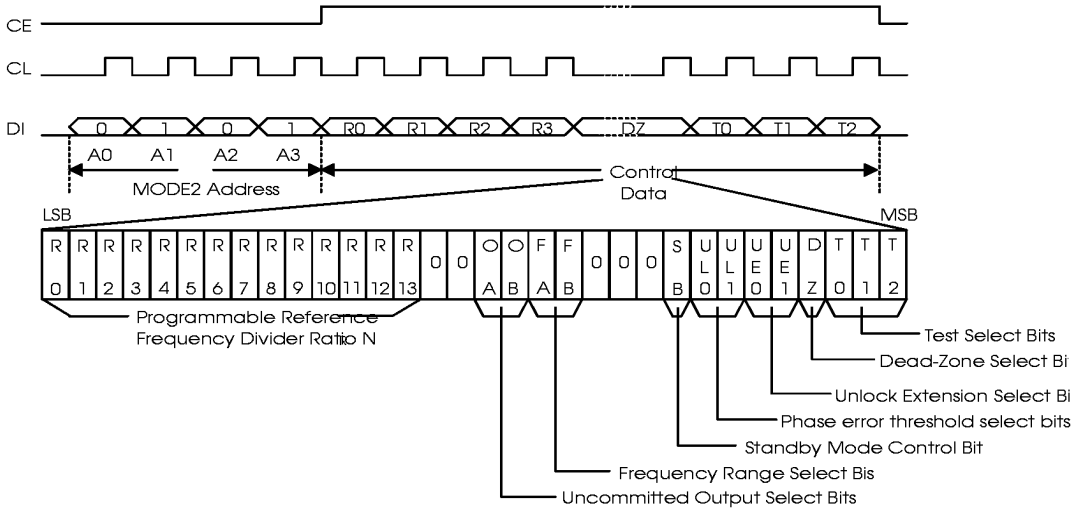


Figure 3. Mode 2 command(reference divider and control data)

Bits R0 to R13 determine the reference divider ratio. The range of allowable divider ratios is N_R=8 (0008H) to 16383 (3FFFH).

Bits OA and OB are the uncommitted output control bits. They are latched and then inverted to control $\overline{OUTA}$ and $\overline{OUTB}$ respectively.

If either bit is "1", the open-drain output is pulled low.

Bits FA and FB are the input frequency range select bits. The PIA and PIB frequency ranges set by FA and FB respectively are shown in table 2.

Table 2. Frequency ranges

FA, FB	Input frequency range	Unit
0	1.5 to 23	MHz
1	20 to 55	MHz

Bits SB is the standby mode control bit. When SB="1", standby mode is selected. In standby mode, PLLB is stopped, PIB is pulled low and PDB1, PDB2 are high impedance. When SB="0", normal operation is selected.

Bits UL0 and UL1 determine the unlock detection threshold. The PLL unlock detector output: $\overline{LDA}$ or $\overline{LDB}$ is pulled low when the phase error Φ_E between the reference and the divider inputs exceeds the threshold set by UL0 and UL1.

The threshold for different crystal frequency is shown in table 3 and the threshold for other frequencies can be calculated.

The threshold is common to both PLLs. Note that a PLL will temporarily lose lock when either UL0 or UL1 is changed. (refer Table 3)

Table 3. Unlock detector thresholds

UL0	UL1	$\overline{LDA}$, $\overline{LDB}$ phase error threshold	Example phase error thresholds (μS)				
			f_{XTAL}= 4MHz	f_{XTAL}= 7.2MHz	f_{XTAL}= 8MHz	f_{XTAL}= 10.24MHz	f_{XTAL}= 12.8MHz
0	0	0	0	0	0	0	0
1	0	$\pm 4/f_{XTAL}$	± 1.00	± 0.55	± 0.05	± 0.35	± 0.31
0	1	$\pm 16/f_{XTAL}$	± 4.00	± 2.22	± 2.00	± 1.56	± 1.20
1	1	$\pm 64/f_{XTAL}$	± 16.00	± 8.85	± 8.00	± 6.25	± 5.00

Bits UE0 and UE1 determine the unlock extension or delay, before the unlock-detector outputs, $\overline{LDA}$ and $\overline{LDB}$ can change state.

The extension for different reference frequency is shown in table 4. However if a phase-error threshold of zero is set using UL0 and UL1, no output extension occurs.

Table 4. $\overline{LDA}$, $\overline{LDB}$ output extensions

UE0	UE1	$\overline{LDA}$, $\overline{LDB}$ output extension	Example output extensions (ms)		
			f_{ref}=1kHz	f_{ref}=5kHz	f_{ref}=12.5kHz
0	0	$4/f_{ref}$	4.0	0.8	0.32
1	0	$8/f_{ref}$	8.0	1.6	0.64
0	1	$32/f_{ref}$	32.0	6.4	2.56
1	1	$64/f_{ref}$	64.0	12.8	5.12

Bit DZ is the dead-zone selection bit. It selects the phase-insensitive bandwidth or dead zone of the phase comparator. When DZ="1", DZB mode is selected and when DZ="0", DZA mode is selected. DZB mode has a larger dead zone than DZA mode.

Test mode

When TEST pin is "high", this chip enter test mode. We can select different test iterms by determining T0, T1, T2 which shown in table 5.

Table 5. Test mode (TEST pin is pulled "high")

Condition (command 2)	Test Iterms
T0=T1=T2=0	The signal on $\overline{OUTA}$ has a frequency of $f_{XTAL}/2$.
T0=0, T1=1, T2=0	The signal on $\overline{OUTA}$ or $\overline{OUTB}$ has a frequency f_{XTAL}/N. $N=N_R$
T0=1, T1=0, T2=0	The signal on $\overline{OUTA}$ or $\overline{OUTB}$ has a frequency fvco/N. $N=N_A$ or N_B

Application Circuit

Figure 4 shows a HT9286 cordless phone application circuit.

The telephone is tuned to channel 1, which has a transmit VCO frequency of 46.610 MHz and a receive VCO frequency of 38.975 MHz.

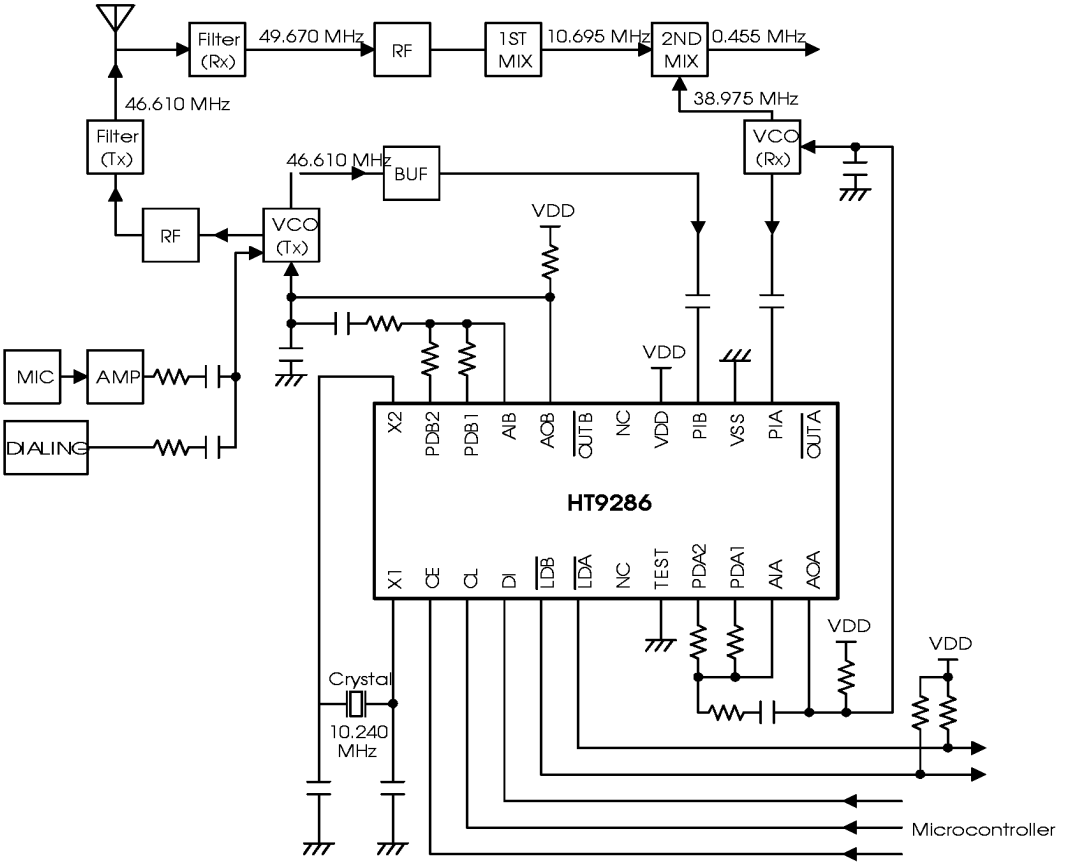


Figure 4. Cordless phone 46/49 MHz base station

We can follow HT9286 function description to determine what serial data to satisfy cordless phone systm specifications.

Solution: For f_{ref} = 5kHz, the divider ratios are as follows.

$$N_A = \frac{VCO\ (Rx)}{f_{ref}} = \frac{38.975\ MHz}{5\ kHz} = 7795\ (1E73H)$$

$$N_R = \frac{T\ x\ VCO}{f_{ref}} = \frac{46.610\ MHz}{5\ KHz} = 9322\ (246AH)$$

$$N_R = \frac{f_{XTAL}}{2\ x\ f_{ref}} = \frac{10.240\ MHz}{2\ x\ f_{ref}} = 1024\ (400H)$$

The Mode 1 and Mode 2 commands are shown in table 6 and table 7 respectively and in figure 5 and figure 6 respectively.

Table 6. Mode 1 command

Field	Value	Command
DA0 to DA15	1E73H	PLLA divider ratio of 7795
DB0 to DB15	246AH	PLLB divider ratio of 9322

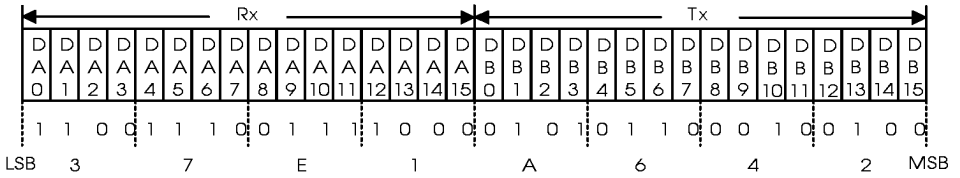


Figure 5. Mode 1 command

Table 7. Mode 2 command

Field	Value	Command
R0 to R13	0400H	Reference divider ratio of 1024
OA	0	$\overline{OUTA}$ and $\overline{OUTB}$ left open
OB	0	
FA	1	20 to 55 MHz Rx VCO input frequency range
FB	1	20 to 55 MHz Tx VCO input frequency range
SB	0 or 1	Standby mode selection
UL0, UL1	11	±6.25 μs lock/unlock detection threshold
UE0, UE1	01	6.4 ms $\overline{LDA}$ and $\overline{LDB}$ output extension
DI	1	DZB dead-zone mode
T0, T1, T2	000	Test mode

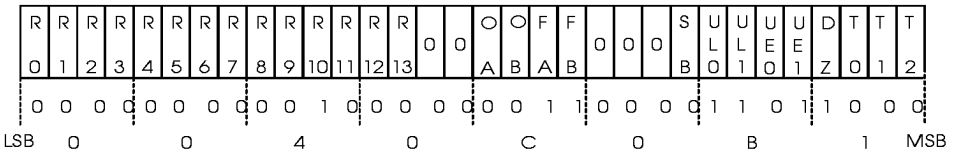


Figure 6. Mode 2 command