HT9287A/HT9287B

Dual PLLs for 46/49MHz Cordless Phone

Features

- Single 2.5 to 5.5V power supply
- On chip oscillator circuits with external X-TAL (10.240MHz)
- Synthesizer up to 10-channel pairs
- Base/Handset selected by MODE pin
- Maximum operating frequency: 60MHz@ Vin= 200mV$_{P-P}$
- Standby mode for power saving by $\overline{SB}$ pin
- Lock detect signal
- 5 kHz output for guard tone
- Standard 16-pin DIP/SOP/NSOP packages

Application

- Cordless Phone System

General Description

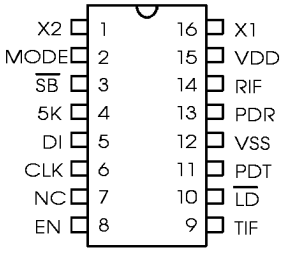
The HT9287A/9287B are dual phase-locked loop frequency synthesizers developed for 46/49MHz of 10-channel band frequency of cordless phone Which are used in U.S.A.

These devices contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits.

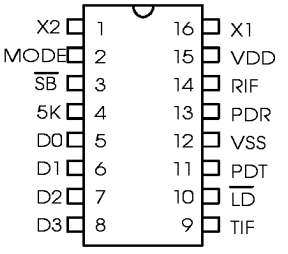
Frequency selection are accomplished by 4-bit parallel input for the HT9287B and serial interface for the HT9287A.

Other features include a lock detect circuit for the transmit loop and a 5.0kHz tone output.

Pin Assignment

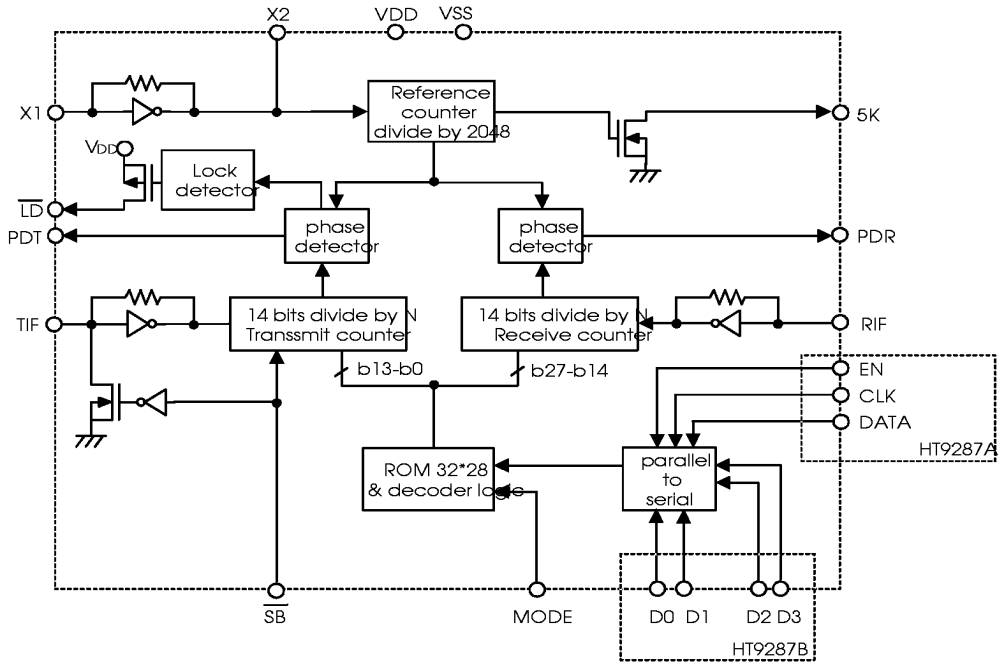


HT9287A
–16 DIP/SOP/NSOP



HT9287B
–16 DIP/SOP/NSOP

Block Diagram



Pad Description

Pin No.	Pin Name	I/O	Function Description
1	X2	O	This output pin generates reference frequency when it is connected to pin 16 with an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24MHz crystal is need.
2	MODE	I	Mode is for determining whether this chip is to be used in the base or handset of a cordless phone. Internal, this pin is used in the decoding logic for selecting the ROM address. When V_{DD}=base mode, and when V_{SS}=handset mode.
3	$\overline{SB}$	I	This pin is used to save power while no transmit and internal pull down. $\overline{SB}$: High, transmit and receive active. $\overline{SB}$: Low, receive acts only.
4	5K	O	The signal derived from the reference oscillator and reference divider, this output is n-channel open drain.

Pin No.	Pin Name	I/O	Description
5	D0 (LSB)	I	These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and receive loop. When address data selects over 1-10, the decoding logic defaults to channel 10. The frequency assignments with D0-D3 are shown in Table 1. These inputs have internal pull down devices.
6	D1	I	
7	D2	I	
8	D3 (MSB)	I	
9	TIF	I	Input to 14-bit programmable transmit counter. The output signal from external VCO circuit can be ac coupled to this pin, the minimum input level is 200m V_{P-P}.
10	$\overline{LD}$	O	Lock detect signal associated with the transmit loop. V_{DD} level: indicate an out-off-lock condition. This is a p-channel open-drain output.
11	PDT	O	Phase detector output for transmit. PDT detects the phase error from transmit PLL and it's output is connected to external low pass filter.
12	VSS	—	Ground
13	PDR	O	Phase detector output for receive. PDR detects the phase error from receive PLL and it's output is connected to external low pass filter.
14	RIF	I	Input to 14-bit programmable receive counter. The output signal from external VCO circuit can be ac coupled to this pin, the minimum input level is 200m V_{P-P}.
15	VDD	—	Power supply
16	X1	I	Connect to the pin 1, external parallel-resonant crystal and capacitor.
5	DI (HT9287A only)	I	The serial input data pin.
6	CLK (HT9287A only)	I	Clock input. Each low to high trnasition of the clock shifts one bit of data into the on-chip shift register.
7	NC	—	No connection
8	EN (HT9287A only)	I	The enable pin controls the data transfer from the shift register to the 4-bit latch. A low to high transition latches the data.

Absolute Maximum Ratings

DC supply voltage.....–0.5 to 6V
Input voltage ..... –0.5 to V_{DD}+0.5V
DC current drain per pin 10mA
Operating temperature range.....–30 to 75°C
Storage temperature range.....–65 to 150°C
DC current drain V_{DD} or V_{SS} pins.....30mA

D. C. Characteristics

(T_A=25°C)

Symbol	Characteristic	Test Condition		Min	Typ.	Max	Unit
		V_{DD}	Condition				
V_{DD}	Power Supply Voltage	—	—	2.5	—	5.5	V
V_{OH}	Output Voltage	2.5V 5.5V	—	2.45 5.45	— —	— —	V
V_{OL}		2.5V 5.5V	—	— —	— —	0.05 0.05	
V_{IH}	Input Voltage	2.5V 5.5V	—	1.75 3.85	— —	— —	V
V_{IL}		2.5V 5.5V	—	— —	— —	0.75 1.65	
I_{OH}	Output Current	2.5V 5.5V	V_{OUT}= 2.2V V_{OUT}= 5.0V	–0.18 –0.55	— —	— —	mA
I_{OL}		2.5V 5.5V	V_{OUT}= 0.3V V_{OUT}= 0.5V	— —	— —	0.18 0.55	
I_{IH}	Input Current	2.5V 5.5V	X_1, TIF, RIF	— —	— —	–30 –66	µA
		2.5V 5.5V	DATA,$\overline{SB}$, MODE	— —	— —	–0.05 –0.11	
I_{IL}		2.5V 5.5V	X_1, TIF, RIF	— —	— —	30 66	
		2.5V 5.5V	DATA, $\overline{SB}$, MODE	— —	— —	50 121	
I_{STB}	Standby Current	2.5V 5.5V	Note 1	— —	— —	1.4 3.6	mA
I_{DD}	Operating Current	2.5V 5.5V	Note 2	—	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current	5.5V	—	—	—	±1	µA

Note 1: X_1: 10.240MHz ; MODE: V_{DD}; $\overline{SB}$: V_{SS}; others are open.

Note 2: X_1: 10.240MHz ; MODE: V_{DD}; $\overline{SB}$: V_{DD}; others are open. (200 mV_{P-P} input at RIF, TIF)

A. C. Characteristics

Symbol	Characteristic	Test Condition		Min	Typ.	Max	Unit
		V_{DD}	Condition				
t_{TLH}	Output Rise Time	3V 5V	Figure 1	—	— —	200 100	ns
t_{THL}	Output Fall Time	3V 5V	Figure 1	—	— —	200 100	ns
T_R	Input Rise Time	3V 5V	Figure 2	—	— —	5 4	μA
T_F	Input Fall Time	3V 5V	Figure 2	—	— —	5 4	μA
F_{MAX}	Input Frequency	3V 5V	X1 TIF input= Sine Wave 200 mV_{P-P} RIF	—	— —	12 60 60	MHz
t_{SU}	Setup Time: data to clock (HT9287A) Setup Time: enable to clock (HT9287A)	3V 3V	Figure 3	100 200	— — — —	— — — —	ns
t_H	Hold Time: clock to data (HT9287A)	3V	Figure 3	80	— —	— —	ns
t_{REC}	Recovery Time: enable to clock (HT9287A)	3V	Figure 4	80	— —	— —	ns
t_W	Input pulse width: clock and enable (HT9287A)	3V	Figure 4	80	— —	— —	ns

Function Description

The HT9287A/9287B are dual phase-locked loop frequency synthesizers developed for 46/49MHz of 10-channel band frequency of cordless phone which are used in U.S.A.

To accomplish the duplex communication in cordless phone system, it must use two different channels to reach the function.

See the table 1 which show the receive channel and transmit channel between base and handset. If any channel of base and handset account interference while radio link, these devices can select another pair to improve the quality of communication.

The $\overline{SB}$ pin is used to save power when not transmitting. IF $\overline{SB}$ is high both the transmit and receive loops are in operating else transmit loop is disabled. Figure5 show the cordless phone application diagram.

Table 1 Divide Ratios and VCO Frequencies Base (MODE=1)

Input				CH	Rx (Fref=5KHz)			Tx= (Fref=5KHz)		
D3	D2	D1	D0		FR_X (MHz)	FVCO (MHz)	N	TR_X (MHz)	FVCO (MHz)	N
0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322
0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326
0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334
0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342
0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346
0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354
0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366
1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374
1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386
1	0	1	0	10	49.970	39.275	7855	46.970	46.970	9394
1	0	1	1	10	49.970	39.275	7855	46.970	46.970	9394
1	1	0	0	10	49.970	39.275	7855	46.970	46.970	9394
1	1	0	1	10	49.970	39.275	7855	46.970	46.970	9394
1	1	1	0	10	49.970	39.275	7855	46.970	46.970	9394
1	1	1	1	10	49.970	39.275	7855	46.970	46.970	9394
0	0	0	0	10	49.970	39.275	7855	46.970	46.970	9394

Remote (MODE=0)

Input				CH	Rx (Fref=5KHz)			Tx= (Fref=5KHz)		
D3	D2	D1	D0		FR_X (MHz)	FVCO (MHz)	N	FT_X(MHz)	FVCO (MHz)	N
0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934
0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969
0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972
0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954
0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975
0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966
0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978
1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986
1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998
1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994
1	0	1	1	10	46.970	36.275	7255	49.970	49.970	9994
1	1	0	0	10	46.970	36.275	7255	49.970	49.970	9994
1	1	0	1	10	46.970	36.275	7255	49.970	49.970	9994
1	1	1	0	10	46.970	36.275	7255	49.970	49.970	9994
1	1	1	1	10	46.970	36.275	7255	49.970	49.970	9994
0	0	0	0	10	46.970	36.275	7255	49.970	49.970	9994

Timing Diagram

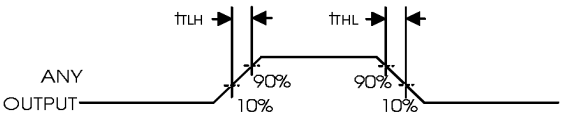


Figure 1

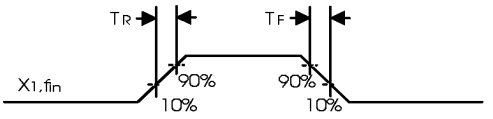


Figure 2

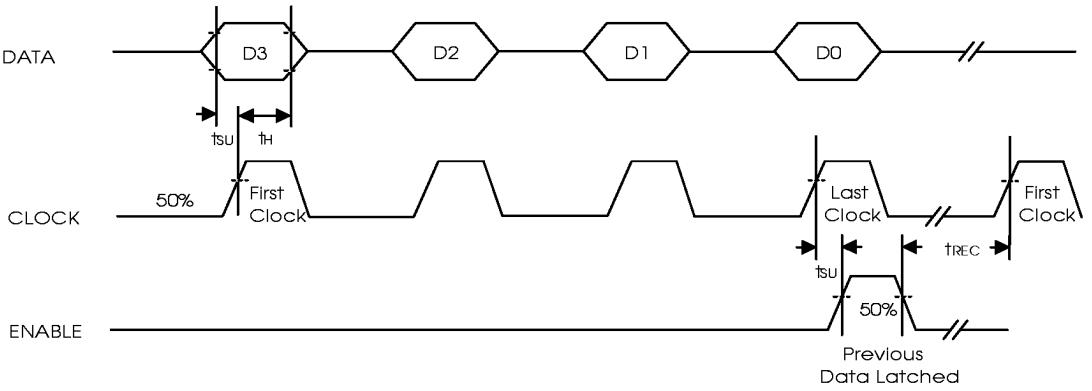


Figure 3

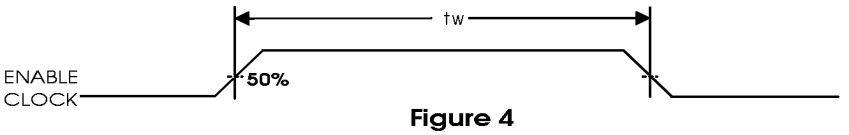


Figure 4

Application Circuit

HT9287A/HT9287B

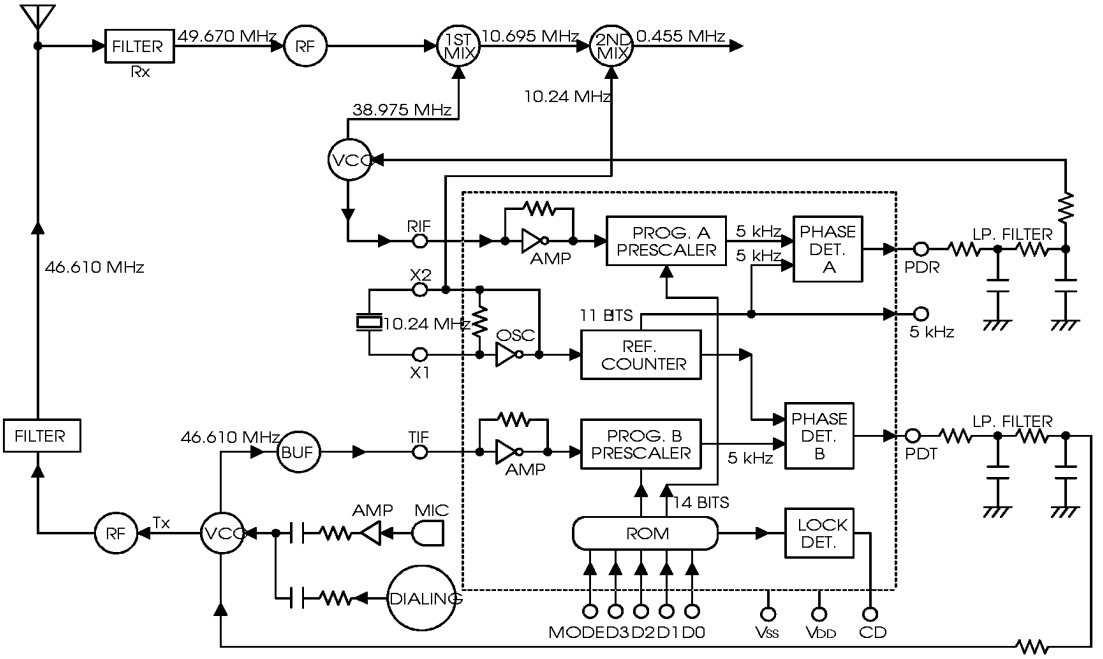


Figure 5