

NBSG16

Product Preview

2.5V / 3.3V SiGe Differential Receiver/Driver with RSECL* Outputs

*Reduced Swing ECL

The SG16 is a Silicon Germanium differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices with much higher bandwidth and lower EMI capabilities.

Inputs contain internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), HSTL, GTL, TTL, CMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV. For LVDS, CML, or CMOS outputs, use the device product numbers NBSGL16, NBSGM16, or NBSGC16.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used for single-ended NECL or PECL inputs and the V_{MM} pin is used for CMOS inputs. For all single-ended input conditions, the unused differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μ f capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

- Maximum Frequency > 12 GHz Typical
- 40 ps Typical Rise and Fall Times
- RSPECL Output with RSPECL, PECL, HSTL, GTL, TTL, CMOS, CML, or LVDS Inputs with Operating Range: $V_{CC} = 2.375$ V to 3.6 V with $V_{EE} = 0$ V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.6 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 75 k Ω Pulldown Resistor on D and \bar{D} , 36.5 k Ω Pullup Resistor on \bar{D}
- 50 Ω Internal Input Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- ESD Protection: (TBD)
- V_{BB} and V_{MM} Reference Voltage Output
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test (TBD)
- Moisture Sensitivity Level 3: ASE Requires Drypack
- Flammability Rating: TBD
- Transistor Count: 167 Devices

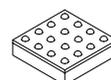
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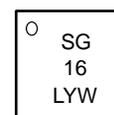
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MARKING DIAGRAM*



BGA-16
BA SUFFIX
CASE 489



L = Wafer Lot
Y = Year
W = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

| Device | Package | Shipping |
|------------|---------------|------------------|
| NBSG16BA | 4x4 BGA-16 | 810 Units/Tray |
| NBSG16BAR2 | 4x4 BGA-16 | 2500 Tape & Reel |

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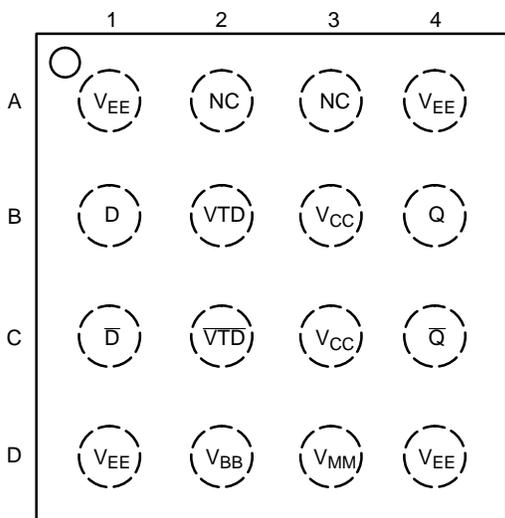


Figure 1. Pinout (Top View)

PIN DESCRIPTION

| PIN | FUNCTION |
|------------------|--|
| D*, \bar{D} ** | ECL, HSTL, GTL, TTL, CMOS, CML, LVDS compatible inputs |
| Q, \bar{Q} | RSECL Data Outputs |
| VTD | 50 Ω Internal Input Termination Resistor |
| \bar{VTD} | 50 Ω Internal Input Termination Resistor |
| V _{MM} | CMOS Reference Voltage Output, V _{CC} /2 |
| V _{BB} | ECL Reference Voltage Output |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |
| NC | No Connect |

* Pin will default low when left open.

** Pin will default to a slightly higher potential than D when both are left open.

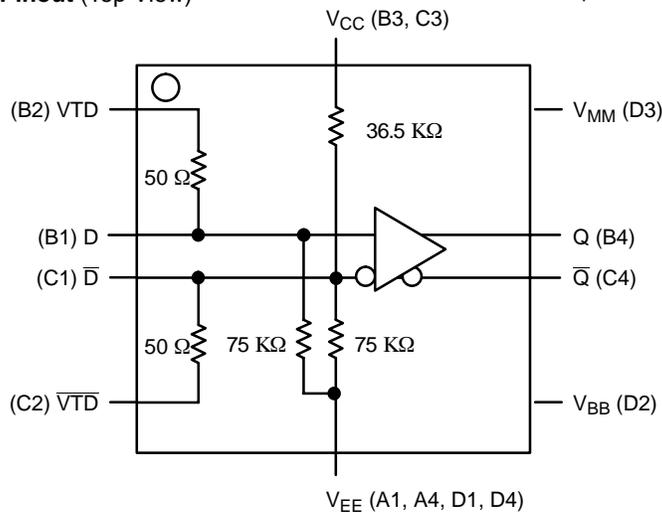


Figure 2. Logic Diagram

MAXIMUM RATINGS (Note 1.)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|------------------|--|--|--|-------------|--------------|
| V _{CC} | Positive Power Supply | V _{EE} = 0 V | | 3.8 | V |
| V _{EE} | Negative Power Supply | V _{CC} = 0 V | | -3.8 | V |
| V _I | Positive Input Negative Input | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 3.8 -3.8 | V V |
| I _{out} | Output Current | Continuous Surge | | 25 50 | mA mA |
| I _{BB} | V _{BB} Sink/Source | | | 1 | mA |
| I _{MM} | V _{MM} Sink/Source | | | 1 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction to Ambient) | 0 LFPM 500 LFPM | 16 BGA 16 BGA | 149 127 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) | std bd | 16 BGA | TBD | °C/W |
| T _{sol} | Wave Solder | TBD | | 265 | °C |

1. Maximum Ratings are those values beyond which device damage may occur.

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DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 2.)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|---------------------|-------------|-----|-------------|------|-----|-------------|-----|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | | | | 25 | | | | | mA |
| V_{OH} | Output HIGH Voltage (Note 3.) | | | | | 1400 | | | | | mV |
| V_{OL} | Output LOW Voltage (Note 3.) | | | | | 1000 | | | | | mV |
| V_{BB} | PECL Output Voltage Reference | | | | | 1200 | | | | | |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Note 4.) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| V_{MM} | CMOS Output Voltage Reference $V_{CC}/2$ | | | | | 1250 | | | | | mV |
| R_T | Internal Termination Resistor | | | | | 50 | | | | | Ω |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | $\frac{D}{\bar{D}}$ | 0.5 -150 | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -1.1 V.

3. All loading with 50 ohms to V_{CC} -2.0 volts.

4. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 5.)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|---------------------|-------------|-----|-------------|------|-----|-------------|-----|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | | | | 25 | | | | | mA |
| V_{OH} | Output HIGH Voltage (Note 6.) | | | | | 2200 | | | | | mV |
| V_{OL} | Output LOW Voltage (Note 6.) | | | | | 1800 | | | | | mV |
| V_{BB} | PECL Output Voltage Reference | | | | | 2000 | | | | | |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Note 7.) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| V_{MM} | CMOS Output Voltage Reference $V_{CC}/2$ | | | | | 1650 | | | | | mV |
| R_T | Internal Termination Resistor | | | | | 50 | | | | | Ω |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | $\frac{D}{\bar{D}}$ | 0.5 -150 | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.3 V.

6. All loading with 50 ohms to V_{CC} -2.0 volts.

7. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT $V_{CC} = 0\text{ V}$; $V_{EE} = -3.6\text{ V}$ to -2.375 V (Note 8.)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|---------------|-------------|-----|--------------|-------------|-----|--------------|-------------|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | | | | 25 | | | | | mA |
| V_{OH} | Output HIGH Voltage (Note 9.) | | | | | -1100 | | | | | mV |
| V_{OL} | Output LOW Voltage (Note 9.) | | | | | -1500 | | | | | mV |
| V_{BB} | NECL Output Voltage Reference | | | | | -1300 | | | | | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 10.) | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | V |
| V_{MM} | CMOS Output Voltage Reference | | | | | $V_{EE}/2$ | | | | | mV |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | $\frac{D}{D}$ | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | μA |

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC} .

9. All loading with 50 ohms to $V_{CC}-2.0$ volts.

10. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.6\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.6 V ; $V_{EE} = 0\text{ V}$

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|--|-------|-----|-----|------|------|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Frequency (See Figure 3. F_{max}/JITTER) (Note 11.) | | | | | > 12 | | | | | GHz |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential P to P | | | | | 150 | | | | | ps |
| t_{SKEW} | Duty Cycle Skew (Note 12.) | | | | | TBD | | | | | ps |
| t_{JITTER} | Cycle-to-Cycle Jitter (See Figure 3. F_{max}/JITTER) (Note 11.) | | | | | TBD | | | | | ps |
| V_{PP} | Input Voltage Swing | | | | 150 | 400 | | | | | mV |
| t_r , t_f | Output Rise/Fall Times (20% – 80%) Q, \bar{Q} | | | | | 40 | | | | | ps |

11. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}-2.0\text{ V}$.

12. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

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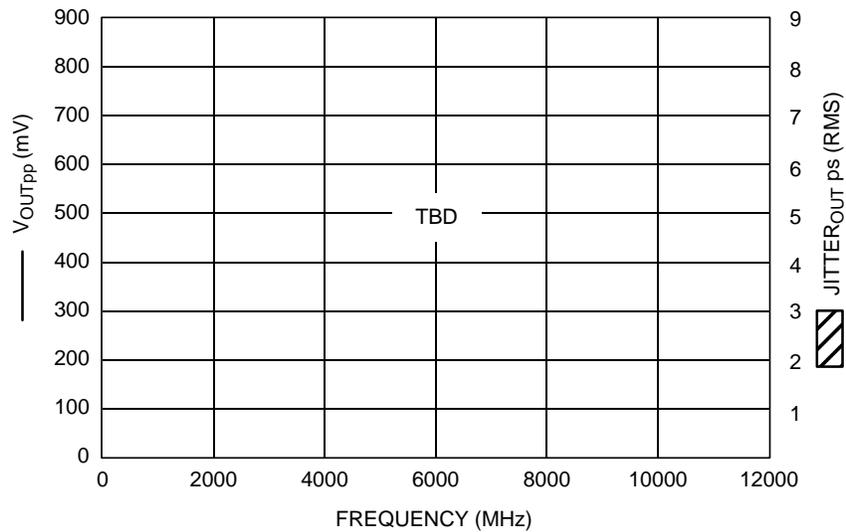


Figure 3. $F_{max}/Jitter$

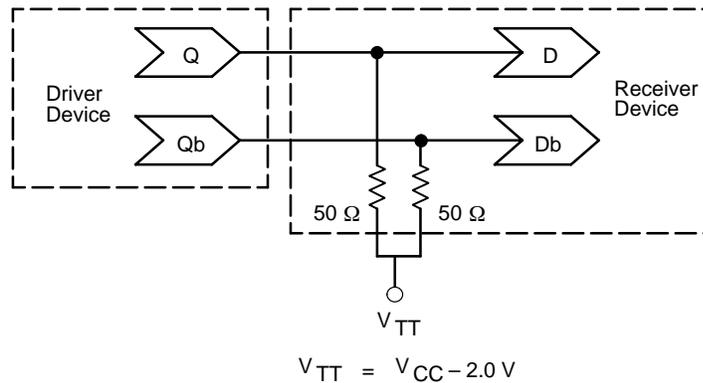


Figure 4. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020 – Termination of ECL Logic Devices)

Resource Reference of Application Notes

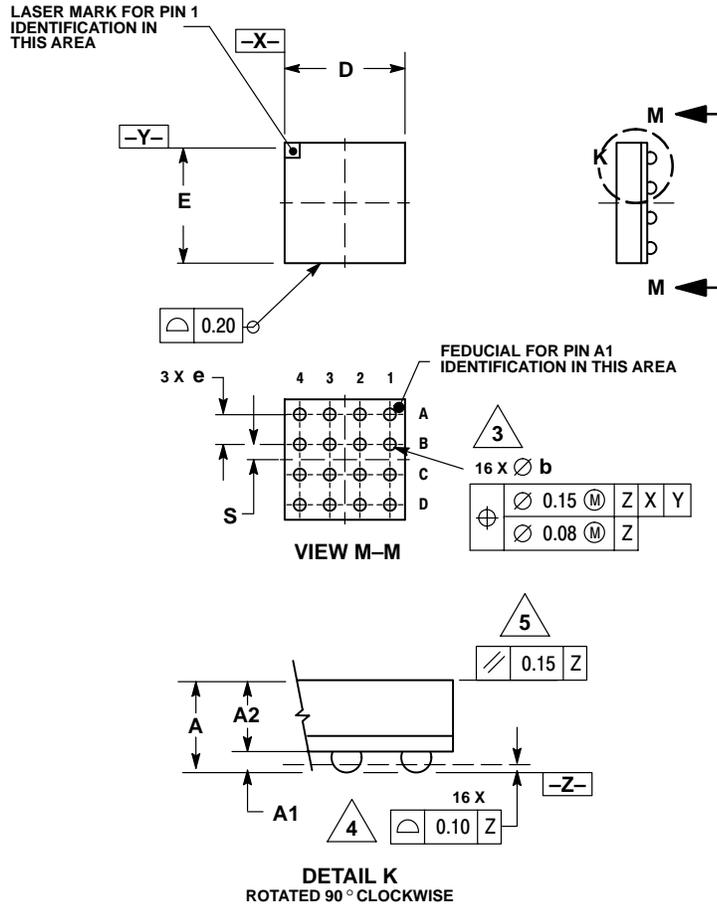
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

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PACKAGE DIMENSIONS

BGA-16
BA SUFFIX
 PLASTIC 4 X 4 BGA FLIP CHIP PACKAGE
 CASE 489
 ISSUE O



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 1.40 | MAX |
| A1 | 0.25 | 0.35 |
| A2 | 1.20 | REF |
| b | 0.30 | 0.50 |
| D | 4.00 | BSC |
| E | 4.00 | BSC |
| e | 1.00 | BSC |
| S | 0.50 | BSC |

Notes

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