NSBC114EPDP6T5G Series

Preferred Devices

Dual Digital Transistors (BRT)

Complementary Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSBC114EPDP6T5G series, two complementary BRT devices are housed in the SOT−963 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 4 mm, 8000 Units Tape and Reel
- These are Pb−Free Devices
- These are Halide−Free Devices

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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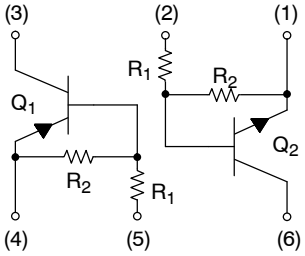
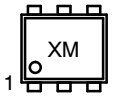


SOT−963
CASE 527AD

MARKING DIAGRAM



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NSBC114EPDP6T5G	SOT−963 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
SINGLE HEATED			
Total Device Dissipation T_A = 25°C (Note 1) Derate above 25°C	P_D	 231 1.9	 mW mW/°C
Thermal Resistance (Note 1) Junction-to-Ambient	$R_{\theta JA}$	540	°C/W
Total Device Dissipation T_A = 25°C (Note 2) Derate above 25°C	P_D	 269 2.2	 mW mW/°C
Thermal Resistance (Note 2) Junction-to-Ambient	$R_{\theta JA}$	464	°C/W
DUAL HEATED (Note 3)			
Total Device Dissipation T_A = 25°C (Note 1) Derate above 25°C	P_D	 339 2.7	 mW mW/°C
Thermal Resistance (Note 1) Junction-to-Ambient	$R_{\theta JA}$	369	°C/W
Total Device Dissipation T_A = 25°C (Note 2) Derate above 25°C	P_D	 408 3.3	 mW mW/°C
Thermal Resistance (Note 2) Junction-to-Ambient	$R_{\theta JA}$	306	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
2. FR−4 @ 500 mm^2, 1 oz. copper traces, still air.
3. Dual heated values assume total power is sum of two equally powered channels.

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking (Clockwise Rotation)	R1 (kΩ)	R2 (kΩ)
NSBC114EPDP6T5G	SOT−963	L	10	10
NSBC124EPDP6T5G	SOT−963	R (90°)	22	22
NSBC144EPDP6T5G	SOT−963	K (180°)	47	47
NSBC114YPDP6T5G	SOT−963	Q (90°)	10	47
NSBC115TPDP6T5G	SOT−963	J (180°)	100	∞
NSBC123TPDP6T5G	SOT−963	A (180°)	2.2	∞
NSBC143EPDP6T5G	SOT−963	V (90°)	4.7	4.7
NSBC143ZPDP6T5G	SOT−963	Y (90°)	4.7	47
NSBC144WPDP6T5G	SOT−963	T (90°)	47	22
NSBC123JPDP6T5G	SOT−963	D (180°)	2.2	47

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted)

TCharacteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current	NSBC114EPDP6T5G	I_{EBO}	–	–	0.5	mAdc
(V_{EB} = 6.0 V, I_C = 0)	NSBC124EPDP6T5G		–	–	0.2	
	NSBC144EPDP5T5G		–	–	0.1	
	NSBC114YPDP6T5G		–	–	0.2	
	NSBC115TPDP6T5G		–	–	0.1	
	NSBC123TPDP6T5G		–	–	4.0	
	NSBC143EPDP6T5G		–	–	1.5	
	NSBC143ZPDP6T5G		–	–	0.18	
	NSBC144WPDP6T5G		–	–	0.13	
	NSBC123JPDP6T5G		–	–	0.2	
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 4) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS (Note 4)						
DC Current Gain	NSBC114EPDP6T5G	h_{FE}	35	60	–	
(V_{CE} = 10 V, I_C = 5.0 mA)	NSBC124EPDP6T5G		60	100	–	
	NSBC144EPDP5T5G		80	140	–	
	NSBC114YPDP6T5G		80	140	–	
	NSBC115TPDP6T5G		160	350	–	
	NSBC123TPDP6T5G		160	350	–	
	NSBC143EPDP6T5G		15	30	–	
	NSBC143ZPDP6T5G		80	200	–	
	NSBC144WPDP6T5G		80	140	–	
	NSBC123JPDP6T5G		80	140	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.3 mA)						
	NSBC114EPDP6T5G		–	–	0.25	
	NSBC124EPDP6T5G		–	–	0.25	
	NSBC144EPDP6T5G		–	–	0.25	
	NSBC114YPDP6T5G		–	–	0.25	
	NSBC144WPDP6T5G		–	–	0.25	
	NSBC123JPDP6T5G		–	–	0.25	
(I_C = 10 mA, I_B = 1 mA)	NSBC115TPDP6T5G		–	–	0.25	
	NSBC143EPDP6T5G		–	–	0.25	
	NSBC143ZPDP6T5G		–	–	0.25	
	NSBC123TPDP6T5G		–	–	0.25	
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)						
	NSBC114EPDP6T5G/NSBC124EPDP6T5G		–	–	0.2	
	NSBC114YPDP6T5G/NSBC123TPDP6T5G		–	–	0.2	
	NSBC143EPDP6T5G/NSBC143ZPDP6T5G		–	–	0.2	
	NSBC123JPDP6T5G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)						
	NSBC144WPDP6T5G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)						
	NSBC144EPDP6T5G/NSBC115TPDP6T5G		–	–	0.2	
Output Voltage (off)		V_{OH}				Vdc
(V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)						
	NSBC114EPDP6T5G/NSBC124EPDP6T5G		4.9	–	–	
	NSBC144EPDP6T5G/NSBC114YPDP6T5		4.9	–	–	
	NSBC143ZPDP6T5G/NSBC144WPDP6T5G		4.9	–	–	
	NSBC123JPDP6T5G		4.9	–	–	
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)						
	NSBC123TPDP6T5G/NSBC115TPDP6T5G		4.9	–	–	
	NSBC143EPDP6T5G		4.9	–	–	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted)

TCharacteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)						
Input Resistor	NSBC114EPDP6T5G	R1	7.0	10	13	kΩ
	NSBC124EPDP6T5G		15.4	22	28.6	
	NSBC144EPDP5T5G		32.9	47	61.1	
	NSBC114YPDP6T5G		7.0	10	13	
	NSBC115TPDP6T5G		70	100	130	
	NSBC123TPDP6T5G		1.54	2.2	2.86	
	NSBC143EPDP6T5G		3.3	4.7	6.1	
	NSBC143ZPDP6T5G		3.3	4.7	6.1	
	NSBC144WPDP6T5G		15.4	47	28.6	
	NSBC123JPDP6T5G		1.54	2.2	2.86	
Resistor Ratio	NSBC114EPDP6T5G	R1/R2	0.8	1.0	1.2	
	NSBC124EPDP6T5G		0.8	1.0	1.2	
	NSBC144EPDP5T5G		0.8	1.0	1.2	
	NSBC114YPDP6T5G		0.17	0.21	0.25	
	NSBC115TPDP6T5G		–	–	–	
	NSBC123TPDP6T5G		–	–	–	
	NSBC143EPDP6T5G		0.8	1.0	1.2	
	NSBC143ZPDP6T5G		0.055	0.1	0.185	
	NSBC144WPDP6T5G		1.7	2.1	2.6	
	NSBC123JPDP6T5G		0.038	0.047	0.056	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114EPDP6 NPN TRANSISTOR

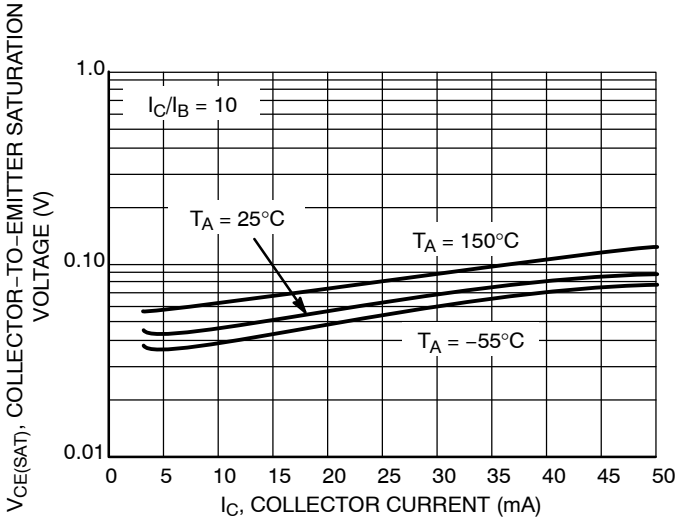


Figure 1. $V_{CE(sat)}$ vs. I_C

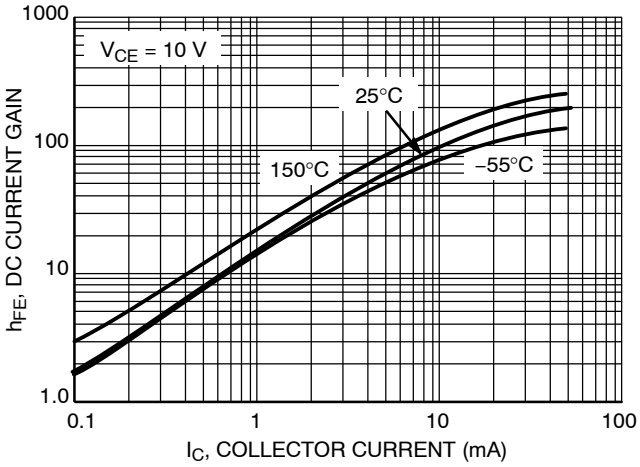


Figure 2. DC Current Gain

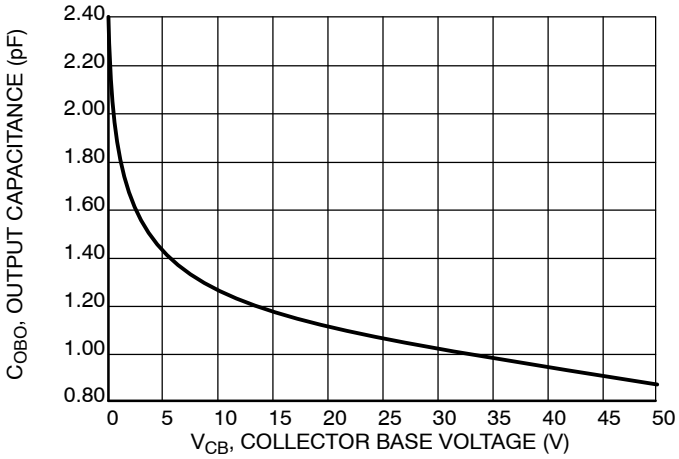


Figure 3. Output Capacitance

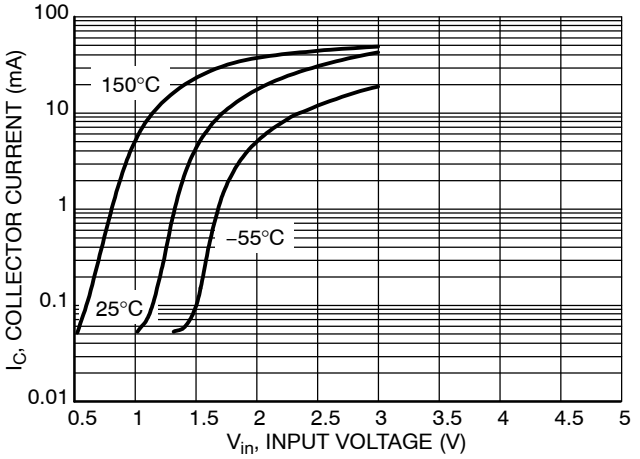


Figure 4. Output Current vs. Input Voltage

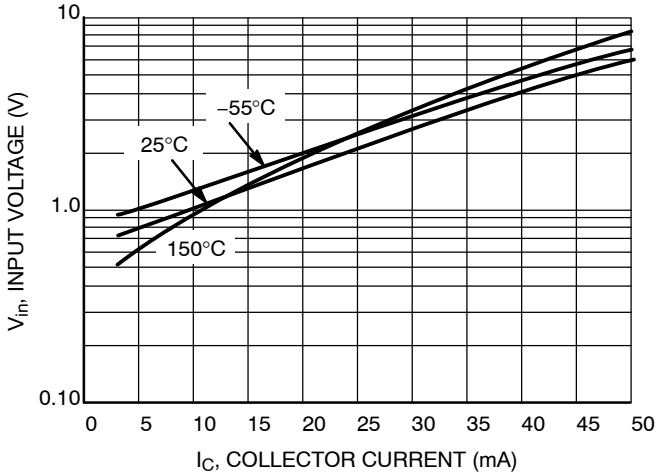


Figure 5. Input Voltage vs. Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114EPDP6 PNP TRANSISTOR

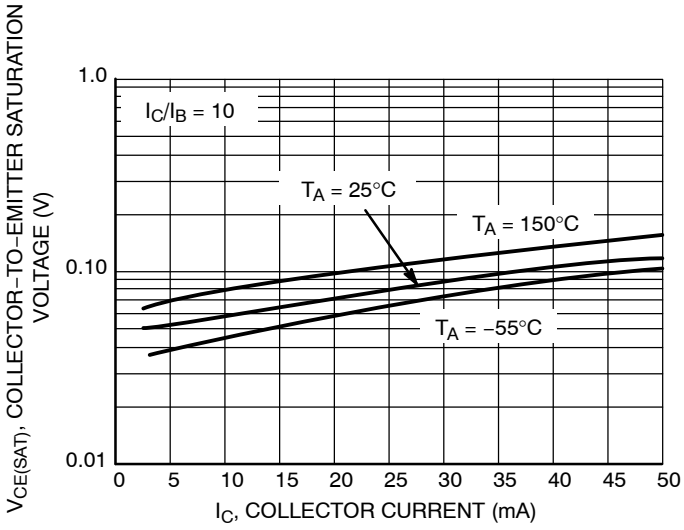


Figure 6. $V_{CE(sat)}$ vs. I_C

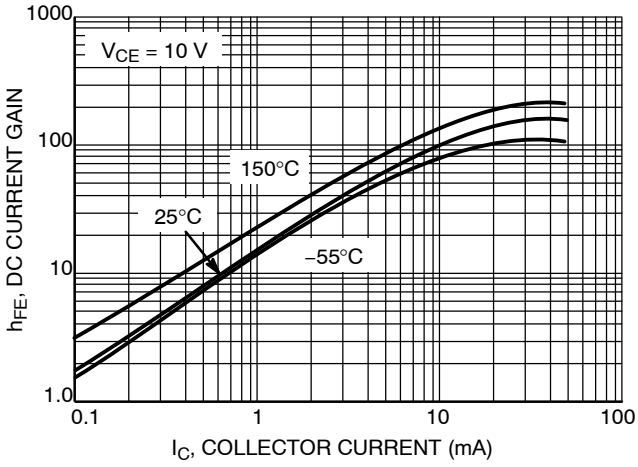


Figure 7. DC Current Gain

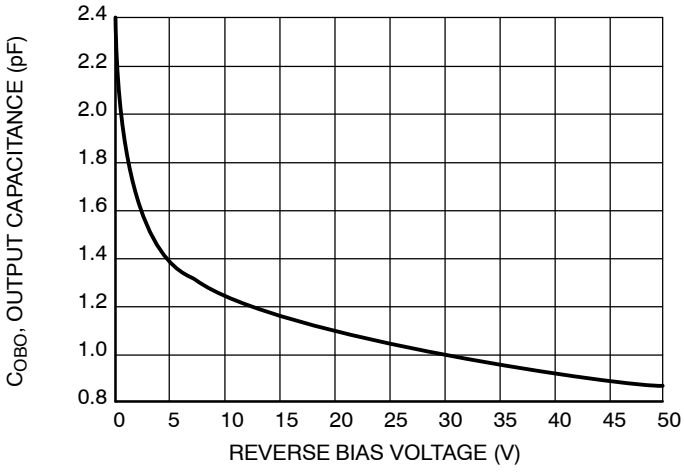


Figure 8. Output Capacitance

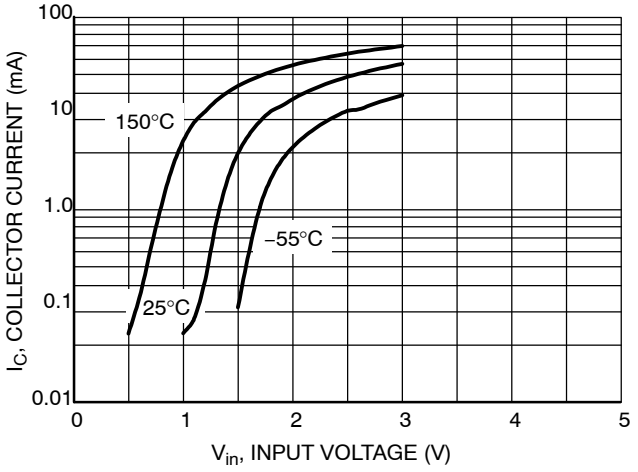


Figure 9. Output Current vs. Input Voltage

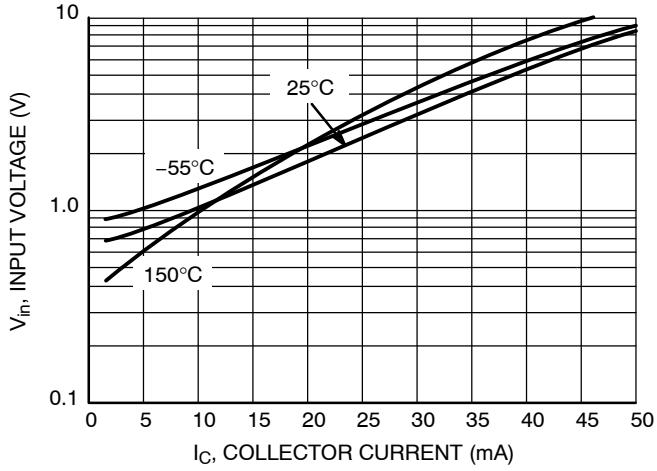
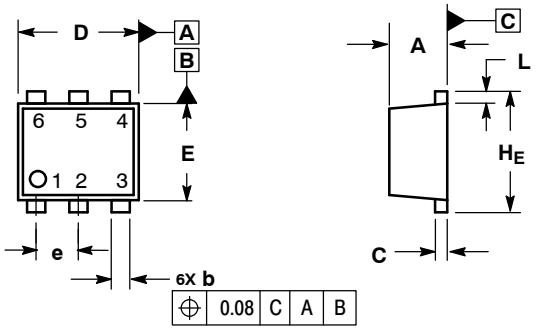


Figure 10. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

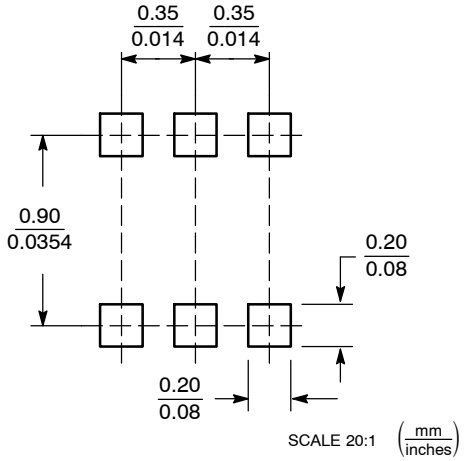
SOT−963
CASE 527AD−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40			
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.07	0.12	0.17	0.003	0.005	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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