EXEL MICROELECTRONICS
Excellence in E²

XL28C64B

8K X 8 CMOS Electrically Erasable PROM
5ms Nonvolatile Write Cycle

FEATURES

■ **Fast Read Access Times**
  — 120ns, 150ns, 200ns and 250ns

■ **Low CMOS Power Consumption**
  — 60mA (Active)
  — 150µA (Standby)

■ **5 Volt-only Operation**
  — Including write

■ **Fast Nonvolatile Write Cycle**
  — Internally latched data and address
  — 120ns byte-load cycle
  — 5ms (max.) nonvolatile write cycle

■ **Self-Timed Writes**
  — Effective 75µs/byte write
  — 64 byte page input buffer
  — Auto-erase before write
  — $\overline{DATA}$ Polling
  — Toggle bit

■ **Software Mode Control**

■ **Automatic Page Write Mode**
  — 64 byte page size
  — 5ms page write time

■ **On-chip Inadvertent Write Protection**

■ **10,000 Rewrites per Byte**

■ **10 Year Secure Data Retention**

■ **ESD Protected to 2000V**
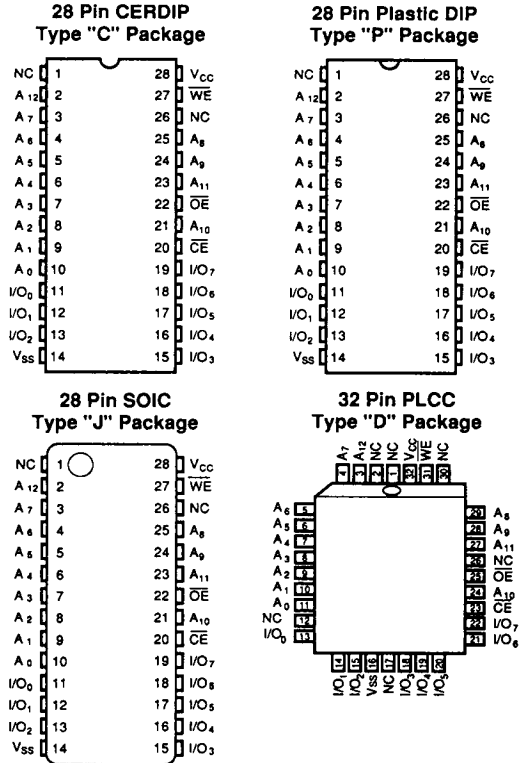
OVERVIEW

The XL28C64B is a full-featured, 8K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 64K devices, but offers improved speed and power efficiency. Read access times can be as low as 120ns; standby current, less than 200µA. It features a page-wide input buffer and improved protection against inadvertent writes. Operating modes function from a single 5V power supply, and the XL28C64B is manufactured with EXEL's proven double-metal, 1.4µ CMOS process.

PIN CONFIGURATIONS

28 Pin CERDIP Type "C" Package

NC	1		28	V_{CC}
A_{12}	2		27	$\overline{WE}$
A_7	3		26	NC
A_6	4		25	A_8
A_5	5		24	A_9
A_4	6		23	A_{11}
A_3	7		22	$\overline{OE}$
A_2	8		21	A_{10}
A_1	9		20	$\overline{CE}$
A_0	10		19	I/O_7
I/O_0	11		18	I/O_6
I/O_1	12		17	I/O_5
I/O_2	13		16	I/O_4
V_{SS}	14		15	I/O_3

28 Pin Plastic DIP Type "P" Package

NC	1		28	V_{CC}
A_{12}	2		27	$\overline{WE}$
A_7	3		26	NC
A_6	4		25	A_8
A_5	5		24	A_9
A_4	6		23	A_{11}
A_3	7		22	$\overline{OE}$
A_2	8		21	A_{10}
A_1	9		20	$\overline{CE}$
A_0	10		19	I/O_7
I/O_0	11		18	I/O_6
I/O_1	12		17	I/O_5
I/O_2	13		16	I/O_4
V_{SS}	14		15	I/O_3

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28 Pin SOIC Type "J" Package

NC	1		28	V_{CC}
A_{12}	2		27	$\overline{WE}$
A_7	3		26	NC
A_6	4		25	A_8
A_5	5		24	A_9
A_4	6		23	A_{11}
A_3	7		22	$\overline{OE}$
A_2	8		21	A_{10}
A_1	9		20	$\overline{CE}$
A_0	10		19	I/O_7
I/O_0	11		18	I/O_6
I/O_1	12		17	I/O_5
I/O_2	13		16	I/O_4
V_{SS}	14		15	I/O_3

32 Pin PLCC Type "D" Package

Top pins: A_7, A_{12}, NC, NC, $\overline{WE}$, NC

Left side: A_6, A_5, A_4, A_3, A_2, A_1, A_0, NC, I/O_0

Right side: A_8, A_9, A_{11}, NC, $\overline{OE}$, A_{10}, $\overline{CE}$, I/O_7, I/O_6

Bottom pins: I/O_1, I/O_2, V_{SS}, NC, I/O_3, I/O_4, I/O_5

PIN NAMES

A_0-A_{12}	Address Inputs
I/O_0- I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM
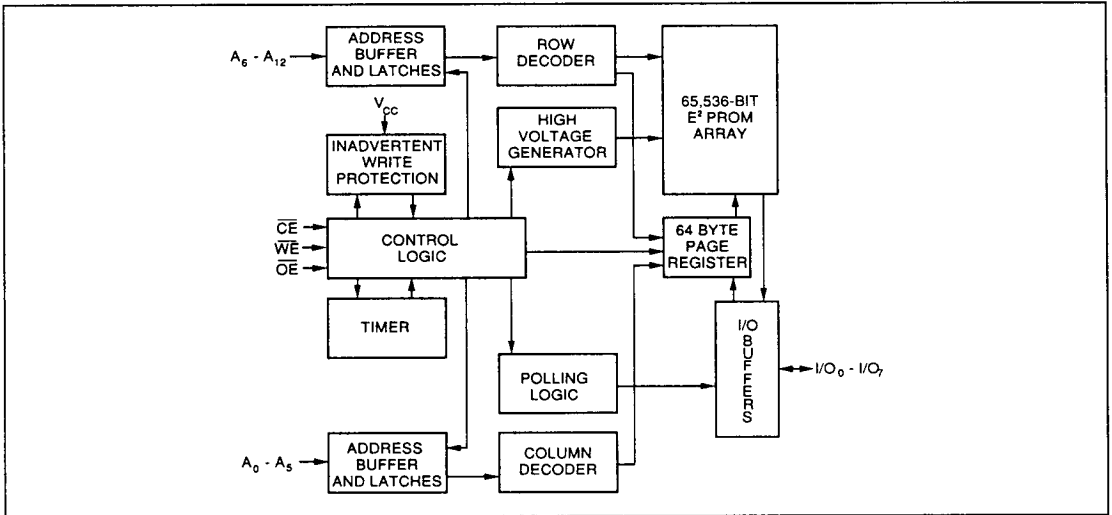
The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and supplemental inadvertent write protection circuitry. It fits into standard SRAM sockets and responds to typical SRAM write commands.

The fully-automatic 64-byte page-write allows the entire memory to be programmed in less than 0.65 sec. Internal latches, for address and data, free the system bus during the 5ms self-timed, nonvolatile write period. Moreover, the byte-load cycle time matches the read access time, adding to system performance.

Inadvertent writes are inhibited by a wide range of protections built into the XL28C64B. A low V_{CC} lockout feature disables nonvolatile write cycles when V_{CC} drops below 3.5V (V_{WI}) (typical). Additionally, the XL28C64B features power-on reset and noise protected $\overline{WE}$.

The XL28C64B is compatible with existing 64K E^2PROMs—both pinout and operating modes conform to industry standards. This compatibility extends to higher and lower density E^2PROMs as well.

APPLICATIONS

The nonvolatile storage in the XL28C64B replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in telephones and facsimile machines. The XL28C64B is ideal in applications that are self-adapting, such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C64B is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of over 81 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard user-operating modes for the XL28C64B. Chip erase (typically executed during test procedures) requires a higher supply voltage on the $\overline{OE}$ input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL28C64B by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the latter of either the time when the controlling line goes LOW ($\overline{CE}$ or $\overline{OE}$), or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle.

Write Mode

The XL28C64B uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent nonvolatile write cycle transfers this data in the page-buffer to the E^2PROM array without user intervention.

The XL28C64B contains (128) 64-byte pages. Address lines A_6-A_{12} identify the page; lines A_0-A_5 identify the byte within the page. All bytes written within one nonvolatile write cycle must be on the same page (A_6-A_{12} must remain unchanged). Any number of the 64 bytes in the page can be written or re-written, in any order; the last data written to any given byte when the nonvolatile write cycle begins is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to initiate the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. An internal byte-load timer is started on the falling edge of the controlling line. The timer provides a 100μs window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period.

When the byte-load timer times out, additional external byte-load cycles are ignored and data is automatically transferred from the page buffer to the E^2PROM array through an internally managed nonvolatile write cycle.

Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The high voltage cycle is immune to any overlapping control pin activity.

An internal write-flag is set on the first byte-load of each write cycle. Data pins remain in a high impedance state except during a byte-load (when they contain the forced input data) or during a $\overline{DATA}$ polling read (see below). When the high voltage cycle is completed, the write-flag is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Standby Mode

Whenever $\overline{CE}$ is brought HIGH, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 200μA with CMOS level inputs.

Chip Erase — High Voltage Mode

The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command, but in this case, the data on the I/O pins is ignored. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

DEVICE OPERATION—SOFTWARE CONTROL

Under software control, the XL28C64B offers 5V-only data protection and chip erase. Software control is accomplished by byte-load sequences involving specific address and data patterns.

Short command sequences require three byte-loads; long sequences require six byte-loads. Whenever one of these sequences is recognized in a write operation, it is executed as a software command sequence, and any preceding byte-loads are lost.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⎍	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⎍	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In = X	Active
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	$\overline{DATA}$ Polling	$\overline{D_7}$	Active
X	V_{IL}	X	Write Inhibit	X	Active

*Contact EXEL for details.

These address and data patterns could conceivably occur in a normal application. However, the protocol utilizes differing page addresses within one write cycle — a practice that is illegal in standard write operations.

Chip Erase Cycle

This software command sequence activates the standard chip erase, but without the high voltage input on the $\overline{OE}$ pin. Contact EXEL technical support for details.

Set Data Protection Mode (See Figure 1)

This software command sequence disables the high voltage cycle for standard writes (those controlled by the enable lines). Each set-data-protect command can be followed by data for one page of the E²PROM array. Thereafter, standard writes are disabled, and can be enabled only by a disable-data-protect command. However, additional pages can be written by the set-data-protect command.

Set Data Protect Software Command Sequence:

Byte-load	A_{12}-A_0	I/O_7-I/O_0
1	1555 (hex)	AA (hex)
2	0AAA (hex)	55 (hex)
3	1555 (hex)	A0 (hex)

When this command is recognized, the part remains in write mode. Any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting a nonvolatile data protect bit. If the data protect bit was already set—by a previous set-data-protect command—it remains set. If a power failure interrupts the operation, neither the data nor the protect bit is written.

Setting the data protect bit inhibits only the high voltage cycles of standard writes (those controlled by the enable lines); byte-load cycles are still accepted. When the byte-load timer expires, the part skips the high voltage cycle and becomes accessible to the standard read mode.

Because the data-protect-status bit is a nonvolatile E² element, protect mode status is maintained during power off.

Disable Data Protection Mode

This software command sequence re-enables the high voltage cycle of the standard write (see Figure 2). Each disable-data-protect command can be accompanied by data for one page of the E²PROM. Standard writes are then enabled, until disabled by a subsequent set-data-protect command.

Disable Data Protect Software Command Sequence:

Byte-load	A_{12}-A_0	I/O_7-I/O_0
1	1555 (hex)	AA (hex)
2	0AAA (hex)	55 (hex)
3	1555 (hex)	80 (hex)
4	1555 (hex)	AA (hex)
5	0AAA (hex)	55 (hex)
6	1555 (hex)	20 (hex)

The six byte-loads specifying this command leave the part in write mode; any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting the nonvolatile data protection. If the data protection was already disabled (by a previous disable-data-protect command), it remains disabled. If a power failure interrupts the operation, neither the data nor the data protection is written. Because the data protect status bit is a nonvolatile E² element, data protection mode status is maintained during power off.

MONITORING DEVICE STATUS

Because the byte-load timer and its high voltage cycle are completely under the control of the XL28C64B, a status register allows the host system to monitor device status.

Status Register

Any read performed during the nonvolatile write cycle is interpreted as a status register read. (Reading the status register has no effect on the byte-load timer, byte-load flags, high voltage cycle or the contents of the page buffer.)

The status of a write operation is monitored in one of two ways; Toggle Polling or $\overline{DATA}$ Polling. While the nonvolatile write cycle is in progress, O_6 will toggle between 0 and 1 on successive reads; O_7 will hold the complement of bit 7 of the last byte loaded. When the write-latch is reset, the write operation is complete. O_6 and O_7 become bits 6 and 7 of the actual byte location. Bit 6 will no longer toggle; bit 7 will no longer be a complement.

While the write cycle is in progress, there is additional information available from the status register, as follows:

Bits 0 and 1:	Reserved for use by factory
Bit 2:	Always 0
Bit 3:	1 means data protect feature is enabled
	0 means data protect feature is disabled
Bit 4:	Always 1
Bit 5:	Reserved for use by factory
Bit 6:	Used in Toggle polling
Bit 7:	Used in $\overline{DATA}$ Polling

Write Sequence for **Setting**
Software Data Protection
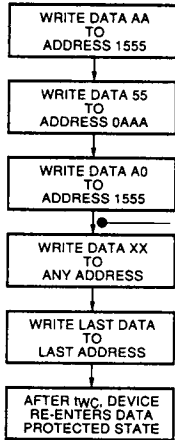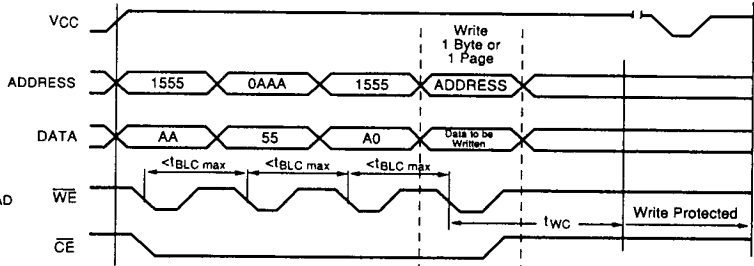
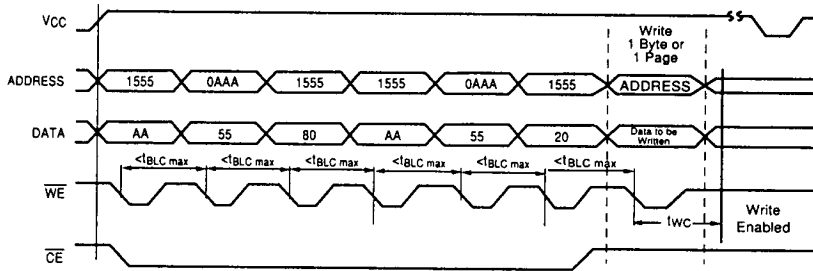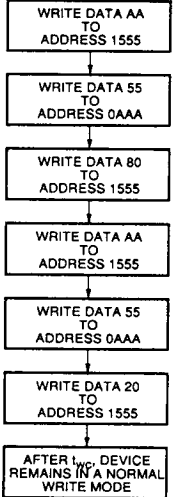**FIGURE 1. WRITE SEQUENCE FOR SETTING SOFTWARE DATA PROTECTION**

Write Sequence for **Disabling**
Software Data Protection

FIGURE 2. WRITE SEQUENCE FOR DISABLING SOFTWARE DATA PROTECTION

$\overline{\text{DATA}}$ Polling

The XL28C64B provides a feature named $\overline{\text{DATA}}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C64B is busy executing its nonvolatile write cycle will be interpreted as a $\overline{\text{DATA}}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{\text{DATA}}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or the nonvolatile cycle timing.

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL28C64B. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C64B. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers output the contents of the status register, during a read cycle. I/O$_7$ is set to output the complement of the value of the MSB of the last byte written to the XL28C64B when a read command is asserted.

$\overline{\text{DATA}}$ POLLING SUBROUTINE
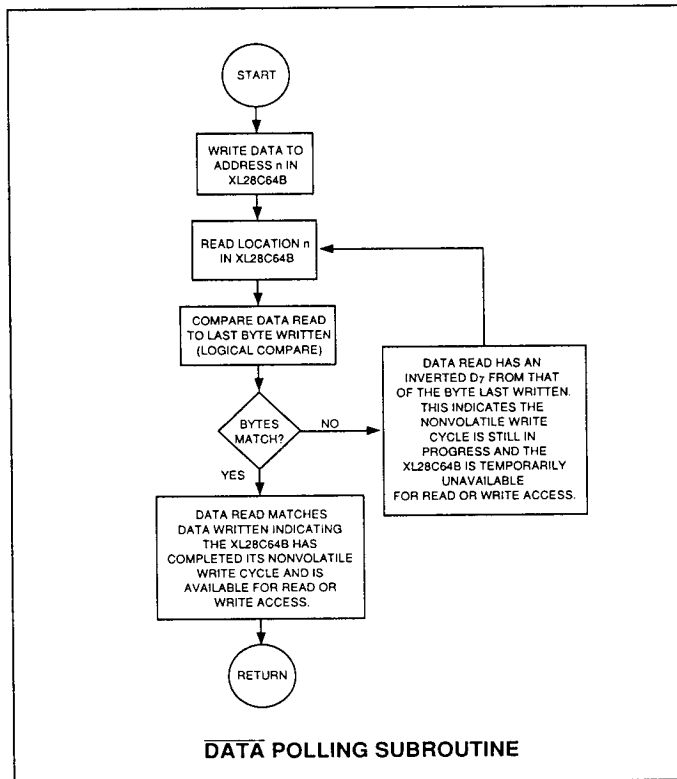
The procedure is quite simple. The system simply reads the location last written to in the XL28C64B and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C64B is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to await the 5ms (max.) period specified, and enabling accelerated device loading operations.

WRITE PROTECT MECHANISMS

The XL28C64B features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise.

$\overline{OE}$ Write Inhibit

If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

Vcc Lockout

The XL28C64B has a specialized power supply monitor circuit integrated to protect the device from inadvertent write commands asserted by the system during low V_{CC} conditions. This circuitry constantly evaluates the power supply voltage level applied to the XL28C64B and actively inhibits the initiation of nonvolatile write cycles if the applied supply voltage falls below V_{WI}. This circuitry does not abort nor affect nonvolatile write cycles already in progress, yet inhibits new cycles from being initiated.

Power-Up Write Enable Delay

At power on, operation is inhibited until V_{CC} is stable and sufficiently high. Write operations are inhibited until 1ms after V_{CC} reaches 3.0V to allow the system to stabilize while blocking potential inadvertent write commands.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

Data Protection Mode (Software Controlled)

The XL28C64B can be placed in a write-disabled mode through software control.

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ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) .... 300°C
Supply Voltage .... 0 to 6.5V
Voltage on Any Pin* .... -1.0 to +7.0V
Voltage on $\overline{OE}$ Pin* .... -1.0 to +15.0V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C64B or -40°C to +85°C for the XLE28C64B, V_{CC} = 5V ±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	Vcc Current — Active (TTL)	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{WE} = V_{IH}$ I/O's = open A_0-A_{12} toggling at 5MHz		60	mA
I_{SB}	Vcc Current — Standby (TTL)	$\overline{CE} = \overline{WE} = V_{IH}$ $\overline{OE} = V_{IL}$ I/O's = open A_0-A_{12} = Vcc		2	mA
I_{SBC}	Vcc Current — Standby (CMOS)	$\overline{CE} = \overline{WE}$ V cc-.2V $\overline{OE} = V$ ss+0.2V I/O's = open A_0-A_{12} = Vcc		150	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc		10	µA
I_{LO}	Output Leakage — Standby	V_{OUT} = GND to Vcc $\overline{CE} = V_{IH}$		10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -10µA	2.4 Vcc-0.1		V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A = 25°C, f = 1.0MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS
READ CYCLE (See Figures 3 and 4)
T_A=0°C to +70°C for the XLS28C64B or -40°C to +85°C for the XLE28C64B, V_{CC}=5V±10%
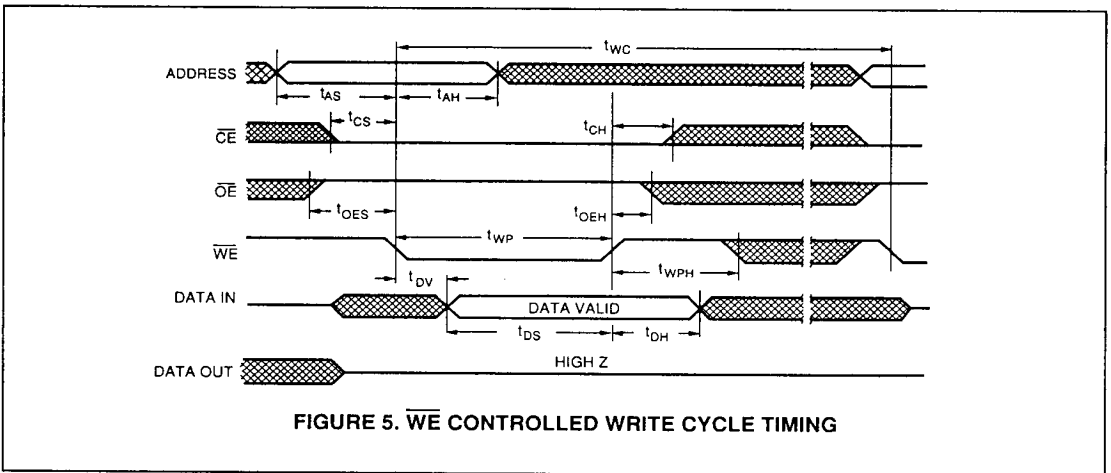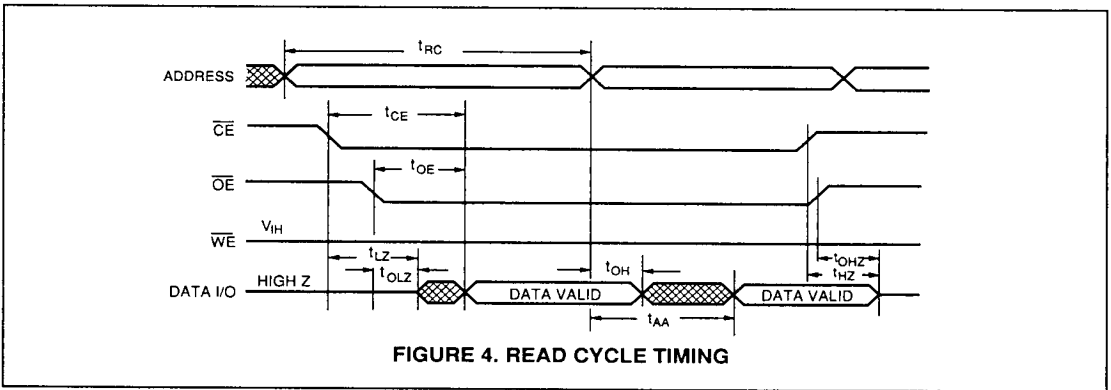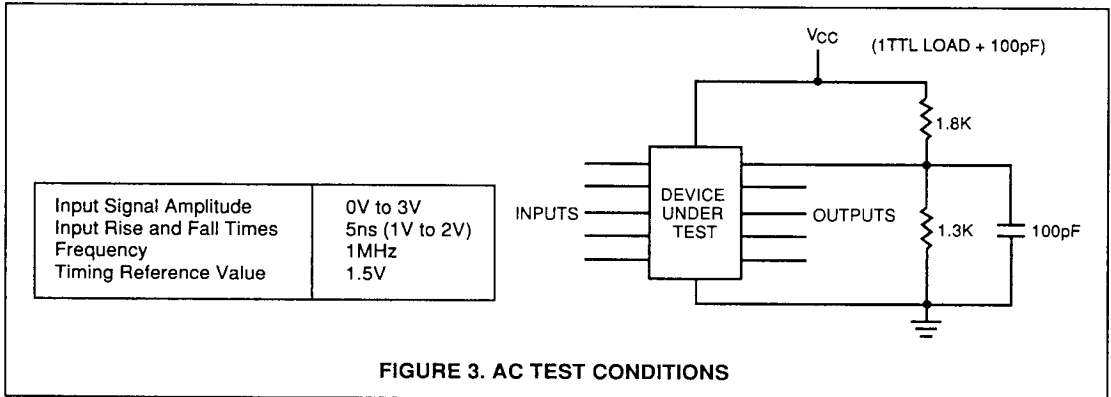
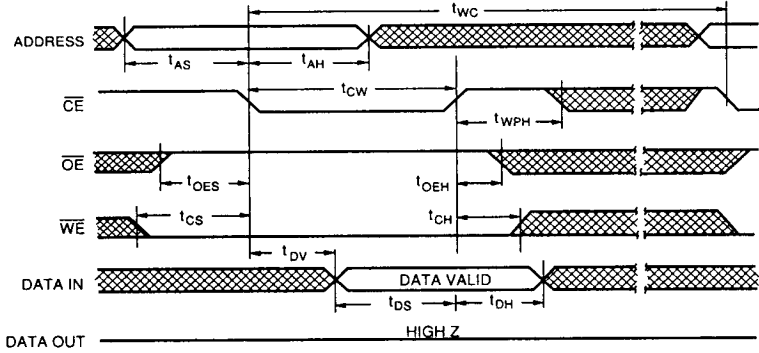| Symbol	Test	XL28C64B-120		XL28C64B-150		XL28C64B-200		XL28C64B-250		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tRC	Read Cycle Time	120		150		200		250		ns
tAA	Address Access Time		120		150		200		250	ns
tCE	Chip Enable Access Time		120		150		200		250	ns
tOE	Output Enable Access Time		50		60		75		100	ns
tLZ	Chip Enable to Output in Low Z	0		0		0		0		ns
tHZ	Chip Disable to Output in High Z	0	50	0	50	0	50	0	50	ns
tOLZ	Output Enable to Output in Low Z	0		0		0		0		ns
tOHZ	Output Disable to Output in High Z	0	50	0	50	0	50	0	50	ns
tOH	Output Hold from Address Change	15		15		15		15		ns

WRITE CYCLE (See Figures 5, 6 and 7)
T_A=0°C to +70°C for the XLS28C64B or -40°C to +85°C for the XLE28C64B, V_{CC}=5V±10%

Symbol	Test	Min.	Max.	Units
tWC	Write Cycle Time		5	ms
tBLC	Byte Load Cycle	.120	100	µs
tAS	Address Setup Time	0		ns
tAH	Address Hold Time	35		ns
tCS	Write Setup Time	0		ns
tCH	Write Hold Time	0		ns
tCW	Chip Enable Pulse Width	50		ns
tOES	Output Enable Setup Time	5		ns
tOEH	Output Enable Hold Time	5		ns
tWP	Write Enable Pulse Width	70		ns
tWPH	Write Pulse Width High	50		ns
tDS	Data Setup Time	30		ns
tDH	Data Hold Time	0		ns
tDV	Data Valid Time		1	µs
tINIT	Power-up Initialization Period		20	ms

FIGURE 3. AC TEST CONDITIONS

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 4. READ CYCLE TIMING

FIGURE 5. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

3-84

FIGURE 6. CE CONTROLLED WRITE CYCLE TIMING

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P DCTS
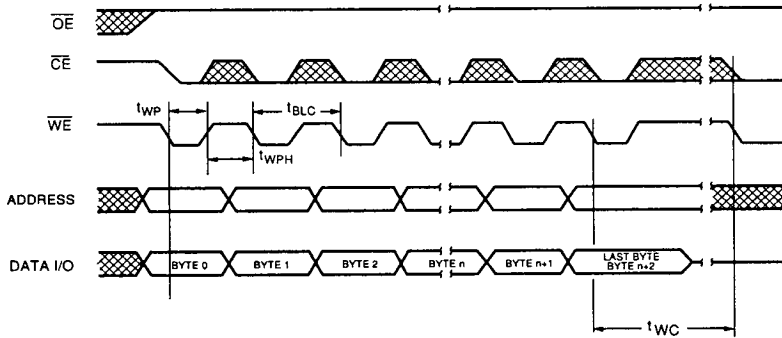
FIGURE 7. PAGE MODE WRITE CYCLE TIMING
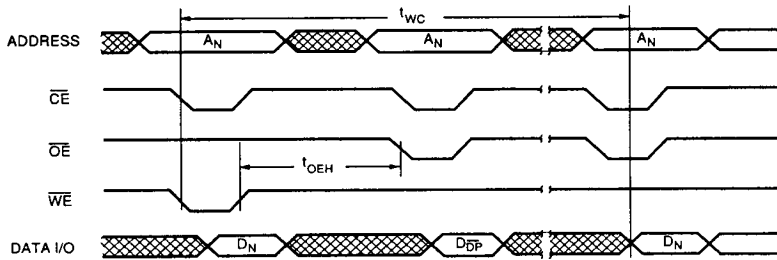
FIGURE 8. DATA POLLING TIMING