National Semiconductor

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T-45-07

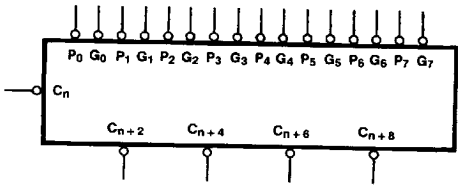
100179
Carry Lookahead Generator

General Description

The 100179 is a high-speed Carry Lookahead Generator intended for use with the 100180 6-bit fast Adder and the 100181 4-bit ALU. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

Logic Symbol

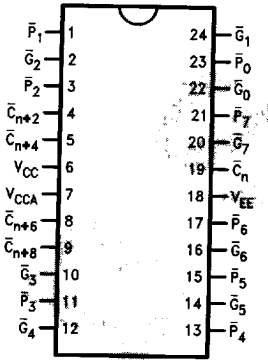


TL/F/9871–3

Pin Names	Description
$\overline{C}_n$	Carry Input (Active LOW)
$\overline{P}_0$–$\overline{P}_7$	Carry Propogate Inputs (Active LOW)
$\overline{G}_0$–$\overline{G}_7$	Carry Generate Inputs (Active LOW)
$\overline{C}_{n+2}$, $\overline{C}_{n+4}$ $\overline{C}_{n+6}$, $\overline{C}_{n+8}$	Carry Outputs

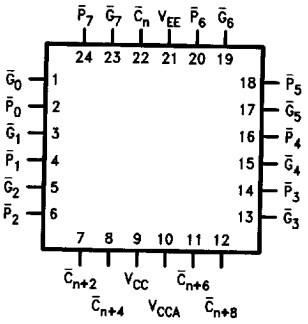
Connection Diagrams

24-Pin DIP



TL/F/9871–1

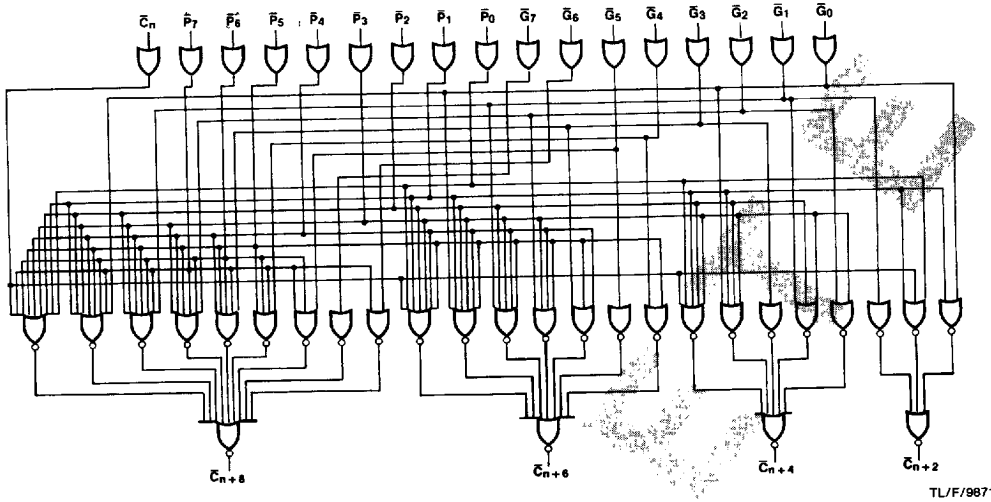
24-Pin Quad Cerpak



TL/F/9871–2

100179

Logic Diagram



TL/F/9871–5

Truth Tables

$\overline{C}_{n+2}$ Output

Inputs					Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{C}_{n+2}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

$\overline{C}_{n+2} = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

$\overline{C}_{n+4}$ Output

Inputs									Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{C}_{n+4}$
X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	L	X	X	L	L
X	X	X	L	X	X	L	X	L	L
X	L	X	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	L
All other combinations									H

$\overline{C}_{n+4} = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$
$\bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

Truth Tables (Continued)

$\overline{C}_{n+6}$ Output

Inputs												Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{G}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{C}_{n+6}$
X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations													H

$$\overline{C}_{n+6} = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

$\overline{C}_{n+8}$ Output

Inputs																Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{G}_6$	$\overline{P}_6$	$\overline{G}_7$	$\overline{P}_7$	$\overline{C}_{n+8}$
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations																	H

$$\overline{C}_{n+8} = \overline{G}_7 \bullet (\overline{P}_7 + \overline{G}_6) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

100179

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current $\overline{C}_N$, $\overline{G}_0$–$\overline{G}_7$ $\overline{P}_0$–$\overline{P}_7$			250 340	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−220	−150	−100	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

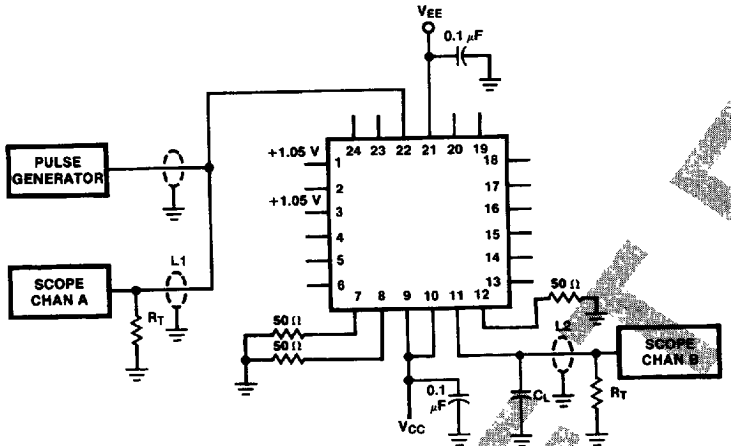
Symbol	Parameter	T_C = 0°C		T_C = +25°		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.90	1.10	2.90	1.10	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.70	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

100179

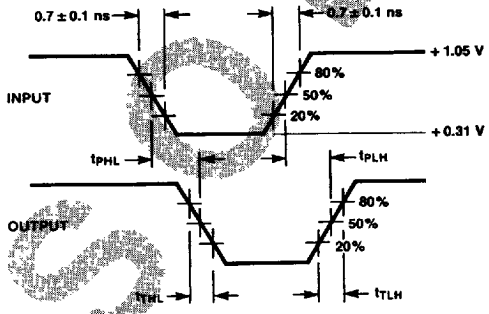


TL/F/9871–6

FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

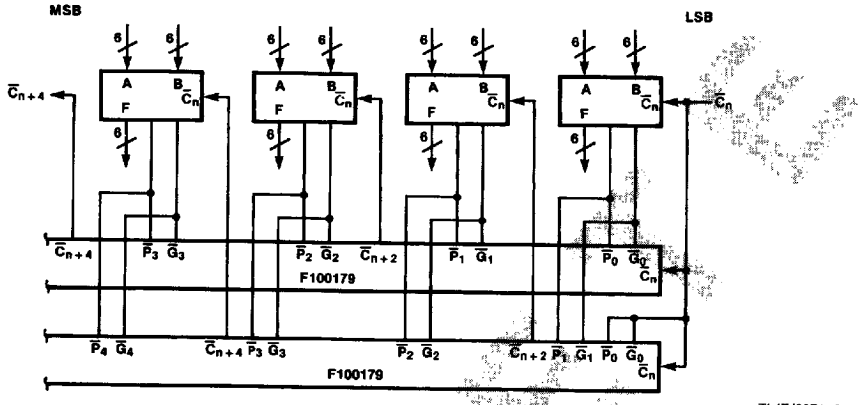


TL/F/9871–6

FIGURE 2. Propagation Delay and Transition Times

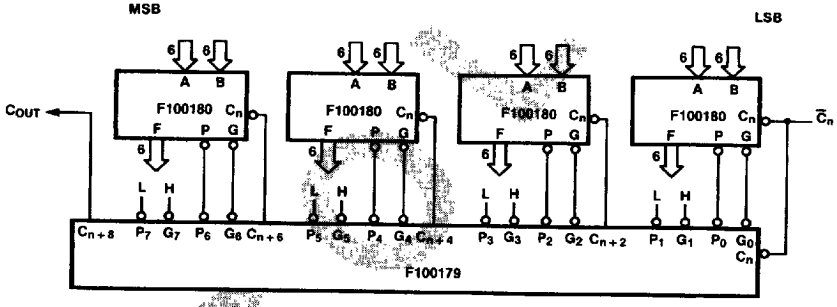
Applications

Fast Adder and Carry Lookahead



TL/F/9871–8

24-Bit Adder Using One Carry Lookahead



TL/F/9871–9