T-62-11

CALMOS™

CA2862

POWER SUPPLY SUPERVISORY CIRCUIT

- **2.5V precision reference**
- **Three separate window comparators**
- **Four 30mA open-collector drivers**
- **Hold time selected by external RC**
- **Wide input voltage range: -0.3V to 16V**
- **Wide supply range : 4.3V to 16V**

The CA2862 contains all the functions required to monitor three power supplies for over and under voltage transients. Narrow glitches can be captured and held for user-definable time periods. The major application for the CA2862 is triple over-/under-voltage transient supervision.

The CA2862 contains three window comparators with user-selectable switch points, a precision silicon bandgap voltage reference, a hold comparator and four CMOS/TTL compatible output drivers. When one of the window comparators detects a glitch, the latch is set, the hold capacitor is discharged, the latch sets four output drivers low (disable mode) . After the glitch disappears the capacitor charges until the hold comparator switchpoint is reached. The output drivers then switch high (enable mode) .

The internal precision reference is accurate to 1% which, combined with offsets, yields an overall device accuracy of 1.25%. During initial power-on, the window comparators are over-ridden and the output drivers are gated low for VCC voltages between 1.8V and 3.3V.

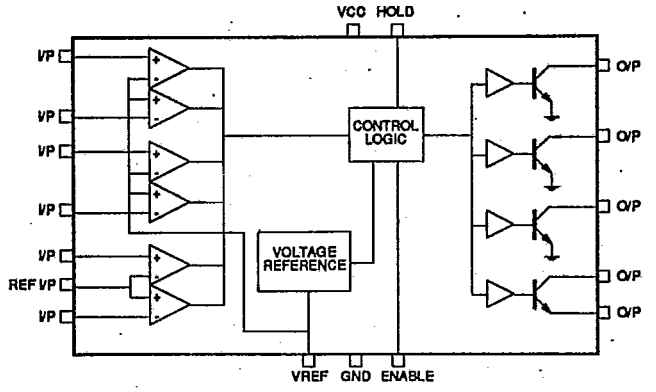

Figure 1 : CA2862 BLOCK DIAGRAM

1	GND	9	C1A
2	PWR GND	10	C1B
3	OUT4	11	C2A
4	OUT3	12	C2B
5	OUT2	13	C3A
6	OUT1	14	C3B
7	HOLD	15	C3R
8	VREF	16	VCC

CA2862 M-16-1

1	GND	9	C1A
2	EN	10	C1B
3	OUT4	11	C2A
4	OUT3	12	C2B
5	OUT2	13	C3A
6	OUT1	14	C3B
7	HOLD	15	C3R
8	VREF	16	VCC

CA2862 M-16-2

1	GND	9	C1A
2	OUT4E	10	C1B
3	OUT4C	11	C2A
4	OUT3	12	C2B
5	OUT2	13	C3A
6	OUT1	14	C3B
7	HOLD	15	C3R
8	VREF	16	VCC

CA2862 M-16-3

Figure 2 : PIN CONFIGURATION OPTIONS FOR THE CA2862

Table 1 : ELECTRICAL CHARACTERISTICS (T_A = 23°C, VCC = 12V)

Parameter	Condition		Min	Typ	Max	Units
VCC Supply Current	Outputs low I_L = 8mA			4.0	8.0	mA
	–20 to +85°C				10.0	mA
	Outputs high			1.8	3.0	mA
	–20 to +85°C				5.0	mA
VCC Supply Voltage Range			4.3		16	V
Window Comparators	V_{IO} Input offset voltage	with respect to V_{REF}		1.0	5.0	mV
	I_{IB} Input bias current			100	500	nA
	Minimum glitch width	100mV overdrive		300	800	ns
	C3 comparator common mode input voltage range		–0.3		V_{CC}–2	V
Hold Comparator	Hold switchpoint			1.25		V
	Discharge switch	V_{OL} @ 100µA		50	200	mV
	I_{IB} Input bias current			50	250	nA
	Hold resistor range	–20° to +85°C	20		200	kΩ
2.5V Bandgap Reference	Output voltage	T_A = 23°C, no load	2.48	2.5	2.52	V
		T_A = –20° to +85°C, no load	2.45		2.55	V
	Output current	Source	1.0			mA
		Sink	–100			µA
	Input regulation	V_S = 4.3V to 16V		0.5	5.0	mV
	Output regulation	I_O = 0 to 1mA		4.0	12.0	mV
	Temperature stability	Average (–20° to +85°C)		50		ppm/°C
Output Drivers	V_{OL}	@8mA			0.4	V
		@25mA			0.8	V
	Output leakage I_{OH}	V_{OH} = 16V			5	µA
	Differential propagation					
	delay	R_{PULLUP} = 10KΩ, Cload = 10pF			10	ns
Enable	I_{IL}	V_L = 0.4V			–75	µA
	I_{IH}	V_H = 2.7V			1.0	µA
	V_{IL} switchpoint				0.8	V
	V_{IH} switchpoint		2.0			V

Note: Operating temperature range is: –20° to +85 °C

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Figure 3 : CA2862 TIMING DIAGRAM

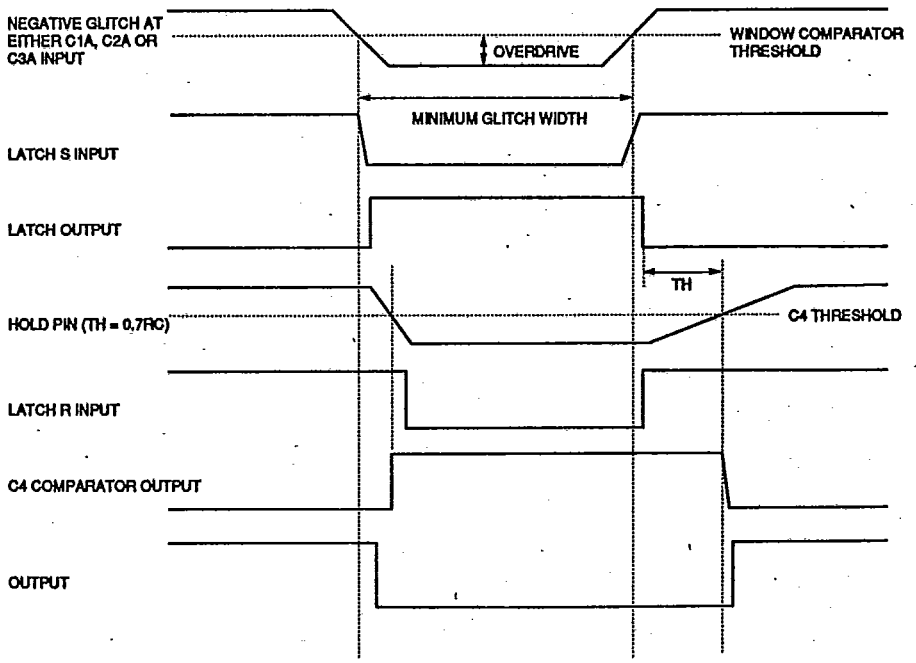

Table 2 : ABSOLUTE MAXIMUM RATINGS

Comparator input voltage range	−0.3 V to VCC
Supply voltage (VCC)	20 V
Storage temperature range	−65° to +150°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

Voltage Reference

The bandgap reference is internally trimmed to an accuracy of ±1% @ 25°C. The output voltage is essentially independent of supply voltage and has a typical temperature coefficient of 50 ppm per °C.

The reference can source 1mA and sink 0.1mA. A bypass capacitor may be required in some applications. Values up to 0.47µF are acceptable.

The reference disables the output (held low) until the supply voltage exceeds 3.3V.

Window Comparators

The device contains three identical window comparators. Two comparators are referenced to 2.5V internally. The third comparator's reference pin is external. This allows for negative supply sensing. An application schematic diagram is shown in Figure 4.

When an out-of-spec (user-defined) supply transient occurs in either the positive or negative direction, the comparator sets an internal latch. The latch starts to discharge the hold pin and bypasses the hold comparator to directly switch the four output drivers low (OK = 1, Fault = 0).

The response time, which includes latch setup times, is less than 1µs with typical times in the 300ns range.

Input offset voltages are typically less than 1mV. The pin configuration of CA2862 M-16 option 1 (see Figure 2) is recommended for high drive current applications since separate power ground and reference ground connections minimize offsets caused by internal load related IR drops.

Hold Comparator

The latch quickly discharges the hold pin below the hold comparator switchpoint of 1.25V, causing the hold comparator to also gate the outputs low. When the hold pin goes below 0.2V, the latch is reset. The pin is released only if the latch has been reset and the input transient has gone away. The hold capacitor will then be charged through R_{HOLD}, normally connected to V_{REF}. Outputs remain low until the hold pin exceeds 1.25V. The hold time is approximately $0.7 \times R_{HOLD} \times C_{HOLD}$. The range of hold resistors recommended will minimize errors due to comparator input bias currents and latch saturation voltages.

Enable

The CA2862 M-16 option 2 pin configuration (Figure 2) has an enable input which allows the outputs to be disabled (low) when held low. The input is Schottky TTL and CMOS compatible.

Output Driver

The output drivers are high for a no fault condition and low for a fault condition. All four output drivers are open collector and can sink up to 30mA each. The outputs may be pulled up to supply not exceeding 16V.

Internal feedback detects driver transistor saturation and removes excess base drive, minimizing supply currents.

The CA2862 M-16 option 3 pin configuration (Figure 2) has outputs OUT4C and OUT4E emitter bonded out to allow for voltage follower applications.

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APPLICATION NOTES

A typical application is illustrated in Figure 4:

- Comparators C1 and C2 are monitoring V_X and V_Y positive supplies. C3 is monitoring V_Z a negative supply, and is referenced to 1.25V.
- V_{REF} is decoupled with a 0.1µf capacitor to minimize false switching caused by noise. The device is supplied from the higher of V_X or V_Y. If one of the supplies drops out, the remaining supply will continue to operate the device.
- OUT1, OUT2 and OUT3 drive three separate lines pulled up by 10KΩ resistors to two separate power supplies. These can sink up to 30mA and therefore could also drive relays.
- OUT4 is connected as an emitter follower as per the CA2862 M–16–3 option. In the other two options, this emitter would be internally tied to ground.
- The enable input is available in CA2862 M–16–2 option.

C1 and C2 Comparators (referenced to 2.5V internal)

High supply voltage detect limit:

$$V_{CCH} = 2.5V\left(\frac{R1+R2+R3}{R3}\right)$$

Low supply voltage detect limit:

$$V_{CCL} = 2.5V\left(\frac{R1+R2+R3}{R2+R3}\right)$$

C3 Comparator (user selected reference)

High supply voltage detect limit:

$$|V_{CCH}| = V_R\left(\frac{R2+R3}{R1}\right) - V_{C3R}\left(\frac{R1+R2+R3}{R1}\right)$$

Low supply voltage detect limit:

$$|V_{CCL}| = V_R\left(\frac{R3}{R1+R2}\right) - V_{C3R}\left(\frac{R1+R2+R3}{R1+R2}\right)$$

Hold Time

Hold Time = 0.7 RC

if R = 100KΩ and C = 0.1µF

then Hold Time = (0.7)(100KΩ)(0.1µf) = 7msec

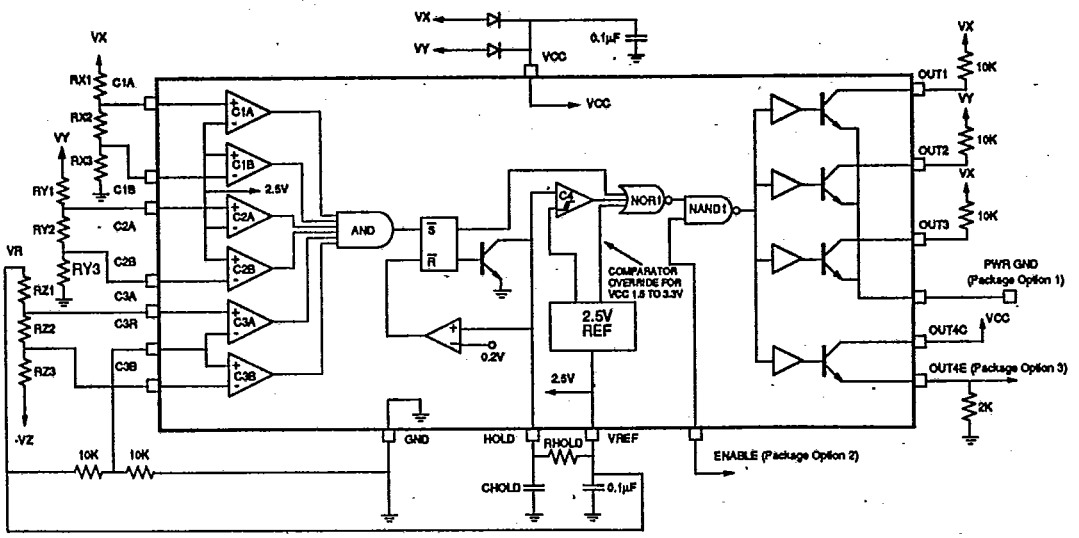

Figure 4 : CA2862 APPLICATION SCHEMATIC