CY7C189
CY7C190

CYPRESS SEMICONDUCTOR

16 x 4 Static R/W RAM

Features

- **Fully decoded, 16 word x 4-bit high-speed CMOS RAMs**
- **Inverting outputs CY7C189**
- **Non-inverting outputs CY7C190**
- **High speed**
  - **—15 ns and 25 ns (commercial)**
  - **—25 ns (military)**
- **Low power**
  - **—303 mW at 25 ns**
  - **—495 mW at 15 ns**
- **Power supply 5V ± 10%**
- **Advanced high-speed CMOS processing for optimum speed/power product**
- **Capable of withstanding greater than 2001V static discharge**
- **Three-state outputs**
- **TTL-compatible interface levels**

Functional Description

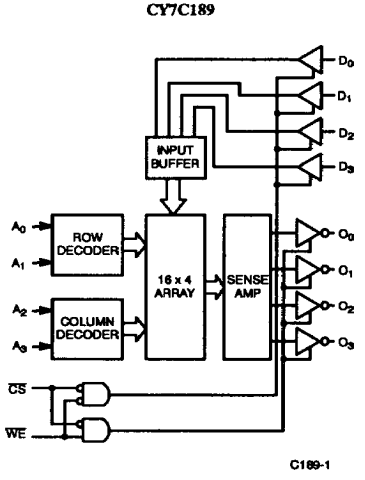
The CY7C189 and CY7C190 are extremely high performance 64-bit static RAMs organized as 16 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting (CY7C189) and non-inverting (CY7C190) outputs.

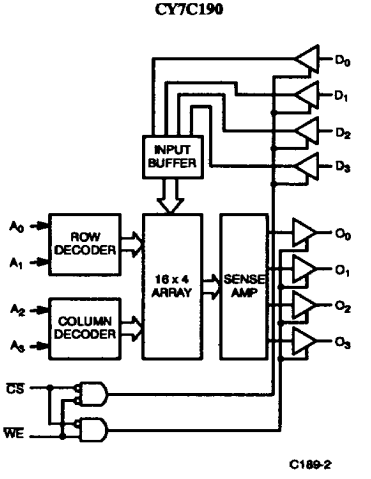
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_3). The outputs are preconditioned such that the correct data is present at the data outputs (O_0 through O_3) when the write cycle is complete. This precondition operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3) in inverted (CY7C189) or non-inverted (CY7C190) format.

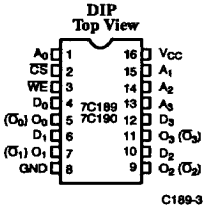
The four output pins remain in high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.

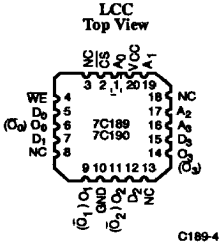
Logic Block Diagram





Pin Configurations





Selection Guide

		7C189–15 7C190–15	7C189–25 7C190–25
Maximum Access Time (ns)	Commercial	15	25
	Military		25
Maximum Operating Current (mA)	Commercial	90	55
	Military		70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 16 to Pin 8) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current, into Outputs (Low) ..... 10 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range [2]

Parameters	Description	Test Conditions		7C189−15 7C190−15 Min.	7C189−15 7C190−15 Max.	7C189−25 7C190−25 Min.	7C189−25 7C190−25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45			V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}		− 40	+40	− 40	+40	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90	mA
I_{OS}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		55	mA
			Mil				70	mA

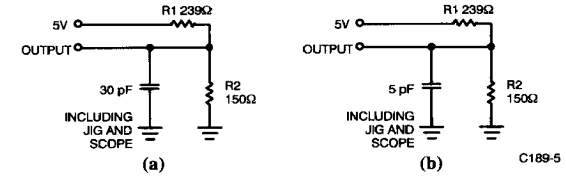
Capacitance [5]

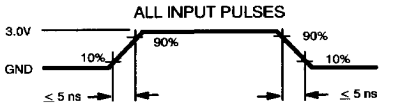
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

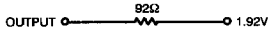
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However these devices are insensitive to − 3V DC input levels and − 5V undershoot pulses of less than 5 ns (measured at 50% points).
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,6]

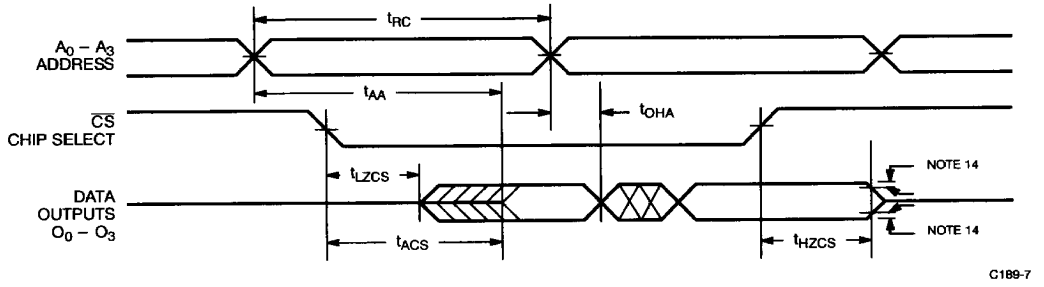
Parameters	Description	7C189–15 7C190–15 Min.	7C189–15 7C190–15 Max.	7C189–25 7C190–25 Min.	7C189–25 7C190–25 Max.	Units
READ CYCLE						
t_{RC}	Read Cycle Time	15		25		ns
t_{AA}	Address to Data Valid[7]		15		25	ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid[7]		12		15	ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[8, 9]		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z		12		15	ns
t_{OHA}	Data Hold from Address Change	5		5		
WRITE CYCLE[10, 11]						
t_{WC}	Write Cycle Time	15		20		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		12		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z		12		20	ns
t_{AWE}	$\overline{WE}$ HIGH to Data Valid[7]		12		20	ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	15		20		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{HA}	Address Hold from Write End	0		0		ns

Notes:

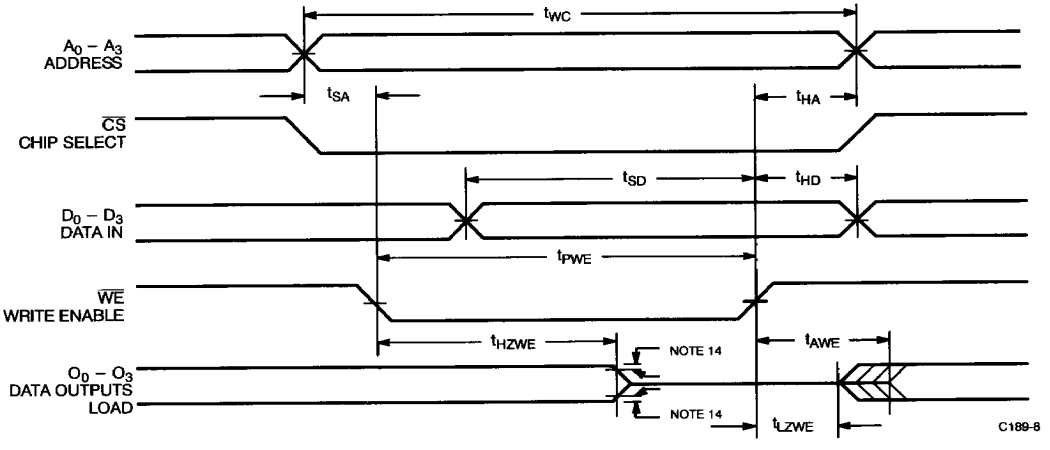
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the spcified I_{OL}/I_{OH}, and 30-pF load capacitance.
7. t_{AA}, t_{ACS}, and t_{AWE} are tested with C_L = 30 pF as in part (a) of AC Test Loads. Timing is referenced to 1.5V on the inputs and outputs.
8. Transition is measured at steady state HIGH level – 500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input.
9. t_{HZCS} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads.
10. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate the write.

Switching Waveforms

Read Cycle



Write Cycle [12, 13]

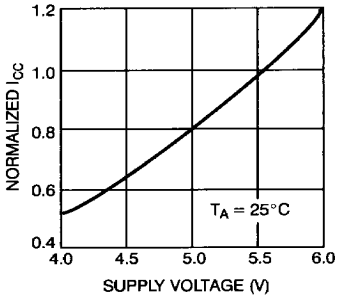


Notes:

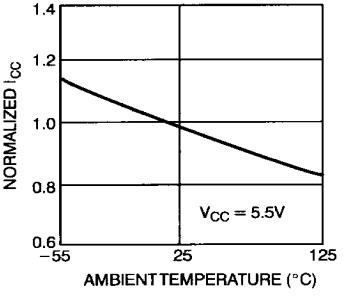
12. All measurements referenced to 1.5V.
13. Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.
14. Transition is measured at steady state HIGH level – 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input.

Typical DC and AC Characteristics

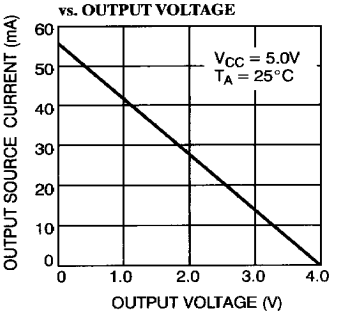
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



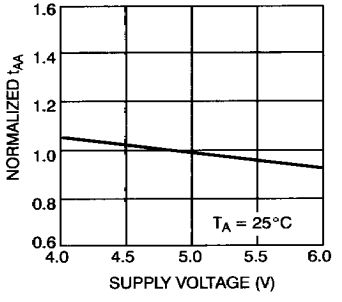
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



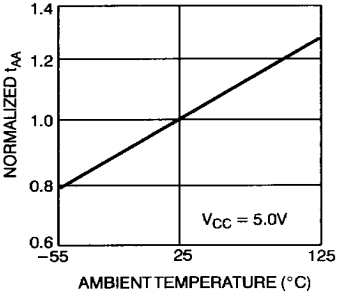
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



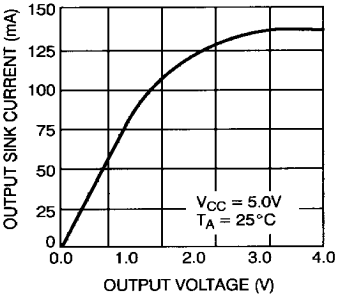
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



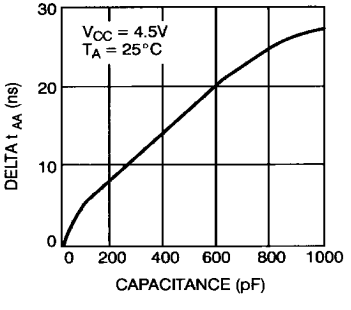
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



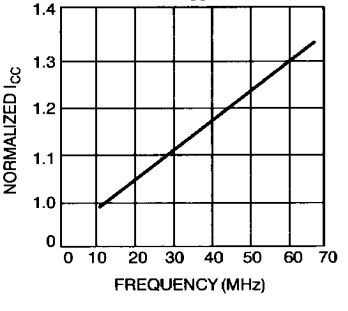
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C189-15PC	P1	Commercial
	CY7C189-15DC	D2	
	CY7C189-15LC	L61	
25	CY7C189-25PC	P1	Commercial
	CY7C189-25DC	D2	
	CY7C189-25LC	L61	
	CY7C189-25DMB	D2	Military
	CY7C189-25LMB	L61	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C190-15PC	P1	Commercial
	CY7C190-15DC	D2	
	CY7C190-15LC	L61	
25	CY7C190-25PC	P1	Commercial
	CY7C190-25DC	D2	
	CY7C190-25LC	L61	
	CY7C190-25DMB	D2	Military
	CY7C190-25LMB	L61	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{AWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11

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