NATIONAL

DM5488/DM7488 256-bit read only memories

general description

These custom-programmed, 256-bit, read only memories are organized as 32 words of 8 bits each. Each monolithic, high-speed, transistor-transistor logic (TTL), 32-word memory array is addressed in straight 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the 32 address gates and cause all 8 outputs to remain high (off). Data, as specified by the customer, are permanently programmed into the monolithic structure for the 256-bit locations. This organization is expandable to n-words to N-bit length.

The address of an 8-bit word is accomplished through the buffered, binary select inputs which are decoded by the 32 five-input address gates. When the memory-enable input is high, all 32 gate outputs are low, turning off the 8 output buffers.

Data are programmed into the memory at the emitters of 32 eight-emitter transistors. The programming process involves connecting or not connecting each of the 256 emitters. If an emitter is connected, a low-level voltage is read out of that bit location when its decoding gate is addressed. If the emitter is not connected, a high-level voltage is read when addressed. Those decoding-gate output emitters which are used are connected to their respective bit lines to drive the 8 output buffers. Since only one decoding gate is addressed at a time, only one of the 32 transistors can supply current to the output buffers at a time.

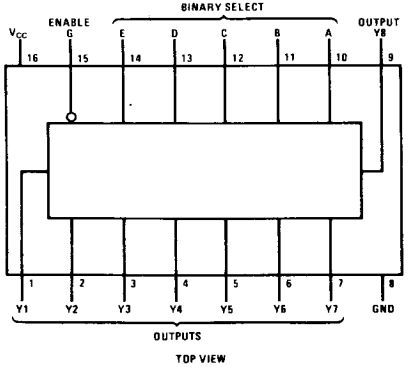
This memory is fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and simplify system design. Input buffers lower the fan-in requirement to only one normalized Series 54/74 load for all inputs including enable (G). The open-collector outputs are capable of sinking 12 mA of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor from each output to the supply line (V_{CC}) is required to define the high-level output voltage. Where multiple DM5488/DM7488 devices are used in a memory system, the enable input allows easy decoding of additional address bits. Access propagation delay time is typically 20 ns and power dissipation is typically 240 mW.

features

- Applications in computer subroutines
- Useful in display systems and readouts
- Memory organized as 32 words of 8-bits each
- Input clamping diodes simplify system design
- Open-collector outputs permit wire-AND capability
- Typical access time: 20 ns
- Typical power dissipation: 240 mW
- Fully compatible with most TTL and DTL circuits

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM5488J or DM7488J
See Package 10
Order Number DM7488N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC} (Note 3)	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5488	4.5	5.5	V
DM7488	4.75	5.25	V
Temperature (T_A)			
DM5488	−55	+125	°C
DM7488	0	+70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})		2			V
Low Level Input Voltage (V_{IL})				0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −12 mA			−1.5	V
High Level Output Current (I_{OH})	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, V_{OH} = 5.5V			40	μA
Low Level Output Current (I_{OL})				12	mA
Low Level Output Voltage (V_{OL}) (Note 2)	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA		0.2	0.4	V
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.4V			25	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.4V			−1	mA
Supply Current, all Outputs High (I_{CCH}) (Note 2)	V_{CC} = Max		37	65	mA
Supply Current, all Outputs Low (I_{CCL}) (Notes 2 and 4)	V_{CC} = Max		48	80	mA

switching characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM INPUT	TO OUTPUT	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	Enable	Any	C_L = 30 pF, R_{L1} = 400Ω, R_{L2} = 600Ω		19	35	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	Enable	Any			18	35	ns
Propagation Delay Time, Low to High Level Output (t_{PLH})	Select	Any			21	35	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	Select	Any			17	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM5488 and across the 0°C to +70°C range for the DM7488. All typicals are given for V_{CC} = 5V and T_A = +25°C.

Note 3: All voltage values are with respect to network ground terminal.

Note 4: All 32 words are addressed separately to ensure that the supply current does not exceed the stated maximum. The typical value shown is for the worst-case condition of all eight outputs driven low at one time.

ordering instructions

Programming instructions for the DM5488 or DM7488 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 32 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the word specified and describes the levels at the eight outputs for that word. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a. Customer's name and address
b. Customer's purchase order number
c. Customer's drawing number

DATA CARD FORMAT

Column

1–2 Punch a right-justified integer representing the positive-logic binary input address (00–31) for the word described on the card.

3–4 Blank

5 Punch "H," "L," or "X" for output Y8. H = high-voltage-level output, L = low-voltage-level output, X = output irrelevant.

6–9 Blank

10 Punch "H," "L," or "X" for output Y7.

11–14 Blank

15 Punch "H," "L," or "X" for output Y6.

16–19 Blank

20 Punch "H," "L," or "X" for output Y5.

21–24 Blank

25 Punch "H," "L," or "X" for output Y4.

26–29 Blank

30 Punch "H," "L," or "X" for ouput Y3.

31–34 Blank

35 Punch "H," "L," or "X" for output Y2.

36–39 Blank

40 Punch "H," "L," or "X" for output Y1.

41–49 Blank

50–51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53–55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57–58 Punch the last two digits of the current year

59 Blank

60–61 Punch "DM"

62–65 Punch the National Semiconductor part number 5488 or 7488.

66–70 Blank

truth table

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

H = High level
L = Low level

functional block diagram