National Semiconductor

DM54ALS1640/DM74ALS1640, DM54ALS1643/DM74ALS1643, DM54ALS1645/DM74ALS1645 Octal TRI-STATE® Bus Transceivers

General Description

This family of advanced low power Schottky devices contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data either transmits from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode, so that the buses are effectively isolated. The TRI-STATE circuitry also contains a protection feature that prevents the buffer from glitching the bus during power-up or power-down.

Features

- Low power versions of ALS640A, ALS643A, ALS645A
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Choice of true or inverting logic
- PNP input design reduces input loading
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

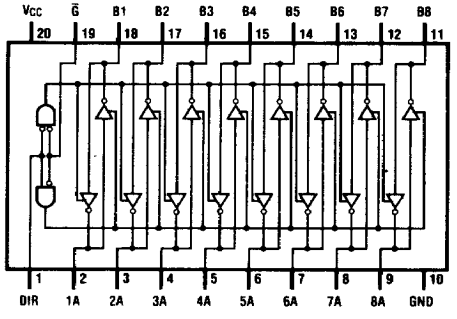
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

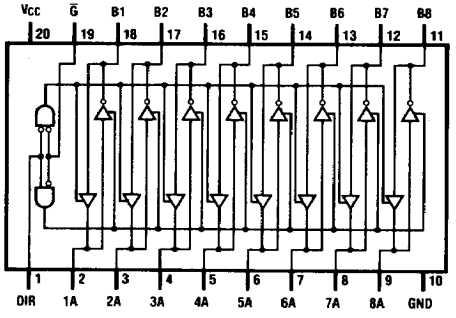
Connection Diagrams

Dual-In-Line Packages



TL/F/6267-1

54ALS1640 (J) 74ALS1640 (J, N)



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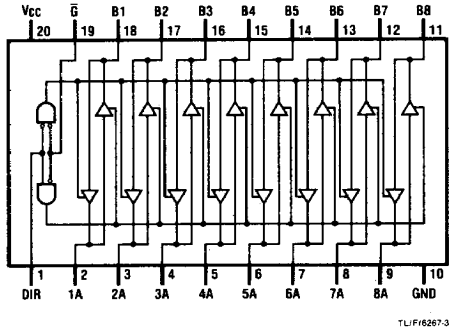
54ALS1643 (J) 74ALS1643 (J, N)

Connection Diagrams (Continued)

Dual-In-Line Package



54ALS1645 (J) **74ALS1645 (J, N)**

Function Table

Control Inputs		Operation		
$\overline{G}$	DIR	ALS1640	ALS1643	ALS1645
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus	B Data to A Bus
L	H	$\overline{A}$ Data to B Bus	$\overline{A}$ Data to B Bus	A Data to B Bus
H	X	Hi-Z	Hi-Z	Hi-Z

Recommended Operating Conditions

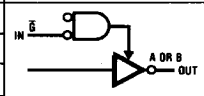
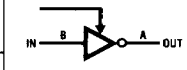
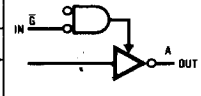
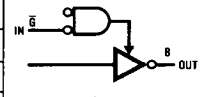
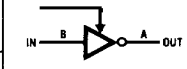
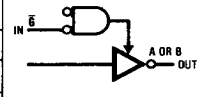
Symbol	Parameter	DM54ALS1640 DM54ALS1643 DM54ALS1645			DM74ALS1640 DM74ALS1643 DM74ALS1645			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	74ALS-1 Option Only						24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions		DM54ALS1640 DM74ALS1640			DM54ALS1643 DM74ALS1643			DM54ALS1645 DM74ALS1645			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5			−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max		2	2.3		2	2.3		2	2.3		V
		I_{OH} = −0.4 mA		V_{CC} − 2			V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 8 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA (74ALS Only) I_{OL} = 24 mA (-1 Options Only)		0.35	0.5		0.35	0.5		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_{IN} = 7V Control Inputs			0.1			0.1			0.1	mA
			V_{IN} = 5.5V A or B Ports										
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1			−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	DM54		18	35		22			25	40	mA
			DM74		18	32		22			25	36	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS			DM74ALS			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1640	5		17	5		15	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		13	2		10	ns
t_{PZL}	Output Enable Time to Low Level	 ALS1640	5		25	5		22	ns
t_{PZH}	Output Enable Time to High Level		5		23	5		20	ns
t_{PLZ}	Output Disable Time from Low Level		5		16	5		13	ns
t_{PHZ}	Output Disable Time from High Level		2		12	2		10	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1643		7			7		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			7			7		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1643		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			8			8		ns
t_{PZL}	Output Enable Time to Low Level	 ALS1643		21			21		ns
t_{PZH}	Output Enable Time to High Level			18			18		ns
t_{PLZ}	Output Disable Time from Low Level			13			13		ns
t_{PHZ}	Output Disable Time from High Level			12			12		ns
t_{PZL}	Output Enable Time to Low Level	 ALS1643		21			21		ns
t_{PZH}	Output Enable Time to High Level			18			18		ns
t_{PLZ}	Output Disable Time from Low Level			13			13		ns
t_{PHZ}	Output Disable Time from High Level			12			12		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1645	2		15	2		13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		15	2		13	ns
t_{PZL}	Output Enable Time to Low Level	 ALS1645	8		28	8		25	ns
t_{PZH}	Output Enable Time to High Level		8		28	8		25	ns
t_{PLZ}	Output Disable Time from Low Level		3		22	3		18	ns
t_{PHZ}	Output Disable Time from High Level		2		14	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.