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Micro MINI E0C6009

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- ● E0C6200B Core CPU
- ● Low Voltage and Low Power
- ● Built-in LCD Driver
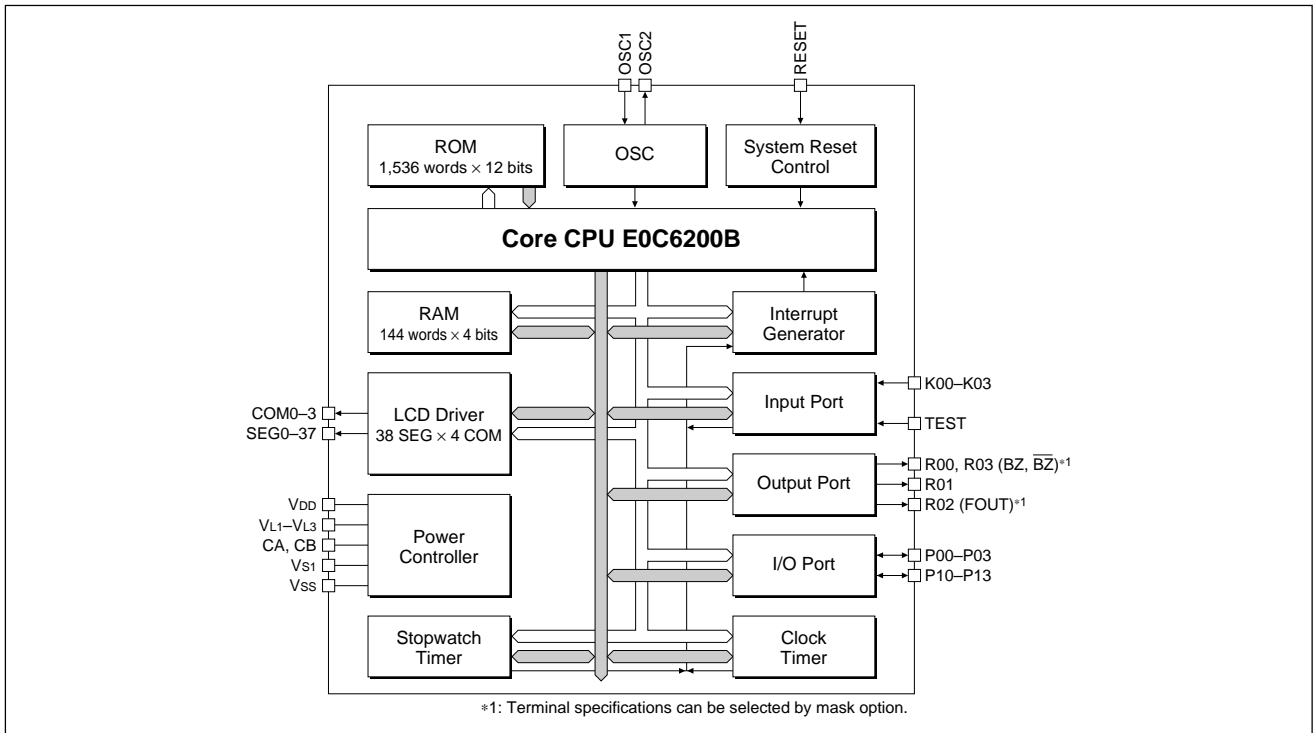- ● Low Cost Performance

■ DESCRIPTION

Micro MINI "E0C6009" is a single chip microcomputer for battery-driven products with 7-segment LCD display. It achieves low cost performance, and is suitable for a product added some feature instead of standard IC. It consists that Seiko Epson's original core CPU E0C6200B, LCD driver (38 segments × 4 commons), 144 words RAM, 1.5K words ROM, clock timer and so on.
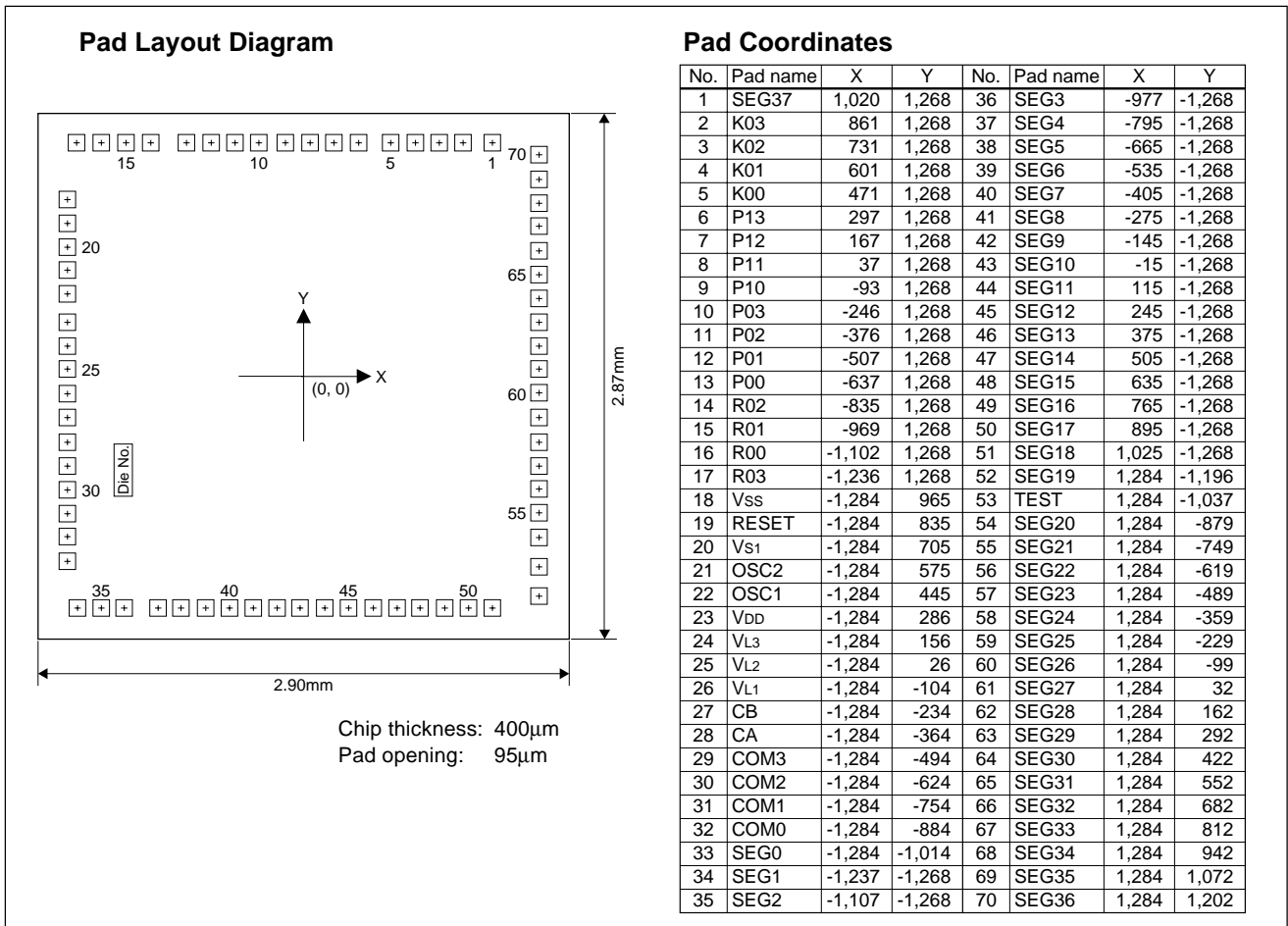
■ FEATURES

- ● CMOS LSI 4-bit parallel processing

- ● Clock .... Crystal 32.768kHz (Typ.) or CR oscillation 65kHz (Typ.)

- ● Instruction set .... 100 instructions

- ● ROM capacity .... 1,536 × 12 bits

- ● RAM capacity .... 144 × 4 bits

- ● I/O port .... I: 4 bits (with pull-down resistor selectable by mask option)
  O: 4 bits (clock and buzzer outputs possible by mask option)
  I/O: 8 bits

- ● Supply voltage detector (SVD) .... No support

- ● Clock timer .... 1ch.

- ● Stopwatch timer .... 1ch.

- ● LCD driver .... 38 segments × 4/3/2 commons

- ● Interrupt .... External : Key interrupt   1 line
  Internal : Timer interrupt   2 lines

- ● Operation voltage .... 1.2 to 1.8V (E0C60L09)
  2.6 to 3.6V (E0C6009)

- ● Power consumption .... 1.0μA (32.768kHz X'tal, 3.0V, HALT)
  2.5μA (32.768kHz X'tal, 3.0V, RUN)

- ● Package .... Die form (pad pitch = 130μm)

E0C6009

■ BLOCK DIAGRAM

*1: Terminal specifications can be selected by mask option.

■ PAD LAYOUT

Pad Layout Diagram

2.87mm

2.90mm

Chip thickness: 400µm
Pad opening: 95µm

Pad Coordinates

No.	Pad name	X	Y	No.	Pad name	X	Y
1	SEG37	1,020	1,268	36	SEG3	-977	-1,268
2	K03	861	1,268	37	SEG4	-795	-1,268
3	K02	731	1,268	38	SEG5	-665	-1,268
4	K01	601	1,268	39	SEG6	-535	-1,268
5	K00	471	1,268	40	SEG7	-405	-1,268
6	P13	297	1,268	41	SEG8	-275	-1,268
7	P12	167	1,268	42	SEG9	-145	-1,268
8	P11	37	1,268	43	SEG10	-15	-1,268
9	P10	-93	1,268	44	SEG11	115	-1,268
10	P03	-246	1,268	45	SEG12	245	-1,268
11	P02	-376	1,268	46	SEG13	375	-1,268
12	P01	-507	1,268	47	SEG14	505	-1,268
13	P00	-637	1,268	48	SEG15	635	-1,268
14	R02	-835	1,268	49	SEG16	765	-1,268
15	R01	-969	1,268	50	SEG17	895	-1,268
16	R00	-1,102	1,268	51	SEG18	1,025	-1,268
17	R03	-1,236	1,268	52	SEG19	1,284	-1,196
18	Vss	-1,284	965	53	TEST	1,284	-1,037
19	RESET	-1,284	835	54	SEG20	1,284	-879
20	Vs1	-1,284	705	55	SEG21	1,284	-749
21	OSC2	-1,284	575	56	SEG22	1,284	-619
22	OSC1	-1,284	445	57	SEG23	1,284	-489
23	VDD	-1,284	286	58	SEG24	1,284	-359
24	VL3	-1,284	156	59	SEG25	1,284	-229
25	VL2	-1,284	26	60	SEG26	1,284	-99
26	VL1	-1,284	-104	61	SEG27	1,284	32
27	CB	-1,284	-234	62	SEG28	1,284	162
28	CA	-1,284	-364	63	SEG29	1,284	292
29	COM3	-1,284	-494	64	SEG30	1,284	422
30	COM2	-1,284	-624	65	SEG31	1,284	552
31	COM1	-1,284	-754	66	SEG32	1,284	682
32	COM0	-1,284	-884	67	SEG33	1,284	812
33	SEG0	-1,284	-1,014	68	SEG34	1,284	942
34	SEG1	-1,237	-1,268	69	SEG35	1,284	1,072
35	SEG2	-1,107	-1,268	70	SEG36	1,284	1,202

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■ PAD DESCRIPTION

Pad name	Pad No.	I/O	Function
VDD	23	(I)	Power supply terminal (+)
VSS	18	(I)	Power supply terminal (-)
VS1	20	–	Constant voltage output terminal
VL1–3	26–24	–	Power source for LCD
CA, CB	28, 27	–	Booster capacitor connecting terminal
OSC1	22	I	Crystal or CR oscillation input terminal *
OSC2	21	O	Crystal or CR oscillation output terminal *
K00–03	5–2	I	Input port terminal
P00–03	13–10	I/O	I/O port terminal
P10–13	9–6	I/O	I/O port terminal
R00	16	O	Output port terminal (BZ output is selectable *)
R03	17	O	Output port terminal ($\overline{BZ}$ output is selectable *)
R01	15	O	Output port terminal
R02	14	O	Output port terminal (FOUT output is selectable *)
SEG0–37	33–52, 54–70, 1	O	LCD segment output (DC output is selectable *)
COM0–3	32–29	O	LCD common output terminal (1/4, 1/3 or 1/2 duty are selectable *)
RESET	19	I	Initial reset input terminal
TEST	53	I	Test input terminal

* Can be selected by mask option

■ BASIC EXTERNAL CONNECTION DIAGRAM

Piezo Buzzer Single Terminal Driving

X'tal	Crystal oscillator	32.768 kHz, C_I = 35 kΩ
CGX	Trimmer capacitor	5–25 pF
C1	Capacitor	0.1 µF
C2	Capacitor	0.1 µF
C3	Capacitor	0.1 µF
C4	Capacitor	0.1 µF
CP	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

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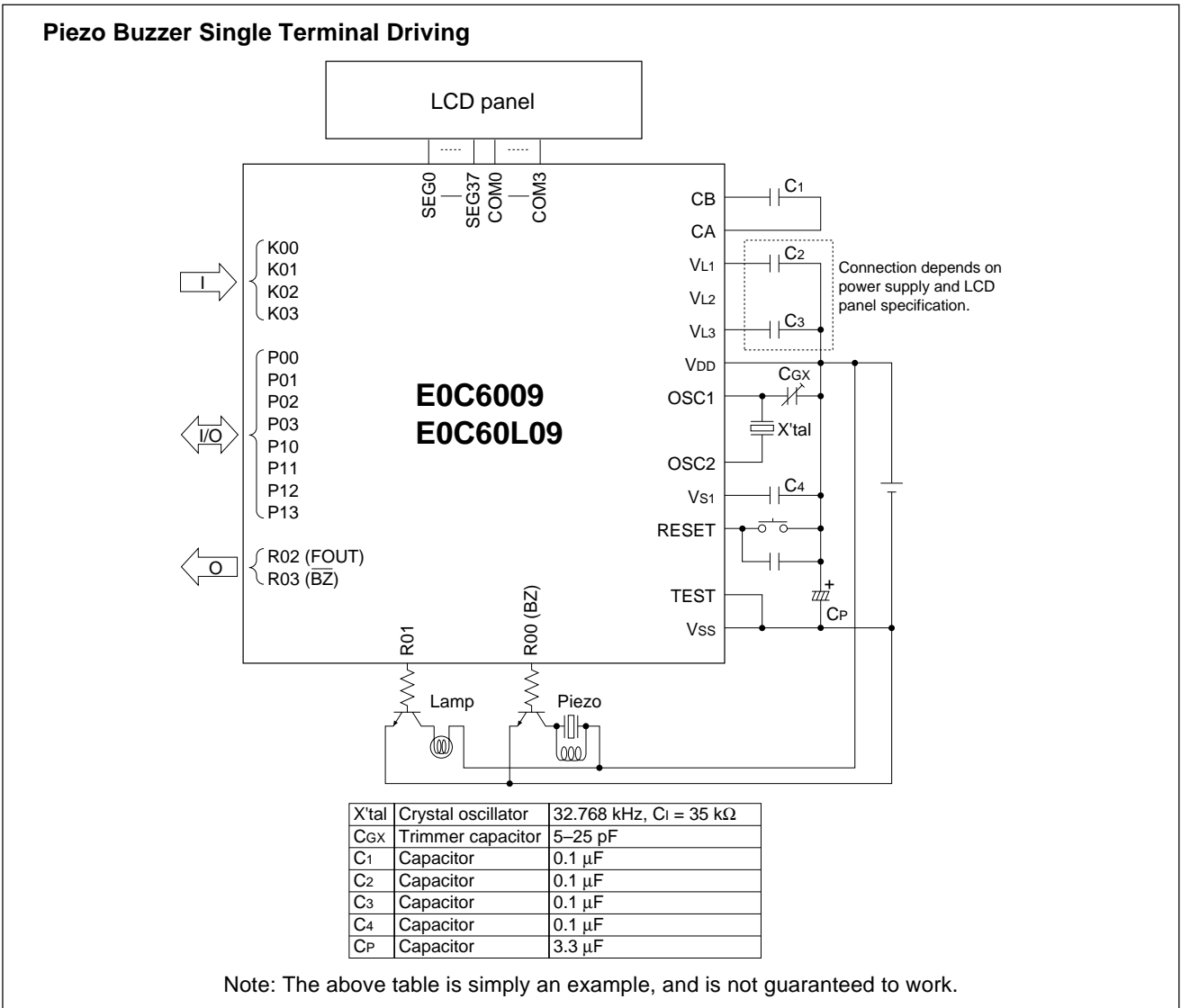
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■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6009

$(V_{DD}=0V)$

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.5 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–

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$(V_{DD}=0V)$

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–

● Recommended Operating Conditions

E0C6009

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	$V_{DD}=0V$	-3.6	-3.0	-2.6	V
Oscillation frequency	f_{OSC}	Crystal oscillation		32.768		kHz
		CR oscillation, $R_{CR}=475k\Omega$		65	80	kHz
Booster capacitor	C_1		0.1			μF
Capacitor between V_{DD} and V_{S1}	C_3 or C_4*1		0.1			μF

*1: Depends on the LCD specification.

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(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	$V_{DD}=0V$	-1.8	-1.5	-1.2	V
Oscillation frequency	f_{OSC}	Crystal oscillation		32.768		kHz
		CR oscillation, $R_{CR}=475k\Omega$		65	80	kHz
Booster capacitor	C_1		0.1			μF
Capacitor between V_{DD} and V_{S1}	C_3 or C_4*1		0.1			μF

*1: Depends on the LCD specification.

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● **DC Characteristics**

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(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $fosc=32.768kHz$, $Ta=25°C$, $V_{S1}/V_{L1}–V_{L3}$ are internal voltage, $C_1–C_4=0.1\mu F$)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	$0.1 \cdot V_{SS}$		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	V_{SS}		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		$0.9 \cdot V_{SS}$	V
High level input current (1)	I_{IH1}	$V_{IH1}=0V$, No pull-down	K00–03, P00–03, P10–13	0		0.5	µA
High level input current (2)	I_{IH2}	$V_{IH2}=0V$, Pull-down	K00–03	4		40	µA
High level input current (3)	I_{IH3}	$V_{IH3}=0V$, Pull-down	P00–03, P10–13 RESET, TEST	50		200	µA
Low level input current	I_{IL}	$V_{IL}=V_{SS}$	K00–03, P00–03, P10–13 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	$V_{OH1}=0.1 \cdot V_{SS}$	R00, R03			-1.8	mA
High level output current (2)	I_{OH2}	$V_{OH2}=0.1 \cdot V_{SS}$	R01, R02, P00–03, P10–13			-0.9	mA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.9 \cdot V_{SS}$	R00, R03	4.0			mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.9 \cdot V_{SS}$	R01, R02, P00–03, P10–13	3.0			mA
Common output current	I_{OH3}	$V_{OH3}=-0.05V$	COM0–3			-3	µA
	I_{OL3}	$V_{OL3}=V_{L3}+0.05V$		3			µA
Segment output current (during LCD output)	I_{OH4}	$V_{OH4}=-0.05V$	SEG0–37			-3	µA
	I_{OL4}	$V_{OL4}=V_{L3}+0.05V$		3			µA
Segment output current (during DC output)	I_{OH5}	$V_{OH5}=0.1 \cdot V_{SS}$	SEG0–37			-200	µA
	I_{OL5}	$V_{OL5}=0.9 \cdot V_{SS}$		200			µA

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(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $fosc=32.768kHz$, $Ta=25°C$, $V_{S1}/V_{L1}–V_{L3}$ are internal voltage, $C_1–C_4=0.1\mu F$)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	$0.1 \cdot V_{SS}$		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	V_{SS}		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		$0.9 \cdot V_{SS}$	V
High level input current (1)	I_{IH1}	$V_{IH1}=0V$, No pull-down	K00–03, P00–03, P10–13	0		0.5	µA
High level input current (2)	I_{IH2}	$V_{IH2}=0V$, Pull-down	K00–03	2		16	µA
High level input current (3)	I_{IH3}	$V_{IH3}=0V$, Pull-down	P00–03, P10–13 RESET, TEST	25		100	µA
Low level input current	I_{IL}	$V_{IL}=V_{SS}$	K00–03, P00–03, P10–13 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	$V_{OH1}=0.1 \cdot V_{SS}$	R00, R03			-300	µA
High level output current (2)	I_{OH2}	$V_{OH2}=0.1 \cdot V_{SS}$	R01, R02, P00–03, P10–13			-150	µA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.9 \cdot V_{SS}$	R00, R03	1400			µA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.9 \cdot V_{SS}$	R01, R02, P00–03, P10–13	700			µA
Common output current	I_{OH3}	$V_{OH3}=-0.05V$	COM0–3			-3	µA
	I_{OL3}	$V_{OL3}=V_{L3}+0.05V$		3			µA
Segment output current (during LCD output)	I_{OH4}	$V_{OH4}=-0.05V$	SEG0–37			-3	µA
	I_{OL4}	$V_{OL4}=V_{L3}+0.05V$		3			µA
Segment output current (during DC output)	I_{OH5}	$V_{OH5}=0.1 \cdot V_{SS}$	SEG0–37			-100	µA
	I_{OL5}	$V_{OL5}=0.9 \cdot V_{SS}$		100			µA

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● **Analog Circuit Characteristics and Current Consumption**

E0C6009 (Crystal Oscillation)

• **4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias** (V_{L2} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L2}$ - 0.1		$1/2 \cdot V_{L2}$ ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3/2 \cdot V_{L2}$ - 0.1		$3/2 \cdot V_{L2}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	μA
		During execution			2.5	5.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L2}$ - 0.1		$1/2 \cdot V_{L2}$ ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3/2 \cdot V_{L2}$ - 0.1		$3/2 \cdot V_{L2}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	μA
		During execution			5.5	10.0	μA

• **3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias** (V_{L3} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	μA
		During execution			2.5	5.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	μA
		During execution			5.5	10.0	μA

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E0C60L09 (Crystal Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L1} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	μA
		During execution			2.5	5.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	μA
		During execution			5.5	10.0	μA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L1} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	μA
		During execution			2.5	5.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	μA
		During execution			5.5	10.0	μA

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E0C6009 (CR Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L2} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L2}$ - 0.1		$1/2 \cdot V_{L2}$ ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3/2 \cdot V_{L2}$ - 0.1		$3/2 \cdot V_{L2}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	μA
		During execution			15.0	20.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L2}$ - 0.1		$1/2 \cdot V_{L2}$ ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3/2 \cdot V_{L2}$ - 0.1		$3/2 \cdot V_{L2}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	μA
		During execution			30.0	40.0	μA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L3} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	μA
		During execution			15.0	20.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$1/2 \cdot V_{L3}$ - 0.1		$1/2 \cdot V_{L3}$ ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	μA
		During execution			30.0	40.0	μA

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E0C60L09 (CR Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L1} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	μA
		During execution			15.0	20.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	μA
		During execution			30.0	40.0	μA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L1} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	μA
		During execution			15.0	20.0	μA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1μF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	μA
		During execution			30.0	40.0	μA

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E0C6009

● Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, boad pattern). Use the following characteristics are as reference values.

E0C6009 Crystal Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-2.6			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-2.6			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	∂f/∂V	Vss=-2.6 to -3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂CG	CG=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-3.6	V
Permitted leak resistance	Rleak	Between OSC1 and VDD, Vss	200			MΩ

E0C60L09 Crystal Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	∂f/∂V	Vss=-1.2 to -1.8V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂CG	CG=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-1.8	V
Permitted leak resistance	Rleak	Between OSC1 and VDD, Vss	200			MΩ

E0C6009 CR Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=475kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC		45.5	65	84.5	kHz
Oscillation start time	tsta	Vss=-2.6 to -3.6V			3	mS

E0C60L09 CR Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, R_{CR}=475kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC		45.5	65	84.5	kHz
Oscillation start time	tsta	Vss=-1.2 to -1.8V			3	mS

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