High Voltage Half Bridge

TARGET DATASHEET

DESCRIPTION

The MED427 offers a high voltage half bridge solution integrated as a module in a ball grid array package. The module is developed specifically for low speed and ultra low power applications where space and quiescent current is of primary concern. The two switches are independently controlled via low voltage compatible inputs controlled by LX1801 (IC1). The lower side IGBT is driven from the LO_EN input via a level shifter. The level shift to the gate drive of the high side IGBT is performed by LX1802 (IC2). When the high side switch is enabled (HI_EN asserted) IC2 is driven from the charged capacitor C2.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

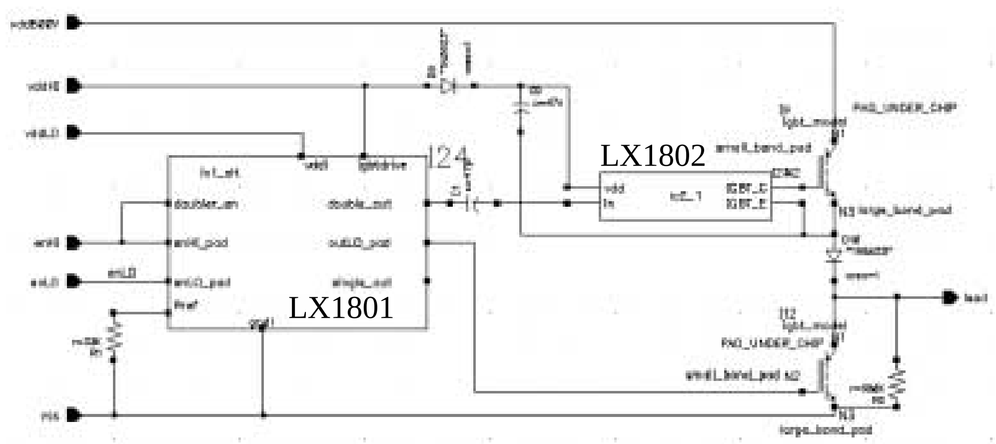
KEY FEATURES

- Miniature size, Multi Chip Module, MCM
- Significant Reduction Component to existing ½ Bridge Design
- Convenient mounting, Ball Grid Array, BGA
- Sn63/Pb37 solder bumps
- 250nA quiescent current
- Maximum switch voltage 1000V
- Maximum switching current 56A

APPLICATIONS

- Implantable Cardioverter Defibrillators
- Low to medium speed applications with low duty cycle requiring small form factor

PRODUCT HIGHLIGHT



MODULE COMPONENT REFERENCE

Component	Manufacturer	Part Number/Value
IC1	Microsemi MP	LX1801
IC2	Microsemi MP	LX1802
R1	State of the Art	0201 33k (5%)
R2	State of the Art	0201 680k (5%)
C1	State of the Art	0805N450J102NT 47pF (1000V)
C2	State of the Art	0603 100nF (50V)
Q1.Q2	Microsemi SA	MSAGA11F120D
D1	Microsemi SA	MD427
D2	Microsemi SA	MD427

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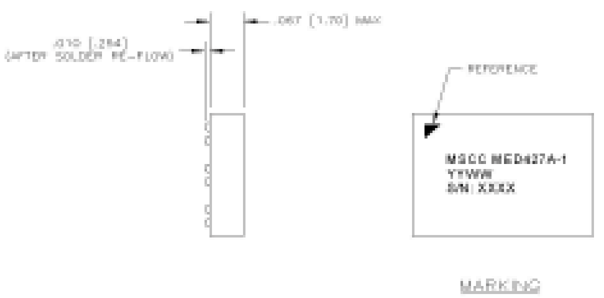
ABSOLUTE MAXIMUM RATINGS

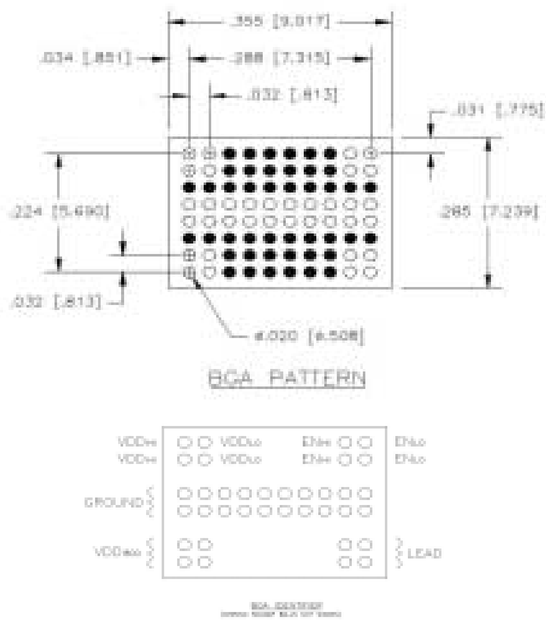
IGBT gate drive voltage, V_{DDHI} 20V
Switch voltage, V_{DD800} 1000V
Positive power supply voltage, V_{DDLO} .... -0.3 to 3.5V

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

MARKING CONFIGURATION



PIN CONFIGURATION



FUNCTIONAL PIN DESCRIPTION

Pin Name	Description
VDDHI	IGBT gate drive supply voltage
VDD800	Switch voltage
VDDLO	Logic Supply voltage
GROUND (VSS)	Negative supply rail, return for Low side switch
ENHI	Enable for high side switch, active high. Note timing requirements
ENLO	Enable for low side switch
LEAD	Switch output, High Z if both LO_EN and HI_EN is low.

OPERATING CONDITIONS

Parameter	MED427-A1 Min	Typ	Max	Units
IGBT gate drive supply voltage V_{DDHI}	15		18	V
Logic level supply, V_{DDLO}	2.6		3.4	V
Ground, V_{SS}		0		V
Operating temperature	31		43	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following test conditions apply: V_{DDHI}=16V,V_{DD800}=V_{SS}=0V,R_{load}=25 Ohm to 0V

Parameter	Symbol	Test Conditions	MED427-A1 Min	Typ	Max	Units
Quiescent current, pin V_{DD}HI Disabled	$I_{DD0(Q)}$	LO_EN=0V,HI_EN=0V		10	100	nA
Quiescent current pin V_{DD800}	$I_{DDH0(Q)}$	VHV=800V,LO_EN,HI_EN=0V				uA
Quiescent current pin V_{DDLO}	$I_{DDLO(Q)}$	HI_EN=0V,LO_EN=0V		10	100	nA
Operating current V_{DD}, HI_EN=1	I_{DDHI_EN}	HI_EN=3.6V,LO_EN=0V		9	12	uA Note 1
Operating current V_{DD}, LO_EN=1	I_{DDL0_EN}	HI_EN=0V,LO_EN=3.6V		10	100	nA
Operating current V_{DDLO}, HI_EN=1	I_{DD1HI_EN}	HI_EN=3.6V,LO_EN=0V				mA
Operating current V_{DDLO} LO_EN=1	I_{DD1L0_EN}	HI_EN=0V,LO_EN=3.6V		10	100	nA
Output voltage rise time	$T_{out(r)}$	VHV=800V 10%-90%, LO_EN=0V,HI_EN=0->3.6V		5		usec
Output fall start	$T_{out(f1)}$	VHV=800V,LO_EN=0V,HI_EN=3.6V->0V		5		Usec
Output fall time	$T_{out(f2)}$	VHV=800V, 90%-10%, LO_EN=0V,HI_EN=3.6V->0V		5		usec
Input low level	Vil	Pins LO_EN, HI_EN			0.3	V
Input high level	Vih	Pins LO_EN, HI_EN	VDDLO-0.3V		VDDLO+0.3 V	V
Quiescent current, pin V_{DD} Disabled	$I_{DD0(Q)}$	LO_EN=0V,HI_EN=0V		10	100	nA

Note 1: Normally the operating current is sourced from the internal bootstrap capacitor. This means that the high side can only be enabled a limited time.

TIMING REQUIREMENTS

Parameter	Symbol	Test Conditions	MED427-A1 Min	Typ	Max	Units
Minimum EN_HI HiToLo to EN_LO LoToHi	T_{d1}		200			usec
Minimum EN_LO HiToLo to EN_HI LoToHi	T_{d2}		10			usec

APPLICATION INFORMATION

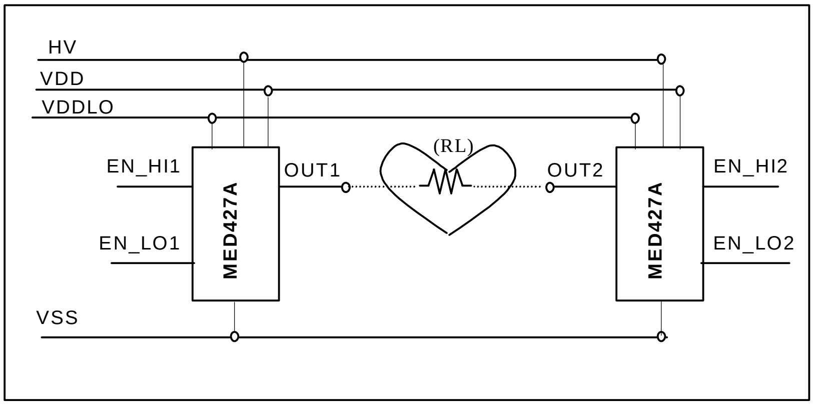


Figure 3

The figures above shows a typical full bridge application that uses two MED427A together with a block diagram for the half bridge. The EN_HI's and EN_LO's are normally controlled from a high voltage controller. A few notes about the operation of this configuration:

1. Before asserting the high side (EN_HI's) any charge on the output of the bridge shall be allowed to "bleed out". In a full bridge application this can also be achieved by discharging through the load and opposite lower side switch.
2. The bootstrap supply relies on that the output is close to VSS before the high side is enabled.
3. The effective high side IGBT gate voltage after EN_HI1 is enabled in half bridge 1 is approximately VGATE0= V(VDD)-V1-V2 where V1 is the voltage at OUT1 when EN_HI1 is enabled and V2 is the voltage drop due charging the gate of Q1.
4. After the high side is enabled IC2 is powered from the energy stored in C2, subsequently there is a limit on how long the high side can be enabled. The high side IGBT gate voltage versus time a can be expressed as VGATE=VGATE0-T*SR.

Where	VGATE0:	Initial gate voltage according to (3) above
	SR:	Typically 0.1V/msec
	T:	Time (in ms) after high side is enabled

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NOTES