DSP56852

Preliminary Product Brief

DSP56852 16-bit Digital Signal Processors

- 120 MIPS at 120MHz
- 6K x 16-bit Program SRAM
- 4K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- 21 External Memory Address lines, 16 data lines and four chip selects
- One (1) Serial Port Interface (SPI) or one (1) Improved Synchronous Serial Interface (ISSI)
- One (1) Serial Communication Interface (SCI)
- Interrupt Controller
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- 81-pin MAPBGA package
- Up to 11 GPIO

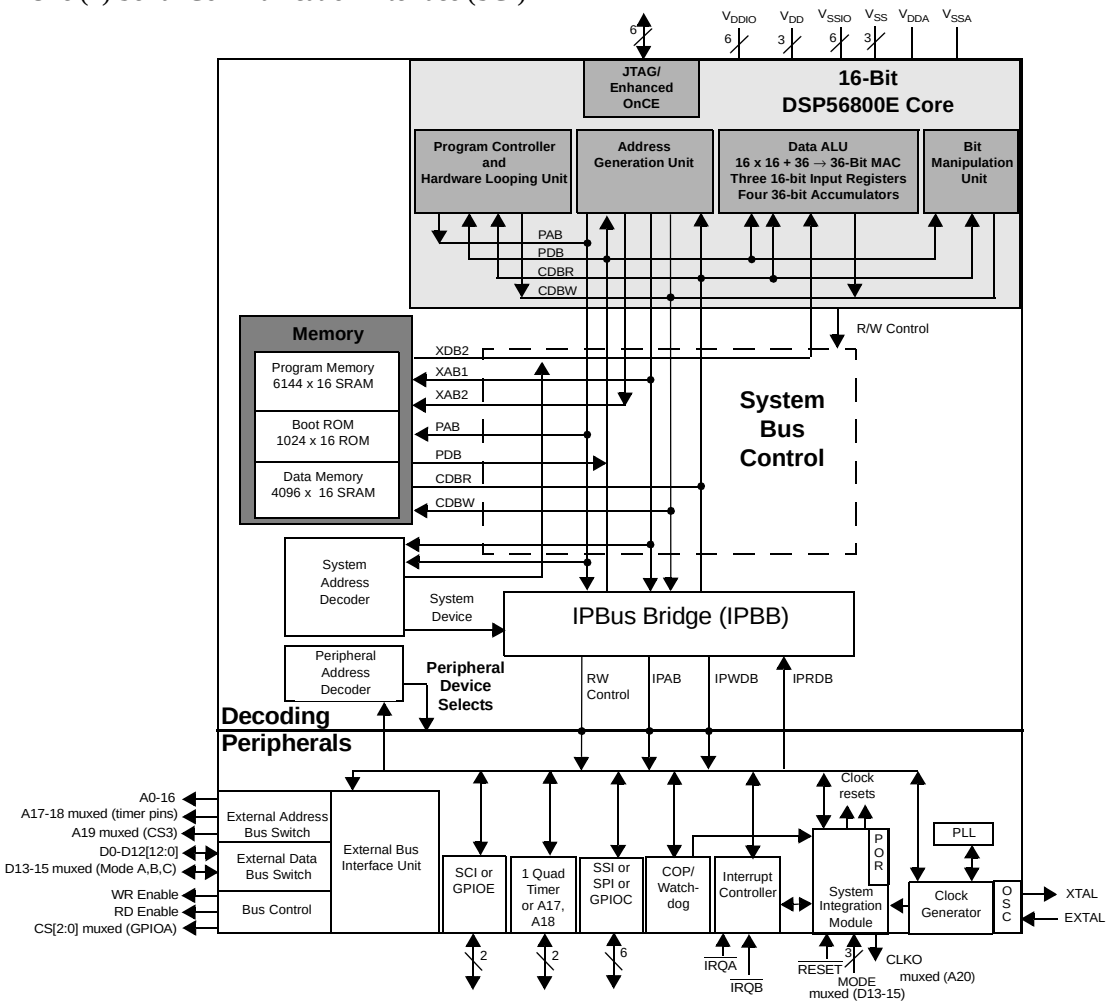

Figure 1. DSP56852 Block Diagram

DSP56800E Core Features

The DSP56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C Compilers to enable rapid development of optimized control applications. Features of the DSP56800E core include:

- Efficient 16-bit DSP engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

DSP56852 Memory Features

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory includes:
  - 6K × 16-bit Program SRAM
  - 4K × 16-bit Data SRAM
  - 1K × 16-bit Boot ROM
- 21 External Memory Address lines, 16 data lines and up to 4 programmable chip select signals

DSP56852 Peripheral Circuit Features

- General Purpose 16-bit Quad Timer with two external pins*
- One (1) Serial Communication Interface (SCI)*
- One (1) Serial Port Interface (SPI) or one (1) Improved Synchronous Serial Interface (ISSI) module*
- Interrupt Controller
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging

- 81 pin MAPBGA package
- Up to 11 GPIO

* Each peripheral I/O can be used alternately as a General Purpose I/O if not needed

Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

DSP56852 Description

The DSP56852 is a member of the DSP56800E core-based family of Digital Signal Processors (DSPs). This device combines the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create an extremely cost-effective solution. The low cost, flexibility, and compact program code make this device well-suited for many applications. The DSP56852 includes peripherals that are especially useful for teledatacom devices, Internet appliances, portable devices, TAD, voice recognition, hands-free devices and general purpose applications.

"Best in Class" Development Environment

The Software Development Kit (SDK) provides fully debugged peripheral drivers, libraries and interfaces that allow a programmer to create his own unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

Product Documentation

The four documents listed below are required for a complete description of and proper design with the DSP56852. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/semiconductors/.

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit DSP core processor and the instruction set	DSP56800ERM/D
DSP56852 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56852	DSP56852UM/D
DSP56852 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56852/D
DSP56852 Product Brief	Summary description and block diagram of the DSP56852 core, memory, peripherals and interfaces (this document)	DSP56852PB/D

Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to order parts.

Table 1. Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56852	1.8V, 3.3V	Map Ball Grid Array (MBGA)	81	120	DSP56852VF120

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