

EPM5128A EPLD

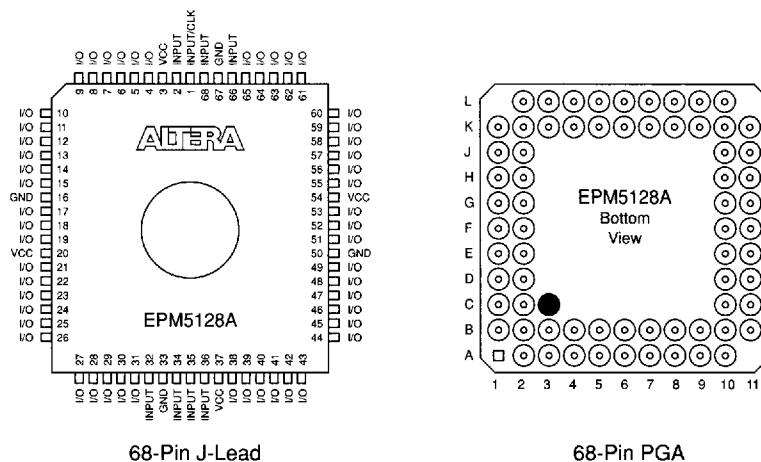
Features

Preliminary Information

- ❑ High-density, second-generation MAX 5000 EPLD developed on an advanced 0.65-micron CMOS EPROM process
- ❑ Higher-speed upgrade for existing EPM5128 designs
- ❑ High-speed multi-LAB architecture
 - t_{PD} as fast as 12 ns
 - Counter frequencies up to 111 MHz
- ❑ 256 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- ❑ Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- ❑ High-density replacement for 74-series SSI and MSI TTL and CMOS logic
- ❑ Available in 68-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 21):
 - J-lead chip carrier (JLCC and PLCC)
 - Pin-grid array (ceramic PGA only)

Figure 21. EPM5128A Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 3 and 4 in this data sheet for package pin-out information. Windows in ceramic packages only.



General Description

The Altera EPM5128A EPLD is a user-configurable, high-performance MAX 5000 EPLD that is pin-, function- and programming-file-compatible with the EPM5128. For a description of the device architecture, see "EPM5128 EPLD" in this data sheet.

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Preliminary Information

Data Sheet

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-2.0	7.0	V
V_I	DC input voltage	Note (1)	-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		-25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	Note (2)	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	-40	85	°C
T_C	Case temperature	For military use	-55	125	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level TTL output voltage	$I_{OH} = -4$ mA DC	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	-10		10	μA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	-40		40	μA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, Notes (2), (5)		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, $f = 1.0$ MHz, Notes (2), (5)		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		20	pF

Data Sheet

Preliminary Information

EPM5128A EPLD

AC Operating Conditions Note (4)

External Timing Parameters			EPM5128A-12		EPM5128A-15		EPM5128A-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			20		25		33	ns
t_{SU}	Global clock setup time		8		10		13		ns
t_H	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		7		8	ns
t_{CH}	Global clock high time		4.5		5		7		ns
t_{CL}	Global clock low time		4.5		5		7		ns
t_{ASU}	Array clock setup time		4		5		6		ns
t_{AH}	Array clock hold time		4		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		11		13		16	ns
t_{ACH}	Array clock high time		4.5		5		7		ns
t_{ACL}	Array clock low time		4.5		5		7		ns
t_{CNT}	Minimum global clock period			9		12		15	ns
f_{CNT}	Max. internal global clock frequency	Note (5)	111.1		83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			9		12		15	ns
f_{ACNT}	Max. internal array clock frequency	Note (5)	111.1		83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	Note (6)	111.1		100.0		71.4		MHz

Internal Timing Parameters Note (7)			EPM5128A-12		EPM5128A-15		EPM5128A-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			2.5		3		4	ns
t_{IO}	I/O input pad and buffer delay			2.5		3		4	ns
t_{EXP}	Expander array delay			6		8		10	ns
t_{LAD}	Logic array delay			6		8		12	ns
t_{LAC}	Logic control array delay			5		5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3		3	ns
t_{ZX}	Output buffer enable delay			5		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5		5	ns
t_{SU}	Register setup time		2		2		1		ns
t_{LATCH}	Flow-through latch delay			0.5		1		1	ns
t_{RD}	Register delay			0.5		1		1	ns
t_{COMB}	Combinatorial delay			0.5		1		1	ns
t_H	Register hold time		5		7		10		ns
t_{IC}	Array clock delay			5		6		8	ns
t_{ICS}	Global clock delay			0		0		0	ns
t_{FD}	Feedback delay			0.5		1		1	ns
t_{PRE}	Register preset time			3		3		3	ns
t_{CLR}	Register clear time			3		3		3	ns
t_{PIA}	Prog. Interconnect Array delay			8		10		13	ns

Notes to tables:

- (1) Minimum DC input is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- (2) Numbers in parentheses are for military- and industrial-temperature-range versions.
- (3) Typical values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V.
- (4) Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C for commercial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C for industrial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_C = -55^\circ\text{C}$ to 125°C for military use.
- (5) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0°C .
- (6) The f_{MAX} values represent the maximum frequency for pipelined data.
- (7) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0°C to 70°C)	Consult factory
Industrial Temp.	(-40°C to 85°C)	Consult factory
Military Temp.	(-55°C to 125°C)	Consult factory
MIL-STD-883-Compliant	Note (1)	See <i>Military Products</i> in this data book.

Note:

- (1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.