PEEL™22V10AZ -15/-25
CMOS Programmable Electrically Erasable Logic Device

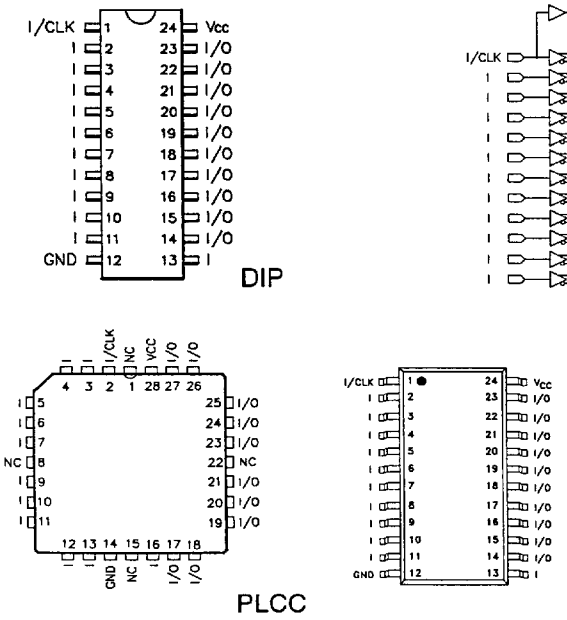
Features

- **Ultra Low Power**
  - — I_{CC} = 25µA (typical) at standby
  - — I_{CC} = 3.5mA (typical) at 1MHz
  - — t_{PD} = 15ns and 25ns versions
- **CMOS Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 133 product term x 44 input AND array
  - — Up to 22 inputs and 10 I/O pins
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Pin and JEDEC compatible with 22V10
  - — Ideal for power-sensitive systems
  - — Enhanced architecture options

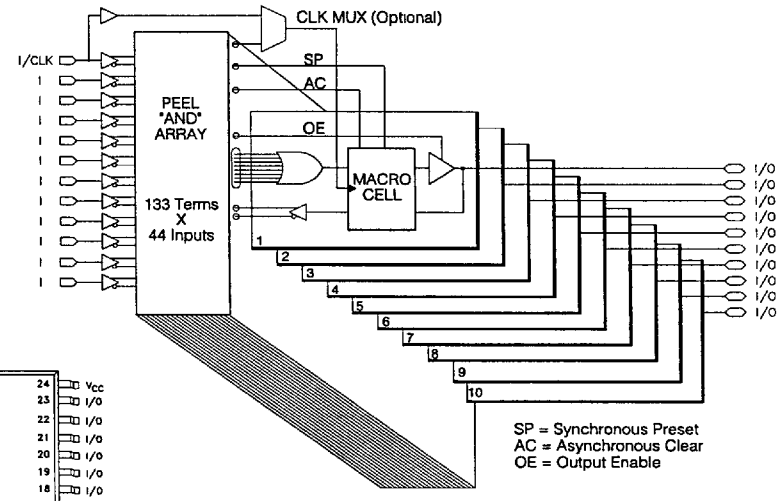
General Description

The PEEL22V10AZ is a Programmable Electrically Erasable Logic (PEEL) device that provides a low power alternative to ordinary PLDs. The PEEL22V10AZ is available in 24-pin DIP and SOIC, and 28-pin PLCC packages. A "zero-power" (100µA I_{CC}) standby mode makes the PEEL22V10AZ ideal for power sensitive applications such as handheld meters, portable communication equipment and laptop computers/peripherals. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability, thus ensuring the highest quality possible. The PEEL22V10AZ is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e. 22V10AZ+). The additional macrocell configurations allow more logic to be put into every device, potentially reducing the design's component count and lowering the power requirements even further. Development and programming support for the PEEL22V10AZ is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



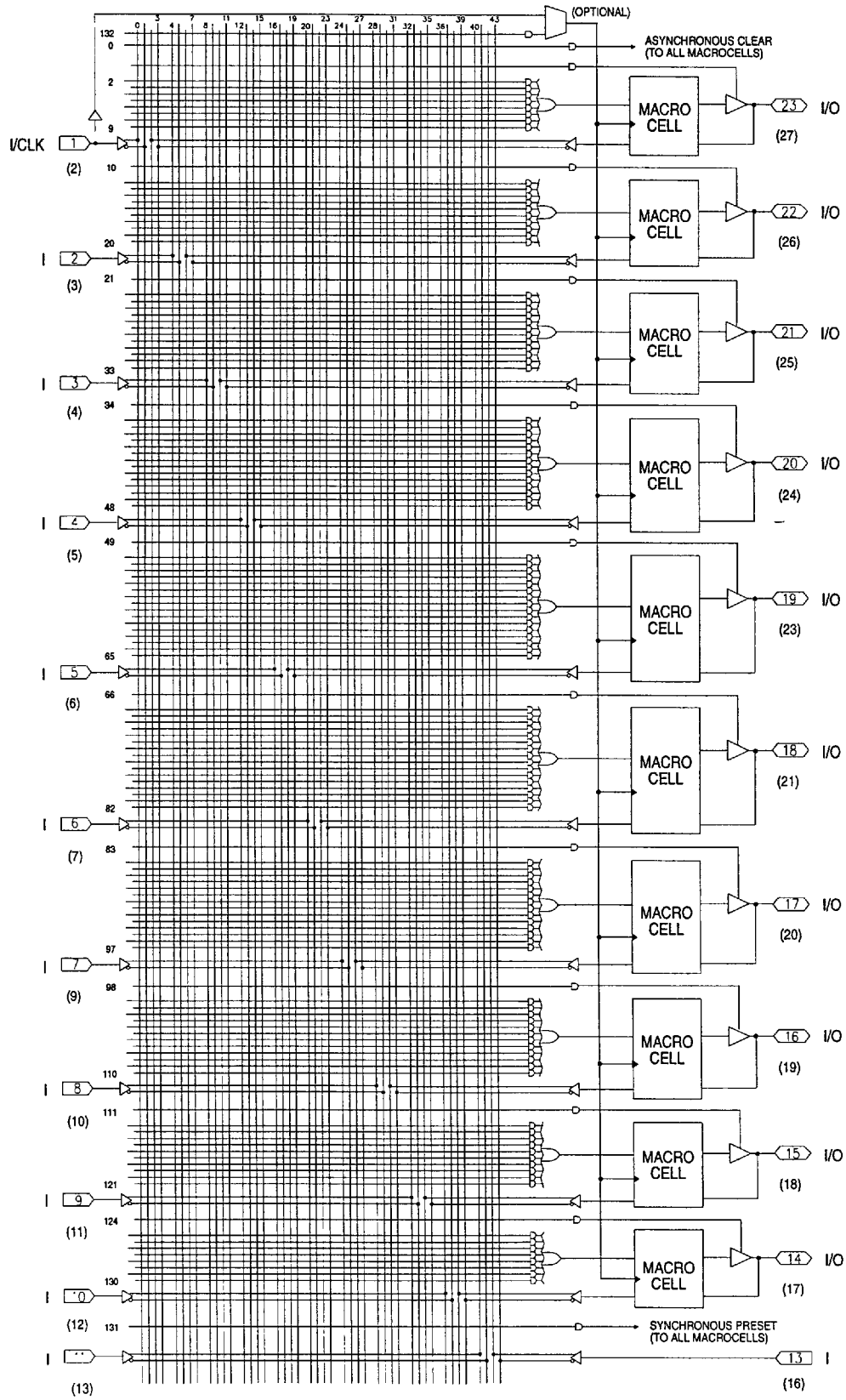


Figure 3. PEEL22V10AZ Logic Array Diagram
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

Function Description

The PEEL22V10AZ implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22V10AZ architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and ten I/Os provide up to 22 inputs and 10 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL22V10AZ can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL22V10AZ (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

133 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form sum of product functions
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term
- 1 global clock term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22V10AZ, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program at least one pair of complementary inputs on unused product terms so that they will have no effect on the output function.)

Variable Product Term Distribution

The PEEL22V10AZ provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22V10AZ to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to Table 1). These bits determine: output polarity and output type (registered or non-registered). Equivalent circuits for the four macrocell configurations are illustrated in Figure 5.

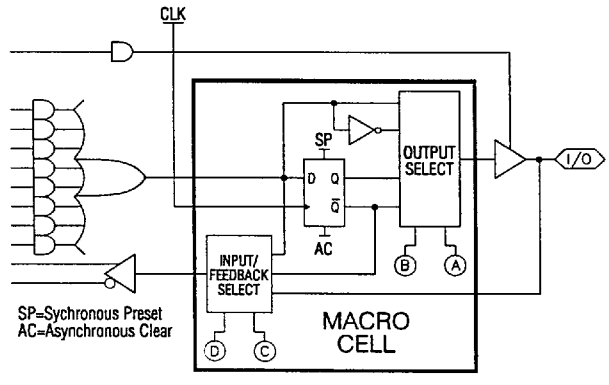


Figure 4. Block Diagram of The PEEL22V10AZ I/O Macrocell

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or clocked into the D-type flip-flop (registered function). The D-type flip-flop loads data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if at least one complementary pair of connections is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5) the Q output of the flip-flop drives the feedback term. When configuring an I/O macrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directional I/O. (Refer also to Table 1.)

Additional Macrocell Configurations

Besides the standard four-configuration macrocell shown in Figure 5, each PEEL22V10AZ provides an additional eight configurations that can be used to increase design flexibility. See Figure 6. The configurations are the same provided by the PEEL 18CV8. However, to maintain JEDEC file compatibility with standard 22V10 PLDs, the additional configurations can only be utilized by specifying the PEEL22V10AZ+ for design entry and device programming. Table 2 shows the macrocell configuration bits for the PEEL22V10AZ+.

Another unique architectural feature of the PEEL22V10AZ+ mode is optional product term macrocell clocking. Using this feature, the macrocell flip flops can be globally clocked from a logic function implemented on a dedicated clock product term.

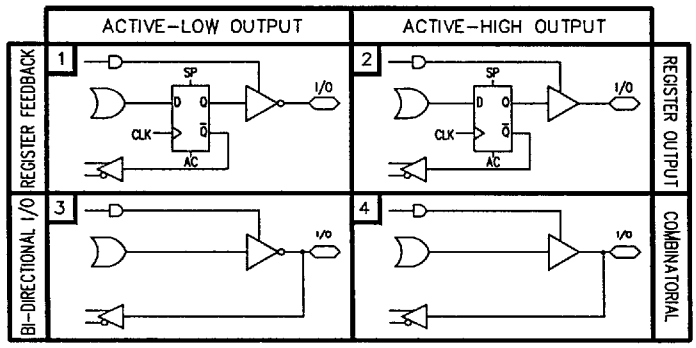


Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22V10AZ I/0 Macrocell

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Table 1. PEEL22V10AZ Macrocell Configuration Bits

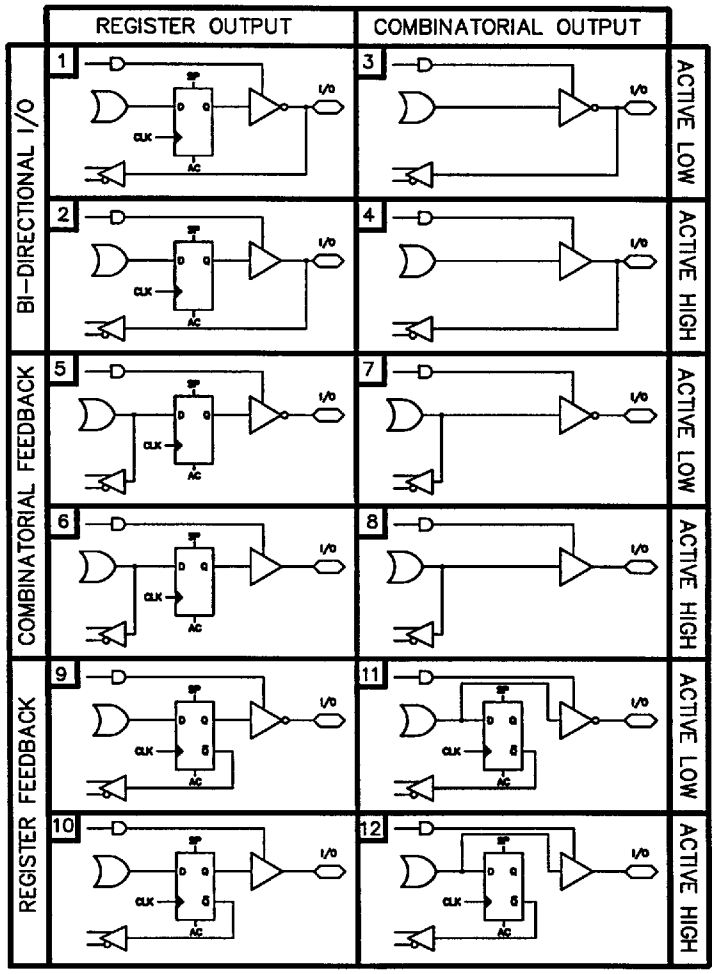


Figure 6. Equivalent Circuits for the Twelve Configurations of the PEEL22V10AZ I/0 Macrocell using the PEEL22V10AZ"+" Design Software and Programming Option

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	"	"	Active High
3	0	1	0	0	"	Combinatorial	Active Low
4	1	1	0	0	"	"	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1	"	"	Active High
7	0	1	1	1	"	Combinatorial	Active Low
8	1	1	1	1	"	"	Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0	"	"	Active High
11	0	1	1	0	"	Combinatorial	Active Low
12	1	1	1	0	"	"	Active High

Table 2. PEEL22V10AZ+ Macrocell Configuration Bits

Zero Power Feature

The CMOS PEEL22V10AZ features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time equal to approximately [t_{PD}], the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will "wake up" for active operation until the signals stop switching long enough to trigger the next power-down.

As a result of the "Zero Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 7.

Design Security

The PEEL22V10AZ provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL22V10AZ if the PEEL22V10AZ+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

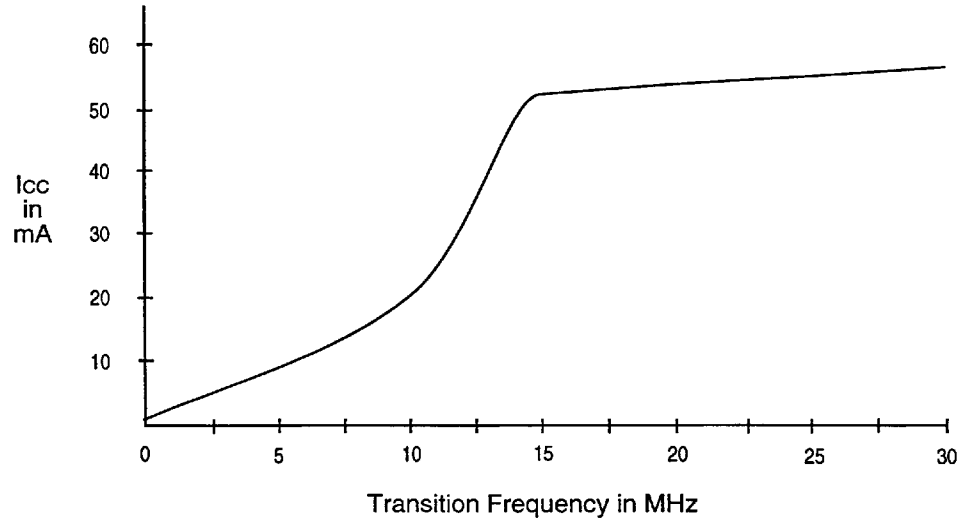


Figure 7. Typical I_{CC} vs Input or Clock transition frequency for 22V10AZ

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin[3]	Relative to Ground[1]	-0.5 to VCC + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+70	°C
T_R	Clock Rise Time	See Note 4		20	ns
T_F	Clock Fall Time	See Note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 4		250	ms

D.C. Electrical Characteristics Over the operating range

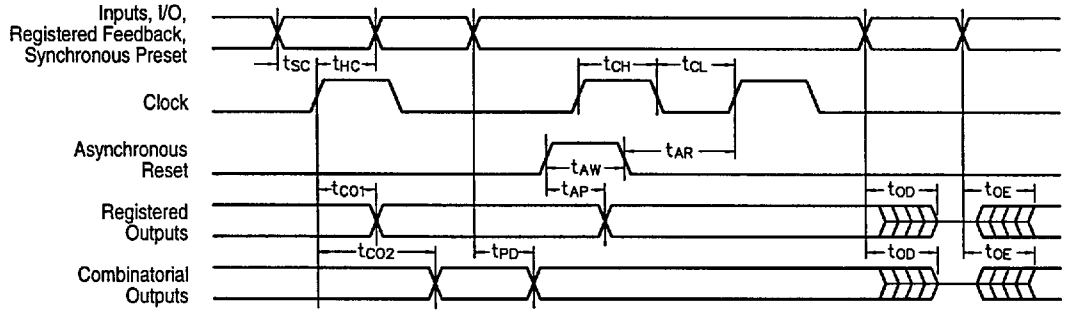
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC}=Min, I_{OH}=-4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage - CMOS	V_{CC}=Min, I_{OH}=-10µA	V_{CC} - 0.1		V
V_{OL}	Output LOW Level - TTL	V_{CC}=Min, I_{OL}=16mA		0.5	V
V_{OLC}	Output LOW Level - CMOS	V_{CC}=Min, I_{OL}=10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		-0.3	0.8	V
I_{IL}	Input and I/O Leakage Current	V_{CC}=Max, GND≤V_{IN}≤V_{CC}, I/O=High Z		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A=25°C	-30	-135	mA
I_{CCS}	V_{CC} Current, Standby	V_{IN} = 0V or V_{CC} All outputs disabled[5]	25 (typ.)	100	µA
I_{CC}[11]	VCC Current, f=1MHz	V_{IN} = 0V or V_{CC} All outputs disabled[5]	3.5 (typ.)	5	mA
C_{IN}[8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}[8]	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range [9, 12]

Symbol	Parameter	-15		-25		Unit
		Min	Max	Min	Max	
t_{PD}	Input[6] to non-registered output		15		25	ns
t_{OE}	Input[6] to output enable[7]		15		25	ns
t_{OD}	Input[6] to output disable[7]		15		25	ns
t_{CO1}	Clock to output		10		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		19		35	ns
t_{CF}	Clock to Feedback		6		9	ns
t_{SC}	Input[6] or feedback setup to clock	10		15		ns
t_{HC}	Input[6] hold after clock	0		0		ns
t_{CL}, t_{CH}	Clock low time, clock high time[9]	7.5		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	20		30		ns
f_{MAX1}	Internal Feedback ($1/t_{SC}+t_{CF}$)[13]	62.5		41.6		MHz
f_{MAX2}	External Feedback ($1/t_{CP}$)[13]	50		33.3		MHz
f_{MAX3}	No Feedback ($1/t_{CL}+t_{CH}$)[13]	66.7		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	15		25		ns
t_{AP}	Input[6] to Asynchronous Reset		18		25	ns
t_{AR}	Asynchronous Reset recovery time		18		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5	µs

Switching Waveforms



Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or Vcc.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; $V_{REF} = V_L$ see test loads in the 1994 ICT Data Book.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as an 10-bit Counter.
12. PEEL Device test loads are specified in the 1994 ICT Data Book.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

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The "Advanced" designation on an ICT data sheet indicates that the product is not yet ready for release. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. ICT or an authorized sales representative should be consulted for current information before using this product.

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