

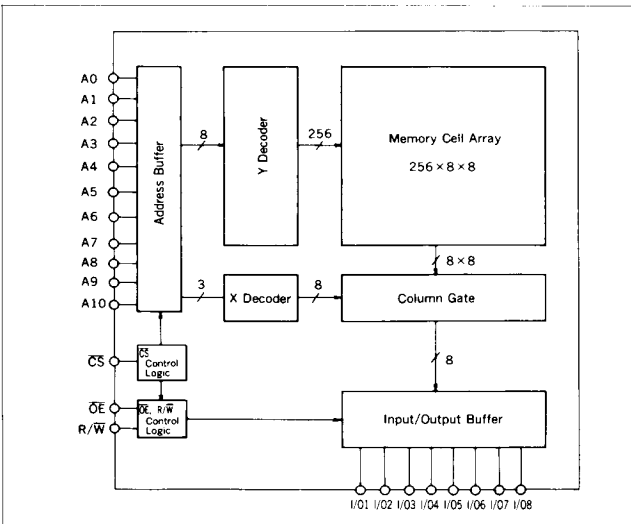
DESCRIPTION

The SRM2016_{10/12} is a 2,048 words x 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

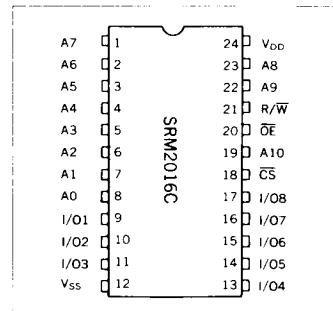
FEATURES

- Access time SRM2016₁₀ 100ns (Max)
SRM2016₁₂ 120ns (Max)
- Low supply current Standby : 1 μ A (Typ)
Operation: SRM2016₁₀ 30mA (Typ)
SRM2016₁₂ 25mA (Typ)
- Completely static operation
- Single power supply .. 5V $\pm$ 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package SRM2016C_{10/12} 24-pin DIP (plastic)
SRM2016M_{10/12} 24-pin SOP (plastic)
SRM2016N_{10/12} 24-pin Skinny DIP (plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A10	Address Input
R/W	Read/Write
OE	Output Enable
CS	Chip Select
I/O1 to 8	Data Input/Output
Vdd	Power Supply (+ 5V)
Vss	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage*	V _I	-0.5 to 7.0	V
Input/output voltage*	V _{I/O}	-0.5 to V _{DD} + 0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temp. & time	T _{sol}	260°C, 10s (at lead)	—

*V_I, V_{I/O} = -1.0V when pulse width is 50 ns

■RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V _{DD}		4.5	5.0	5.5	V
	V _{SS}		0	0	0	V
Input voltage	V _{IH}		2.2	3.5	V _{DD} + 0.3	V
	V _{IL}		-0.3*	—	0.8	V

*V_{IL}(Min) = -1.0V when pulse width is 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM201610			SRM201612			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I _{LI}	V _{DD} = 5.5V, V _I = 0 to V _{DD}	-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CS = V _{IH} , or OE = V _{IH} , V _{I/O} = 0 to V _{DD}	-1	—	1	-1	—	1	μA
Operating supply current	I _{DD0}	CS = V _{IL} , I _{I/O} = 0mA	—	30	60	—	25	50	mA
	I _{DD01}	V _{IH} = 3.5V, V _{IL} = 0.6V, I _{I/O} = 0mA	—	16	—	—	16	—	mA
Average operating current	I _{DDA}	Min. cycle, duty = 100%, I _{I/O} = 0mA	—	30	60	—	25	50	mA
Standby supply current	I _{DDS}	CS = V _{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I _{DDS1}	CS = V _{DD} - 0.2V	—	1	50	—	1	50	μA
Output voltage	V _{OL}	I _{OL} = 4.0mA	—	—	0.4	—	—	0.4	V
	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V

* Typical values are for reference, with V_{DD} = 5V and Ta = 25°C assumed

●Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C _I	V _I = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	6	8	pF

●AC Electrical Characteristics

○Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM201610		SRM201612		Unit
			Min	Max	Min	Max	
Read cycle time	t _{RC}	*1	100	—	120	—	ns
Address access time	t _{ACC}		—	100	—	120	ns
CS access time	t _{ACS}		—	100	—	120	ns
CS output setup time	t _{CLZ}	*2	10	—	10	—	ns
OE access time	t _{OE}	*1	—	55	—	60	ns
OE output setup time	t _{OLZ}	*2	5	—	10	—	ns
CS output floating	t _{CHZ}		0	40	0	40	ns
OE output floating	t _{OHZ}		0	40	0	40	ns
Output hold time	t _{OH}	*1	10	—	10	—	ns

○ Write Cycle

(V_{DD}=5V±10%, V_{SS}=0V, T_a=0 to 70°C)

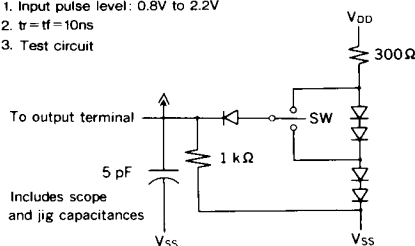
Parameter	Symbol	Conditions	SRM2016 ₁₀		SRM2016 ₁₂		Unit
			Min	Max	Min	Max	
Write cycle time	t _{WC}	*1	100	—	120	—	ns
Chip select time (CS)	t _{CW}		80	—	85	—	ns
Address enable time	t _{AW}		80	—	85	—	ns
Address setup time	t _{AS}		0	—	0	—	ns
Write pulse width	t _{WP}		65	—	70	—	ns
OE output floating	t _{OHZ}	*2	0	40	0	40	ns
R/W output floating	t _{WHZ}	*3	0	45	0	50	ns
Input data setup time	t _{DW}	*1	45	—	50	—	ns
Address hold time	t _{WR}		5	—	5	—	ns
Input data hold time	t _{DH}		0	—	0	—	ns
R/W output setup time	t _{OW}		5	—	10	—	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Input/output timing reference level: 1.5V
4. Output load: I_{ML} + C_L = 100pF

*3 Test conditions.

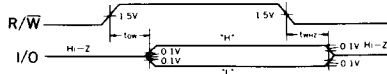
1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit



○ SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of t_{OW} or t_{WHZ}.

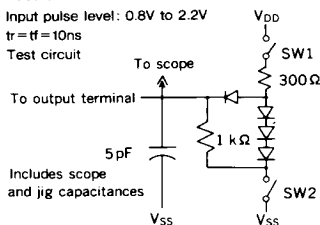
○ SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of t_{OW} or t_{WHZ}.

Output turn-on turn-off times



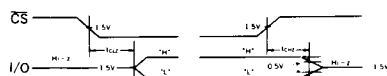
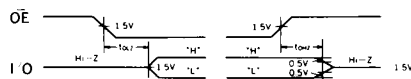
*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit



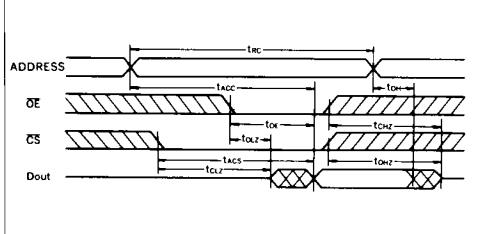
- Both SW1 and SW2 are closed when measuring t_{OHZ} or t_{WHZ}.
- SW1 is open and SW2 is closed when measuring Hi-z-high of t_{OW} or t_{OWH}.
- SW1 is closed and SW2 is open when measuring Hi-z-low of t_{OW} or t_{OWH}.

Output turn-on turn-off times

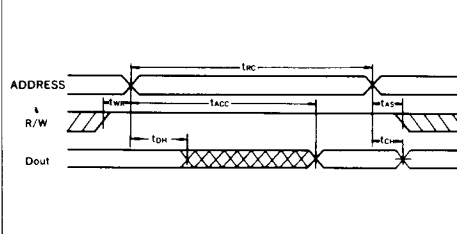


● Timing Chart

○ Read cycle 1 (OE, CS control, R/W=high)



○ Read cycle 2 (R/W control, OE=low, CS=low)



● Writing Data

There are the following three ways of writing data into the memory.

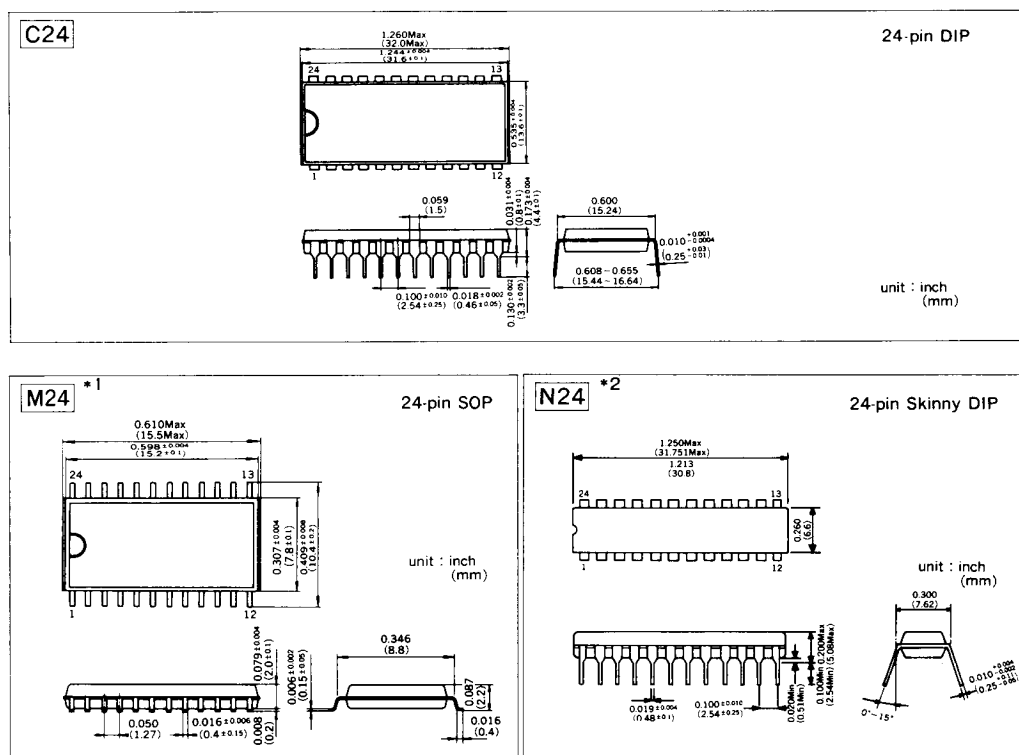
- (1) Hold $\overline{CS}$ low, set the address, and apply a low pulse to $R/\overline{W}$.
- (2) Hold $R/\overline{W}$ low, set the address, and apply a low pulse to $\overline{CS}$.
- (3) Set the address, then apply low pulses to both $\overline{CS}$ and $R/\overline{W}$.

In each case, data from the DATA I/O terminal is fetched into the SRM201610/12 at the last transition of a section in which both $\overline{CS}$ and $R/\overline{W}$ are low. Because the DATA I/O terminal is in high-impedance state when $\overline{CS}$ or $\overline{OE}$ is high, or $R/\overline{W}$ is low, contention of the data driver on the bus and memory output is avoided.

● Standby Mode

When $\overline{CS}$ is high, SRM201610/12 is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state, and input of an address, $R/\overline{W}$ signal, or data is prohibited. When $\overline{CS}$ is above $V_{DD} - 0.2V$, current flowing within the SRM201610/12 chip is only that in the high-resistance portion of the memory cells and leakage current.

■ PACKAGE DIMENSIONS



* 1 Represents model SRM2016M10/12 that has the same electrical characteristics as model SRM2016C10/12.

* 2 Represents model SRM2016N10/12 that has the same electrical characteristics as model SRM2016C10/12.

■ CHARACTERISTICS CURVES

