SUN MICROELECTRONICS

STP1080A

July 1997

UltraSPARC™-I Data Buffer (UDB-I)

DATA SHEET Companion Device for 167/200 MHz UltraSPARC-I Systems

DESCRIPTION

The UDB-I is a data buffer device used in UltraSPARC-I systems to connect the CPU and its external SRAM cache bus to the system bus:

- On the CPU/SRAM side, the E-Cache Bus consists of 128 data bits and 16 parity bits
- On the system side, the UPA Bus consists of 128 data bits and 16 ECC bits

The UDB-I is clocked by the UPA clock; its interfaces are fully synchronous.

The UDB-I is a 256 pin, 3.3 volt CMOS device. It is an integral part of an UltraSPARC-I CPU system. In CPU module based systems, the UDB-I is part of the module design.

The UDB-I device was originally called the "UDB". The UDB-I device's original part number was STP1080BGA or simply STP1080. The "-I" suffix was added to the UDB reference to differentiate it from the UDB-II, used in UltraSPARC-II designs.

The UDB-I part number was revised to STP1080A to reflect a package change. The package thickness was reduced from 2.4 mm to 2.19 mm. No other changes were made to its form, fit, or function. The STP1080A is designed to be a drop-in replacement for the STP1080.

Features	*Benefits*
• Isolates the processor from the system bus	• High performance: ease of design
• Interface to the UPA	• Fully synchronous design
• Operates at system frequency	
• Provides data buffering	
• Supports parity on the CPU side and ECC on the system side	
• Stores interrupt vectors. Interrupt registers visible to software	• Enables secondary cache transfers and system memory transfers by isolation
• IEEE1149.1 (JTAG) boundary scan test	• Ease of manufacturing test
• 256 PBGA package	• Small footprint and cost effective packaging

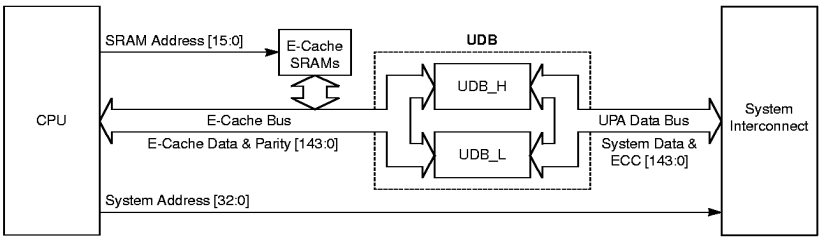


Figure 1. UDB Module Block Diagram

UDB has intelligent storage for 1 64-byte cache line, and 8 16-byte stores.It allows delivery of desired 16-byte chunk first, and compensates for the discrepancy in the delivery rates of the E-Cache and Interconnect.

UltraSPARC-I has a second-level cache of at least 512KB. The second-level cache is physically indexed, physically tagged. The system address goes to the system controller and does not pass through UDB.

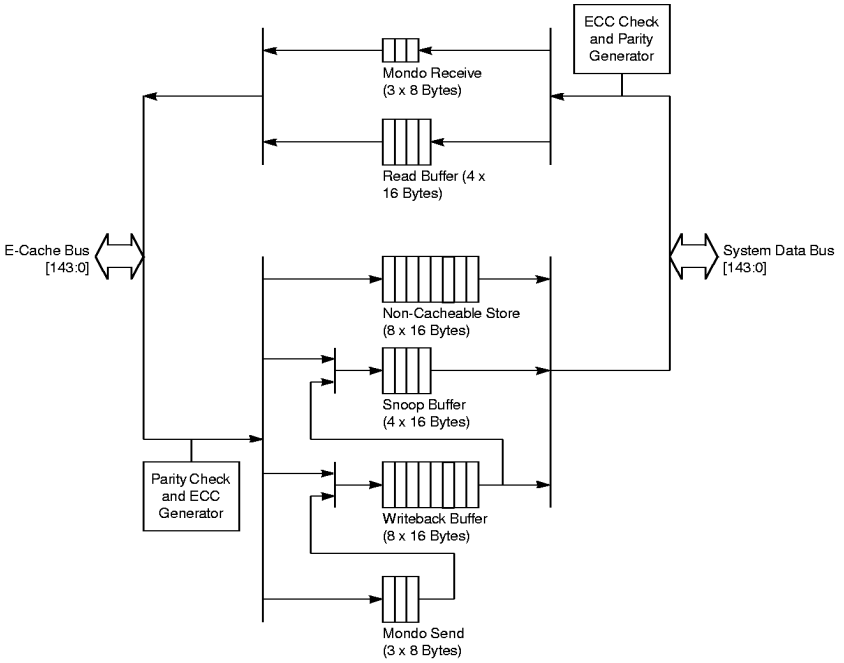


Figure 2. UDB Datapath Logical Block Diagram

TECHNICAL OVERVIEW

Data Buffering

UltraSPARC-I can have multiple outstanding request types, and be responding to multiple request types from the Interconnect (receiving interrupts, delivering snoop data). However, except for noncacheable stores, UltraSPARC-I can have only one outstanding request of each type. 'Outstanding" implies that the address is driven to the interconnect, but not the data.

There is storage for 1 64-byte external cache line. Eight outstanding noncacheable stores are allowed (16-bytes of data due to compression) using the full interconnect bandwidth of 1 per interconnect cycle).

64-byte Buffers

64-byte buffers are provided for READs from the DataBus, and for SNOOPs and Writebacks from the EcacheBus.

16-byte Buffers

The UDB can hold data for 8 noncacheable stores in progress.This store data comes from UltraSPARC-I's store buffer.

8-byte Buffers

Two interrupts, each consisting of three 64-bit packets, are also buffered in UDB. One buffer holds data going from the cpu to the UPA, while the other holds data going from the UPA to the cpu.

TABLE 1: Mondo Vector Format

Component	Interrupt _0 (Cycle 1)	Interrupt_1 (Cycle 2)	Interrupt_2 (Cycle 3)	Interrupt_3 (Cycle 4)
UDB_h	Data0	Data1	Data2	xxxxxx
UDB_l	xxxxxx	xxxxxx	xxxxxx	xxxxxx

Sub-Block Ordering

The UDB delivers and receives 16-byte subblocks in desired-word-first order. Subsequent blocks are delivered in order, wrapping to the beginning of the block, if necessary. UDB does no data re-ordering.

All 64-byte write-backs from UltraSPARC-I are delivered starting with subblock 0.Data returned for snoops is desired subblock first also. The UDB chips supply pending CopyBack data in the correct order for a snoop.

ECC/Parity

ECC is 8 bits per 64 data bits. It is one of the single-error correcting, double error (and nibble-error) detecting codes. The implementation has separate trees for ECC checking and correcting. Correctable errors are fixed in the same cycle as they are detected. The UDB will log the syndrome for the error (to help in diagnosing multi-bit errors). There are some CSR read/write registers for enabling/disabling ECC. (accessible through special ASI load/stores). There are two trap modes:

1. Trap on any ECC error
2. Trap on non-correctable ECC error

There is no automatic updating of memory when a single-bit ECC error is corrected. Software may update memory with corrected data, maintaining MP cache coherency, by using cache flushes and Compare-And-Swap.

Data is protected on the CPU side using parity (odd parity), and on the system side using ECC. Parity is generated for data going from the UDB to the CPU, while ECC bits are generated for data going from the UDB to the UPA. Data coming to the UDB from the CPU is checked for parity errors, while data coming from the UPA to the UDB is checked for ECC.

ECC Code Used

ECC is performed on a 64-bit boundary, using Kaneda SEC/DED/S4ED codes. There are eight check bits per 64-bit boundary. The code provides detection of single and double bit errors, as well as three and four bit errors within a nibble. In addition, the code provides correction of any single bit error on 64-bit data.

ECC Control and Status Registers

Memory is not updated after correcting an error. Parity error is detected by the XOR of the eight P_syndrome bits. During ECC checking, the syndrome for the first correctable error is logged, and is only overwritten by the syndrome for an uncorrectable error. When there is an uncorrectable error, bad parity is forced onto data going out to the CPU. In diagnostic mode, a check bit vector of ECC bits is forced for data going from UDB to UPA.

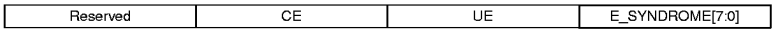


Figure 3. ECC and Parity Fault Status Register (Duplicated in UDB_H and UDB_L)

TABLE 2: ECC Status Definition [1]

Field	Description	Type
CE	Correctable Error	W1C
UE	Uncorrectable Error	W1C
E_Syndrome	ECC syndrome bits, 64 bits -> 8 bits	R

1. This register is cleared to 0 at power-on reset; W1C implies write-1-to-clear.

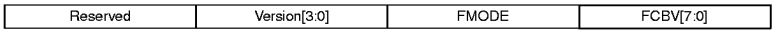


Figure 4. ECC Control and Diagnostic Register (Duplicated in UDB_H and UDB_L)

TABLE 3: ECC Control and Diagnostic Register Definition

Field	Description	Type
Version	Software-accessible Version Number ==TAP_IDreg[31:28]	R
FMODE	Force Check Bit Vector for data to UPA	RW
FCBV	Forced Check Bit Vector	RW

Bad Parity errors need not be forced by the UDB; UltraSPARC-I could write the SRAMs with bad parity and have the UDB detect it. Bad ECC errors can be forced by using the check bit vector FCBV[7:0] in each UDB.

Error Detection and Correction

Parity Errors

If an E-Cache parity error occurs while snooping, a known bad ECC data/checkbit pattern will be forced. This will cause an UncorrectableError (UE) trap at the master that requested the data. The slave processor will log error information, (physical address etc). This error log can be read by the master after he traps.The slave is not interrupted.

If parity error occurs while the E-Cache was being read for a WriteBack (victimized line), bad ECC is also generated, before the data goes to memory. The error info is logged in the same register, and the processor traps.

The bad ECC guarantees no one else will use the bad data. Software can clean up the bad ECC in memory in the trap handler.

ECC Errors

The UDB will not stall the data delivery to UltraSPARC-I on a Correctable or Uncorrectable Error.

Uncorrectable errors will have bad parity forced, before installing in the E-Cache. This prevents using the bad data, or having the bad data written to memory with correct check bits later on.

In either case, the error log will save appropriate state. Separate CE and UE enables will control whether the processor is trapped.

If the error occurs in a sub-block after the sub-block referenced by the processor, the trap will still happen.

If an ECC error is detected, bad parity is generated for outgoing data to UltraSPARC-I and/or the SRAMs.

When an ECC error occurs at the same time as the UDB status register is being written by software, the syndrome will be updated according to the UE and CE bits with the software clearing factored in. This is consistent with the conceptual model of software update being performed before the error is logged.

Assertion of ecc_valid indicates whether the ecc bits with the data being driven is valid. Error detection and correction are disabled for incoming data when ecc_valid is dis-asserted.

Interrupts

The DataPath has storage for receiving interrupts.They reside in the UDB only until UltraSPARC-I pulls them out. UDB has the “real” interrupt registers that are visible to software.

Interrupt Data Buffers

Interrupts are delivered as write transactions from the System Controller to UltraSPARC-I.

I/O devices will interrupt by sending interrupt data packets to a selected processor. The packet will typically consist of a 64-bit PC, a 64-bit data structure pointer, and one 64-bit datum.

UltraSPARC-I is an interrupt data receiver. The processor will be able to post interrupts to itself at any level by writing to the SOFTINT register.

Parity and ECC errors on reads are reported back to the LSU, which logs the error status and traps the processor. Errors on writes are reported asynchronously by slaves, using interrupts.

Interrupt-Send Unit

UltraSPARC-I will be able to send interrupts. ASI stores will load data into a special UDB buffer. A final ASI store will initiate the interrupt. A status register in UltraSPARC-I can be read with an ASI load to interrogate the completion status of the interrupt.

Control and Data Transfers

For UltraSPARC-I, the queue depth is generally one. UltraSPARC-I DataBuffer chips (UDB) have 64-byte buffers reserved for each request class. Master Writes are the exception. To handle multiple noncacheable stores to the frame buffer, this queue has eight entries. The UDB knows that only noncacheable stores use queue entries besides the first, and doesn't require a full cache line of data buffering. Only 16 data bytes are used for those queue entries.

Data transfers occur some arbitrary time after address requests. Masters are responsible for buffering all data associated with queued requests.

Interrupt data delivery is handled as a normal System Controller (SC) write. (It is the only allowed SC write. All other SC to UltraSPARC-I (SP) transactions must be SC reads).

The EcacheBus is controlled by the UltraSPARC-I ECU. Besides E-Cache reads and writes, there are transfers to and from the UDB. UDBCntl[4:0] tells the UDB what's happening on EcacheBus.

TABLE 4: CNTL[4:0] Encodings

CNTL	Mnemonic	Action
00000	Noop	
00001	rd_nodeid	Read nodeid (during reset)
00010	rd_ctrl	Read UDB control register (UDB_h and UDB_l)
00011	rd_stat	Read UDB status register (UDB_h and UDB_l)
00100	rd_mondor0	Read interrupt vector[0] (PC)
00101	rd_mondor1	Read interrupt vector[1] (Pointer)
00110	rd_mondor2	Read interrupt vector[2] (Data)
00111	rd_readbuf	Read buffer
01000	mv_wrback0	Move writeback buffer[0] to snoop buffer
01001	mv_wrback1	Move writeback buffer[1] to snoop buffer
01010	mv_wrback2	Move writeback buffer[2] to snoop buffer
01011	mv_wrback3	Move writeback buffer[3 to snoop buffer
10000	wr_ctrl_l	Write UDB_l control register (LS)
10001	wr_ctrl_h	Write UDB_h control register (MS)
10010	wr_stat_l	Write UDB_l status register (LS)
10011	wr_stat_h	Write UDB_h status register (MS)
10100	wr_mondos0	Write mondo vector [0] (by CPU)
10101	wr_mondos1	Write mondo vector [1] (by CPU)
10110	wr_mondos2	Write mondo vector [2] (by CPU)
11000	wr_snoop	Write snoop buffer
11001	wr_ncst	Write noncacheable store buffer
11010	wr_wrback	Write writeback buffer
11100	mv_mondos0	Move interrupt vector[0] to writeback buffer
11101	mv_mondos1	Move interrupt vector[1] to writeback buffer
11110	mv_mondos2	Move interrupt vector[2] to writeback buffer
11111	mv_mondos3	Move interrupt vector[3](fake) to wrback buffer

There is a pin (UDB_CE) from the UDB for indicating when a single bit ECC error is detected and corrected. There is a pin (UDB_UE) from the UDB for identifying uncorrectable ECC errors. If asserted during a E-Cache miss, the new line must not be marked valid in the E-Cache or D-Cache. ECC on the full DataBus is checked/generated for all system transactions.

Transactions on the DataBus are controlled by the System Controller (SC) to UltraSPARC-I ReplyBus.

TABLE 5: S_REPLY[3:0] Encodings [1]

S_REPLY	Mnemonic	Action
0000	s_idle	Default
0001*	s_err	Bus error
0010	s_sack	Coherence read block: UDB => snoop buffer (64B)
0011	s_wbcan	Writeback cancel: incr. wrback buffer readctr by 4
0100	s_was	Write ack single: UDB => non-cacheable store
0101	s_wab	Write ack block: UDB => wrback/block_store/interrupt send
0110*	s_oak	Ownership ack block
0111*	s_inak	Interrupt nack
1000	s_rbu	Read block unshared: UDB <= read fill (64B)
1001	s_rbs	Read block shared: UDB <= read fill (64B)
1010	s_ras	Read ack single: read fill (16B)
1011*	s_rto	Read time-out
1101	s_swib	Slave write interrupt block: UDB <= interrupt receive
1110	s_srs	Slave read single: UDB => read_portid
1111*	s_srb	Slave read block

1. Opcodes with * imply the UDB-I takes no action.

The data_stall signal from the UPA allows the system controller to control the flow of data to or from that UPA port. It is typically used to allow memory several cycles of setup on the UPA bus, or to ask the UPA port to hold data longer, so that it can be held at memory longer.

Clocking

Processor/Interconnect Clock Relationship

The ratio of the processor to interconnect clock can be either 2:1 or 3:1. UDB operates at interconnect frequency.

Testability

The UDB implements the IEEE 1149.1 standard, to aid in board level testing. Boundary Scan Description Language (BSDL) is available for the device.

External Power Down

The power down mode is intended to support Energy Star compliance. The EPD pin initiates an internal reset, stops the clock and PLL, and UDB enters power-down mode. Exiting power down mode is similar to normal power-up sequence.

SIGNAL DESCRIPTIONS

Symbol	Type	Name and Function
EDATA[63:0]	I/O	The UDB chip does data transfers over this bus with both the E-Cache RAMs and the UltraSPARC-I. On E-Cache misses, this bus is an output, and supplies data to the E-Cache RAMs from one of its buffers. On E-Cache write-backs, data is transferred from the E-Cache RAMs on this bus into one of the UDB chip buffers. Two UDB chips, each handle half the width of the 128 bit data bus from the UltraSPARC-I and E-Cache. Non-cacheable loads and stores transfer data directly between the UltraSPARC-I and the UDB chips on this bus. Also, special ASI loads and stores from the UltraSPARC-I for writing/reading certain control/status registers on the UDB chip for enabling/disabling ECC will also be supported over this bus.
EDPAR[7:0]	I/O	The UDB chip does data transfers over this bus with both the E-Cache RAMs and the UltraSPARC-I. On E-Cache misses, this bus is an output, and supplies data to the E-Cache RAMs from one of its buffers. On E-Cache write-backs, data is transferred from the E-Cache RAMs on this bus into one of the UDB chip buffers. Two UDB chips, each handle half the width of the 128 bit data bus from the UltraSPARC-I and E-Cache. Non-cacheable loads and stores transfer data directly between the UltraSPARC-I and the UDB chips on this bus. Also, special ASI loads and stores from the UltraSPARC-I for writing/reading certain control/status registers on the UDB chip for enabling/disabling ECC will also be supported over this bus
SYSDATA[63:0]	I/O	The UDB chip does data transfers with the system interconnect over this bus. Data is transferred at the system interconnect clock rate.
SYSECC[7:0]	I/O	Eight ECC check bits for the 64-bit data being transferred will be generated by the UDB chip, for all UltraSPARC-I writes to the system interconnect, and the SYSECC bus will then be configured as an output. On input, good ECC check bits generated by slaves will be transferred to the UDB chip over this bus, and checked inside the UDB chip
UDB_CE	O	These are pins driven by the UDB to tell the UltraSPARC-I that it has detected a correctable ECC error on the data that it received from the interconnect, i.e. a single bit error.
UDB_UE	O	This pin is driven by the UDB chip to tell the UltraSPARC-I that it has detected an uncorrectable ECC error on the data that it received from the interconnect.
S_REPLY[3:0]	I	These pins are connected to an unidirectional4 bit bus that receives encoded acknowledges from the System Controller in response to an address transaction sent out by UltraSPARC-I.
SYSID[4:0]	I	This bus is used to convey a five-bit system node ID to the UDB chip from the system interconnect.
SYSCLK[1:0]	I	This is an input from the clock controller chip, and has the same frequency as the system clock. It is a differential, PECL clock
EXT_EVENT	I	This is an input signal used to indicate the clock should be stopped. It is a debug signal which is set inactive on production systems. This signal powers down the STP1080 when asserted.
PLL_BYPASS	I	When asserted this pin caused the phase-lock loop to be bypassed. The clock from the differential receiver is directly passed to the clock trunk.
RESET	I	This signal is asserted when an external reset request occurs.
UDB_CNTL[4:0]	I	These pins are used by the UltraSPARC-I to tell the UDB when to load its buffers from the external cache data bus and when to drive the content of these buffers on to this bus.
UDB_H	I	This pin is hardwired to VDD for UDB_h (the UDB chip for the most significant 72 bits) and to GND for UDB_l (the UDB chip for the least significant 72 bits).
EPD	I	This input from the CPU signals external power-down.
TDI	I	IEEE 1149 test data input. This pin is internally pulled to logic one when not driven.

SIGNAL DESCRIPTIONS (CONTINUED)

Symbol	Type	Name and Function
TDO	O	JTAG Interface. IEEE 1149 test data output. A three-state signal driven only when that TAP controller is in the shift-DR state
TMS	I	IEEE 1149 test mode select input. This pin is internally pulled to logic one when not driven.
TCK	I	IEEE 1149 test clock input. This pin if not hooked to a clock source must always be driven to a logic 1 or a logic 0.
$\overline{\text{TRST}}$	I	IEEE 1149 test reset input (active low). This pin is internally pulled to logic one when not driven.
SC_DATA_STALL	I	Input from system to indicate how long data from the system interface will be delayed.
SC_ECC_VALID	I	Input from the system to indicate when to ignore ECC of SYSDATA coming in from the UltraSPARC-I bus. When asserted, the STP1080 checks the ECC on SYSDATA, else SYSDATA ECC is ignored.
LF1	I	PLL loop filter output of charge pump.
LF2	I	PLL loop filter input pin to VCO.
LF3	I	Loop filter ground.
CLKCTL_CLKOUT	O	Output of the internal clock for characterization of clock in PLL or BYPASS mode.

TIMING CONSIDERATIONS

The UDB will not stall data delivery to UltraSPARC-I on a Correctable Error or an Uncorrectable Error.

The number of transaction cycles on the data bus are as follows:

- 1 for noncacheable stores (128 bits)
- 4 for mondo vectors (192 bits)
- 4 for cache lines (512 bits)

Following are timing diagrams of data transfers from the UPA to the CPU, and from the CPU to the UPA. Arrows indicate when data is registered at the UDB except when otherwise noted. Diagrams show timing for minimum latency.

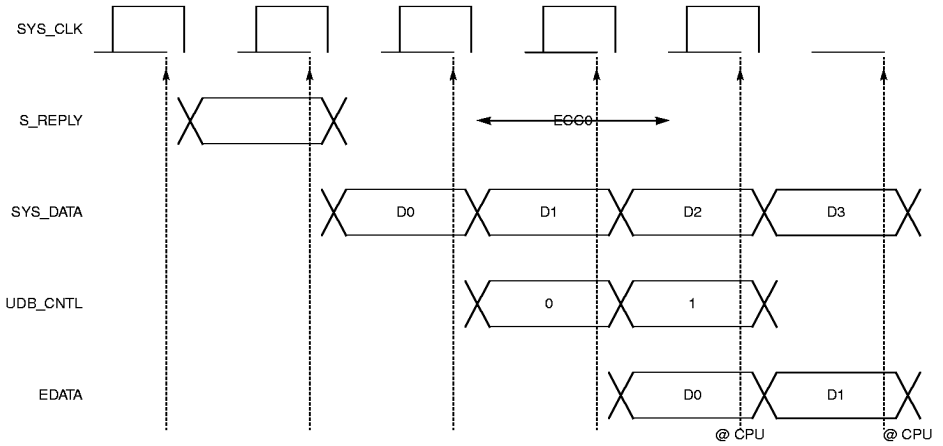


Figure 5. UPA to CPU Data Transfer Timing Diagram

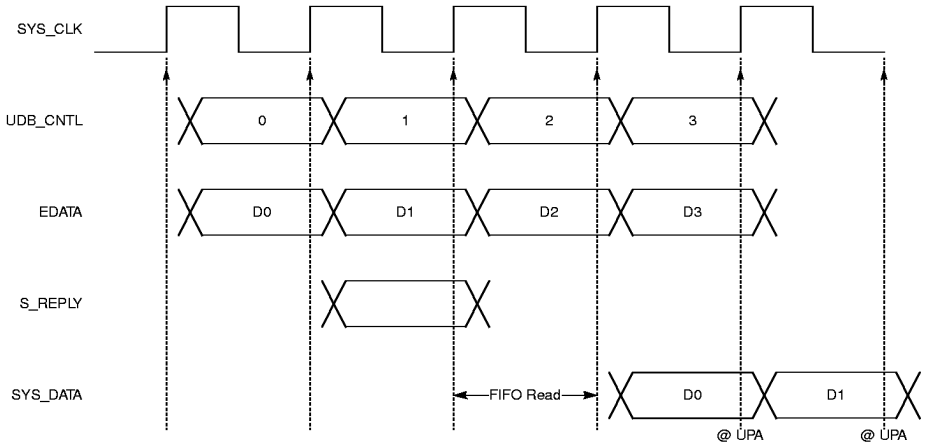


Figure 6. CPU to UPA Data Transfer Timing Diagram

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1] [2]

Symbol	Parameter	Rating	Units
V_{CC}	Supply voltage range	0 to 4.0	V
V_I	Input voltage range (Standard)	-0.5 to V_{CC} + 0.5	V
V_I	Input Voltage range (PECL)	V_{CC} - 2.0 to V_{CC} + 0.5	V
V_O	Output voltage range	-0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{CC})	±20	mA
	Current into any output in the low state	50	mA
T_{STG}	Storage temperature	-40 to 150	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Unless otherwise noted, all voltages are with respect at V_{SS}.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{SS}	Ground		–	0	–	V
V_{IH}	High-level input voltage	All except CLK	2.0	–	V_{CC} + 0.3	V
		CLK	V_{CC} - 1.35	–	V_{CC} - 0.70	V
V_{IL}	Low-level input voltage	All except CLK	-0.3	–	0.8	V
V_{IL}		CLK	V_{CC} - 2.0	–	V_{CC} - 1.55	V
I_{OH}	High-level output current		–	–	-4.0	mA
I_{OL}	Low-level output current		–	–	8.0	mA
T_J	Operating junction temperature		–	–	80	°C
T_A	Operating ambient temperature		0	–	[1]	°C

1. Maximum ambient temperature is limited by air flow such that the maximum junction temperature does not exceed T_J.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High-level output voltage	V_{CC} = Min, I_{OH} = Max	2.4	–	–	V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max	–	–	0.4	V
V_{IH}	High-level input voltage (except SYSCLK[1], SYSCLK[2])	V_{CC} = Max	2.0	–	–	V
	High -level input voltage (SYSCLK[1], SYSCLK[2)	V_{CC} = Max	V_{CC} - 1.35	–	V_{CC} - 0.70	V
V_{IL}	Low-level input voltage (except SYSCLK[1], SYSCLK[2)	V_{CC} = Min	–	–	0.8	V
	Low-level input voltage (SYSCLK[1], SYSCLK[2)	V_{CC} = Min	V_{CC} - 2.0	–	V_{CC} - 1.55	V
I_{DDD}	Supply current [1]	V_{CC} = Max, freq = 83MHz	-	-	1.0	A
I_{OZ}	High-impedance output current	V_{CC} = Max, V_O = V_{CC}	-10	–	10	µA
		V_{CC} = Max, V_O = V_{SS}	-10	–	10	µA
I_I	Input current	V_{CC} = Max, V_O = V_{SS} to V_{CC}	-10	–	10	µA
C_I	Input capacitance [2]		–	5	–	pF
C_O	Output capacitance [2]		–	10	–	pF

1. Assumes data being sent to the SYSTEM and CPU every four cycles on average.
2. This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.

AC Characteristics - Signal Timing (Except Clock and IEEE1149.1) [1]

Symbol	Parameter	Signals	Conditions	83 MHz		100 MHz		Units
				Min	Max	Min	Max	
t_{SU}	Input setup time to CLK	EDATA[63:0], EDPAR[7:0]	*Figure 8*	6.6	–	4.5	–	ns
t_H	Input hold time to CLK			0.3	–	0.3	–	ns
t_{SU}	Input setup time to CLK	SYSDATA[63:0], SYSECC(7:0), S_REPLY, SC_ECC_VALID		2.9	–	2.5	–	ns
t_H	Input hold time to CLK			0.9	–	0.9	–	ns
t_{SU}	Input setup time to CLK	UDB_CNTL[4:0]		6.6	–	4.5	–	ns
t_H	Input hold time to CLK			0.0	–	0.0	–	ns
t_{PD}	Output delay from CLK	EDATA[63:0], EDPAR[7:0], UE, CE	I_{OL} = 8 mA I_{OH} = -4 mA C_L = 35 pF V_{LOAD} = 1.5V *Figure 7*	–	7.7	–	6.8	ns
t_{OH}	Output hold time from CLK			0.8	–	0.8	–	ns
t_{PD}	Output delay from CLK	SYSDATA[63:0], SYSECC(7:0)		–	5.1	–	4.5	ns
t_{OH}	Output hold time from CLK			0.5	–	0.5	–	ns
t_{LOCK}	PLL acquisition time		*Figure 11*	7.0		7.0		µ
				1000		1000		cycle

1. All timing requirements are specified with PLL enabled.

AC Characteristics - Clock Timing

Symbol	Parameter	83 MHz			100 MHz			Units
		Min	Typ	Max	Min	Typ	Max	
t_{CYC} (CLK)	Processor clock cycle time [1]	12	–	–	10	–	–	ns
t_W(CLK)	Processor clock duty cycle [1]	40	50	60	40	50	60	%
t_{SLEW}(CLK)	Clock input slew rate [1]	TBD	–	–	TBD	–	–	V/ns
t_{CYC} (TCK)	TCK clock cycle time	30	–	--	30	–	--	ns
t_W(TCK)	TCK clock duty cycle	40	50	60	40	50	60	%
t_W ($\overline{\text{RESET}}$)	$\overline{\text{RESET}}$ pulse width LOCK MODE (See *Figure 9*)	10	–	–	10	–	–	ns
t_W (RESET)	RESET pulse width BYPASS MODE (See *Figure 9*)	t_{CYC} (CLK) x3	–	–	t_{CYC} (CLK) x3	–	–	ns
t_W($\overline{\text{TRST}}$)	$\overline{\text{TRST}}$ pulse width (See *Figure 9*)	10.5			10.5			ns

1. This is for the PLL enabled.

AC Characteristics - IEEE1149.1 Timing

Symbol	Parameter	Signals	Conditions	83 MHz			100 MHz			Units
				Min	Typ	Max	Min	Typ	Max	
t_{SU} (TRST)	Input setup time to TCK	TRST	*Figure 8*	10		–	10		–	ns
t_{SU} (TDI)	Input setup time to TCK	TDI			2	–		2	–	ns
t_{SU} (TMS)	Input setup time to TCK	TMS			2	–		2	–	ns
t_H(TRST)	Input hold time to TCK	TRST		10		–	10		–	ns
t_H(TDI)	Input hold time to TCK	TDI			2	–		2	–	ns
t_H(TMS)	Input hold time to TCK	TMS			2	–		2	–	ns
t_{PD}(TDO)	Output delay from TCK [1]	TDO	I_{OL} = 8 mA I_{OH} = -4 mA C_L = 35 pF V_{LOAD} =1.5V *Figure 7*		15	–		15	–	ns
t_{OH}(TDO)	Output hold time from TCK [1]	TDO		–	10	–	–	10	–	ns

1. TDO is referenced from falling edge of TCK.

AC Characteristics - T_{PD} (Output) Capacitive Derating Factor [1]

Symbol	Parameter	83 MHz			100 MHz			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Capacitive derating factor	0.2	0.3	0.4	TBD	TBD	TBD	ns/10pf

1. Derating factors are shown to aid in board design. This specification is not verified during manufacturing testing.

Loop Filter Values [1]

Frequency	Rs	Cs	Cp
83Mhz	18ohm	56nf	1.0nf

1. Loop filter values are given as an aid in board design. Values may need to be optimized for your particular application.

Thermal Resistance vs. Air Flow [1]

Symbol	Air Flow (ft/min)				Units
	100	200	300	500	
$Theta_{JA}$	TBD	TBD	TBD	TBD	(°C/W)

1. TJ can be calculated by: $T_J = T_A + P_D \times Theta_{JA}$.
Thermal resistance measured using UltraSPARC-I heatsink. P_D = Power Dissipation.

PARAMETER MEASUREMENT

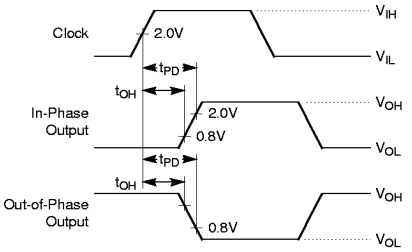


Figure 7. Voltage Waveforms - Propagation Delay Times

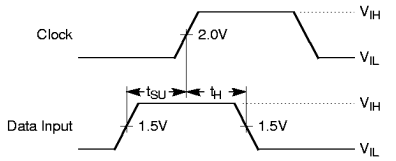


Figure 8. Voltage Waveforms - Setup and Hold Times

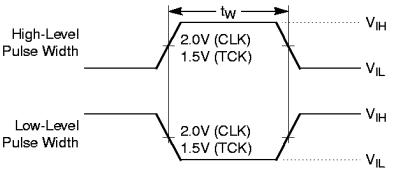


Figure 9. Voltage Waveforms - Clock Pulse Duration

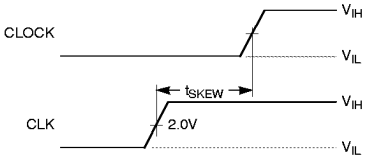


Figure 10. Voltage Waveforms - Clock Skew

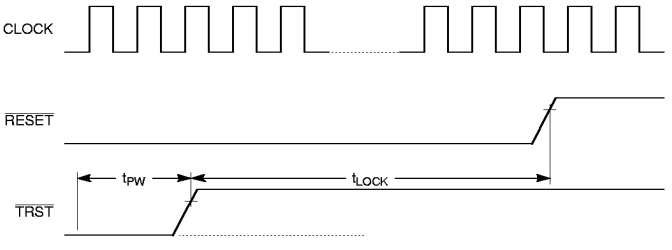


Figure 11. Reset Timing

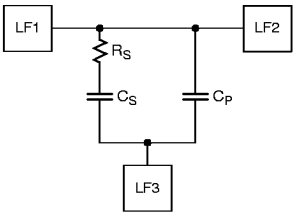


Figure 12. Loop Filter Configuration

PIN ASSIGNMENTS

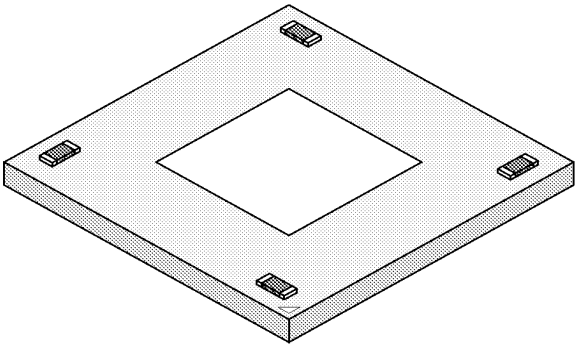
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
A4	EDATA[57]	C16	EDATA[42]	G20	VDD_C	N1	SYSDATA[8]	S20	VSS_C	W9	VDD_C
A5	EDATA[54]	C17	EDATA[40]	G21	EDATA[9]	N2	EDPAR[0]	S21	SYSDATA[35]	W10	SYSID[2]
A6	EDATA[51]	C18	VSS_O	G22	VDD_O	N3	EDATA[7]	S22	SYSDATA[34]	W11	SYSCLK[0]
A7	EDATA[49]	C19	EPD	G23	UDB_CNTL[3]	N4	VSS_C	S23	SYSDATA[33]	W12	APLL_VDD
A8	EDATA[31]	D4	EDATA[56]	H1	EDATA[33]	N20	SYSDATA[7]	T1	SYSDATA[44]	W13	VDD_C
A9	EDATA[28]	D5	VSS_O	H2	VDD_O	N21	VDD_O	T2	SYSDATA[45]	W14	SYSDATA[48]
A10	EDATA[27]	D6	EDATA[53]	H3	EDATA[34]	N22	SYSDATA[6]	T3	VSS_O	W15	S_REPLY[1]
A11	EDATA[24]	D7	VDD_C	H4	EDATA[35]	N23	SYSDATA[5]	T4	SYSDATA[46]	W16	VDD_O
A12	EDATA[20]	D8	EDATA[48]	H20	UDB_CNTL[2]	P1	SYSDATA[11]	T20	SYSDATA[32]	W17	SYSDATA[52]
A13	EDATA[17]	D9	EDATA[30]	H21	VSS_O	P2	SYSDATA[10]	T21	VSS_O	W18	VDD_O
A14	EDATA[47]	D10	EDATA[25]	H22	EDATA[8]	P3	VSS_O	T22	SYSDATA[63]	W19	SYSDATA[58]
A15	EDATA[44]	D11	VSS_C	H23	UDB_UE	P4	SYSDATA[9]	T23	SYSDATA[62]	W20	VSS_O
A16	EDATA[41]	D12	EDATA[22]	J1	EDATA[36]	P20	VDD_C	U1	SYSDATA[47]	X5	VSS_O
A17	$\overline{\text{TRST}}$	D13	EDATA[19]	J2	EDATA[37]	P21	SYSDATA[4]	U2	SYSDATA[16]	X6	SYSDATA[23]
A18	TCK	D14	VDD_C	J3	VSS_O	P22	SYSDATA[3]	U3	SYSDATA[17]	X7	SYSDATA[26]
A19	UDB_H	D15	EDATA[46]	J4	EDATA[38]	P23	SYSDATA[2]	U4	VSS_C	X8	VDD_O
B4	VSS_O	D16	EDATA[43]	J20	UDB_CNTL[0]	Q1	SYSDATA[12]	U20	VDD_O	X9	$\overline{\text{RESET}}$
B5	EDATA[55]	D17	VSS_C	J21	UDB_CNTL[1]	Q2	VDD_O	U21	SYSDATA[61]	X10	VSS_C
B6	EDATA[52]	D18	TDI	J22	VSS_C	Q3	SYSDATA[13]	U22	VSS_O	X11	PECL_VDD
B7	VSS_O	D19	VDD_C	J23	UDB_CE	Q4	SYSDATA[14]	U23	SYSDATA[60]	X12	LF3
B8	EDPAR[3]	D20	EDATA[15]	K1	EDATA[39]	Q20	SYSDATA[1]	V1	SYSDATA[19]	X13	APLL_VSS
B9	VDD_O	D21	VSS_O	K2	EDPAR[4]	Q21	VSS_O	V2	VSS_O	X14	EXT_EVENT
B10	EDATA[26]	D22	VDD_O	K3	EDATA[0]	Q22	SYSDATA[0]	V3	VDD_O	X15	VDD_C

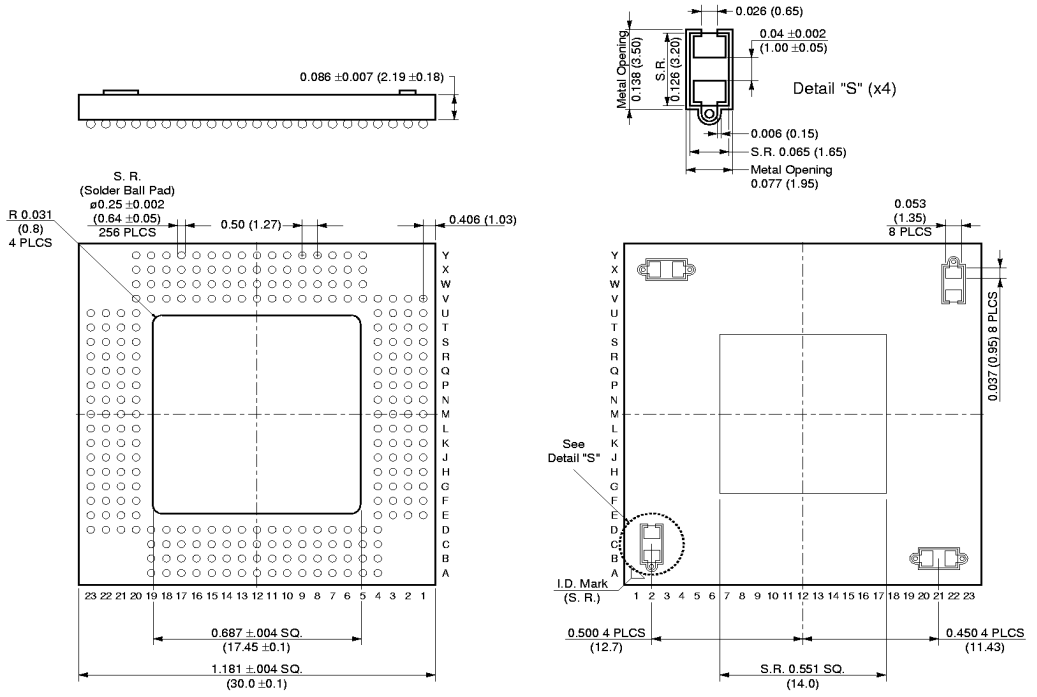
PIN ASSIGNMENTS (CONTINUED)

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
B11	EDPAR[2]	D23	EDPAR[1]	K4	VDD_C	Q23	SYSDATA[39]	V4	SYSDATA[18]	X16	S_REPLY[2]
B12	VSS_O	E1	EDATA[58]	K20	SYSECC[6]	R[1]	SYSDATA[15]	V5	VDD_O	X17	VSS_O
B13	EDATA[18]	E2	VSS_O	K21	VDD_C	R2	SYSDATA[40]	V6	SYSDATA[24]	X18	SYSDATA[54]
B14	EDPAR[5]	E3	EDATA[59]	K22	SC_ECC_VALID	R3	VSS_O	V7	VSS_O	X19	SYSDATA[57]
B15	EDATA[45]	E4	VDD_O	K23	SYSECC[7]	R4	SYSDATA[41]	V8	SYSDATA[30]	X20	VDD_O
B16	VDD_O	E20	VDD_O	L1	EDATA[1]	R20	SYSDATA[38]	V9	SYSID[0]	Y5	SYSDATA[20]
B17	TDO	E21	EDATA[14]	L2	EDATA[2]	R21	SYSDATA[37]	V10	SYSID[3]	Y6	SYSDATA[22]
B[18]	TMS	E22	EDATA[13]	L3	VDD_O	R22	VDD_O	V11	SYS_CLK[1]	Y7	SYSDATA[25]
B19	VSS_C	E23	EDATA[12]	L4	EDATA[3]	R23	SYSDATA[36]	V12	PECL_VSS	Y8	SYSDATA[28]
C4	VDD_O	F1	EDATA[60]	L20	VSS_C	S1	SYSDATA[42]	V13	PLL_BYPASS	Y9	SYSDATA[31]
C5	EDPAR[6]	F2	EDATA[61]	L21	SYSECC[3]	S2	VDD_O	V14	VDD_C	Y10	SYSID[1]
C6	VDD_O	F3	VSS_O	L22	SYSECC[4]	S3	SYSDATA[43]	V15	SYSDATA[49]	Y11	SYSID[4]
C7	EDATA[50]	F4	EDATA[62]	L23	SYSECC[5]	S4	VDD_C	V16	S_REPLY[3]	Y12	LF1
C8	VDD_O	F20	EDATA[11]	M1	EDATA[4]	S20	VSS_C	V17	VSS_C	Y13	LF2
C9	EDATA[29]	F21	VSS_O	M2	VSS_O	S21	SYSDATA[35]	V18	SYSDATA[55]	Y14	SC_DATA_STALL
C10	VSS_O	F22	UDB_CNTL[4]	M3	EDATA[5]	S22	SYSDATA[34]	V19	VDD_C	Y15	S_REPLY[0]
C11	EDATA[23]	F23	EDATA[10]	M4	EDATA[6]	S23	SYSDATA[33]	V20	SYSDATA[59]	Y16	SYSDATA[50]
C12	EDATA[21]	G1	EDATA[63]	M20	SYSECC[2]	S1	SYSDATA[42]	W5	SYSDATA[21]	Y17	SYSDATA[51]
C13	VDD_O	G2	EDPAR[7]	M21	SYSECC[1]	S2	VDD_O	W6	VSS_O	Y18	SYSDATA[53]
C14	EDATA[16]	G3	EDATA[32]	M22	VSS_O	S3	SYSDATA[43]	W7	SYSDATA[27]	Y19	SYSDATA[56]
C15	VSS_O	G4	VDD_O	M23	SYSECC[0]	S4	VDD_C	W8	SYSDATA[29]	Y20	CLKCTL_CLKOUT

PACKAGE DIMENSIONS

256-Pin PBGA Package





Notes: 1. S.R.: Solder Mask Resist Opening
2. All Dimensions are in Inches. Dimensions in parenthesis ( ) are in millimeters.
3. On the solder ball pad side, thermal via holes are covered with photo imagable solder mask.
4. There is plating (NI, Au) on bondfingers, metalized area for heat sink attachment and other exposed metal.
5. Two chip caps are attached to VSSC/VDDC planes. The other two chip caps are attached to VSSO/VDDO planes
6. Flatness of package surface on ball side: 0.005 inch (0.127 mm) per package.

ORDERING INFORMATION

Part Number	Speed	Description
STP1080ABGA-83	83 MHz	UltraSPARC-I Data Buffer for 167 MHz UltraSPARC-I Systems
STP1080ABGA-100	100 MHz	UltraSPARC-I Data Buffer for 200 MHz UltraSPARC-I Systems

Document Part Number: 802-7956-02