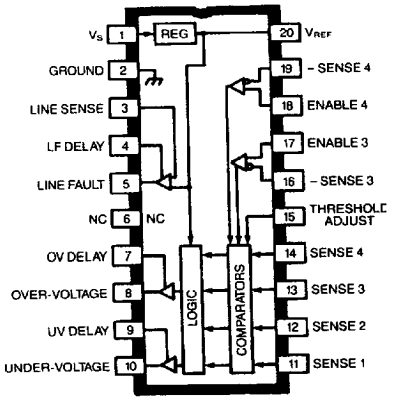
PRECISION SUPERVISORY SYSTEMS MONITOR

ULN8131A



Dwg. No. W-185

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **35 V**
Power Dissipation, P_D . . . . . **1.1 W**
Operating Temperature Range,
T_A . . . . . **0°C to +70°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**
Junction Temperature, T_J . . . . . **+150°C**

Capable of monitoring four dc power lines, the ULN8131A and ULN8131LW are power-fault monitors for both under-voltage and over-voltage conditions. Two of the four inputs are designed to monitor positive voltages, while the other two inputs can be used to monitor positive or negative voltages. Typical examples might be a +5 V logic supply, +15 V and -15 V analog supplies, and a positive peripheral power load supply. The primary power line is monitored by an additional comparator and will provide early warning of line voltage drop-out.

During low-supply voltage operations, an under-voltage lockout, which monitors the ULN8131A/LW internal supply, prevents false outputs from occurring. The logic outputs can be used to operate LEDs or other low-voltage indicators.

The circuit configuration of the ULN8131A/LW allows easy programming of over-voltage thresholds which are referenced to a 1% trimmed 2.5 V bandgap reference. The UV FAULT (pin 10) is initiated by one or more of the four sense inputs falling below the UV trip point (the internal reference voltage). The OV FAULT (pin 8) is activated by one or more of the sense inputs rising above the externally set (pin 15) OV trip point. The LINE OK output (pin 5) will remain high as long as the LINE SENSE input (pin 3) is above the internal voltage. The LINE SENSE will accept a positive dc voltage proportional to either the high-voltage master bus or the ac line.

continued next page...

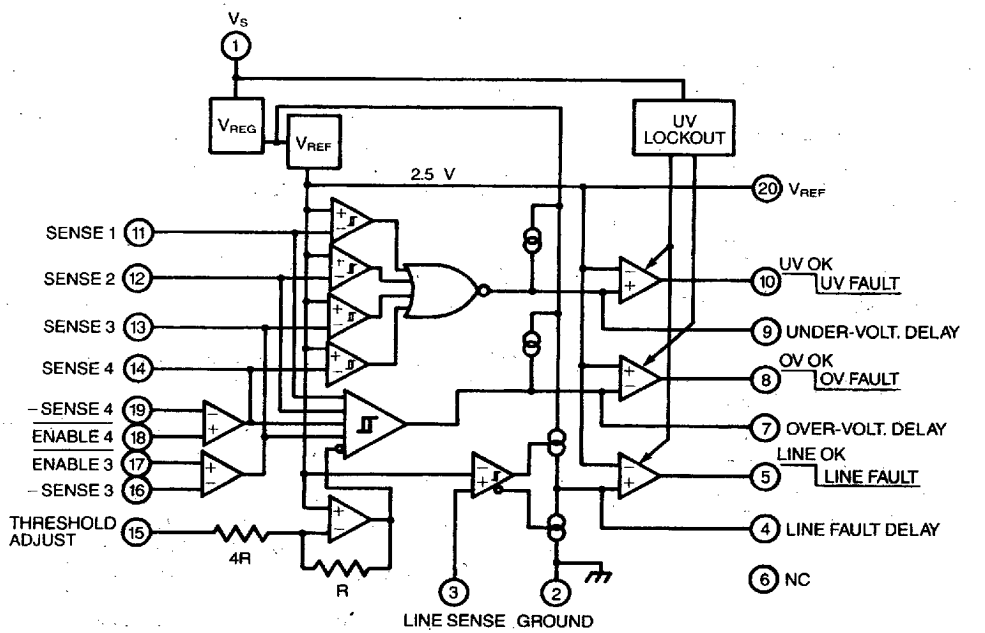
FEATURES

- Monitors Four DC Supplies
- V_S Under-Voltage Lockout
- Fixed Under-Voltage Threshold
- Low Standby Current
- Line Sense Input
- Programmable Over-Voltage Threshold
- Pull-Up Clamped Outputs
- Programmable Output Delays
- 10 to 35 Volts Operation
- Reference Trimmed to 1%
- Separate Under-Voltage Comparators

Always order by complete part number:

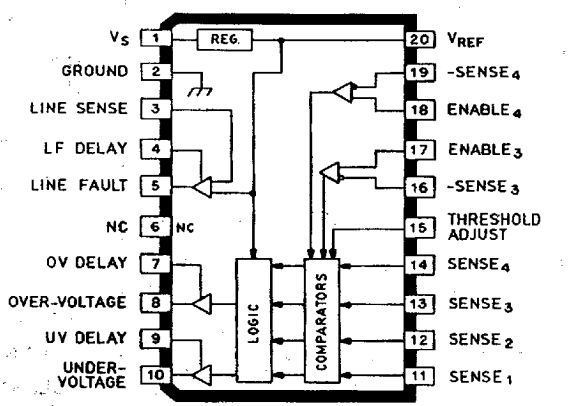
Part Number	Package
ULN8131A	20-Pin DIP
ULN8131LW	20-Lead SOIC

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. W-186

ULN8131LW



Dwg. No. A-14,372

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 15 V

Characteristic	Test Pin	Test Conditions	Limits Min.	Limits Max.	Units
Functional V_S Range	1		10	35	V
Quiescent Current	1	V_S = 35 V, $V_{17} = V_{18} = V_{20}$ No Fault	—	15	mA
REFERENCE VOLTAGE SECTION					
Reference Voltage	20	No Load, T_A = +25°C	2.47	2.53	V
		No Load, Change Over Temp.	—	25	mV
Load Regulation	20	I_{REF} = 0 to 10 mA	—	20	mV
Line Regulation	20	V_S = 10 to 35 V	—	10	mV
Ripple Rejection	20	f = 120 Hz	60	—	dB
Short-Circuit Current Protection	20		—	40	mA
COMPARATOR SECTION					
Under-Voltage Trip Points	11-14*	T_A = +25°C	2.47	2.53	V
		Over Temperature	2.46	2.54	V
Under-Voltage Trip Hysteresis	11-14*	Over Temperature	10	25	mV
Over-Voltage Trip Points	11-14*	V_{15} = 0	3.08	3.17	V
Over-Voltage Trip Hysteresis	15	V_{15} = 0 to 2.5 V, Over Temp.	10	25	mV
Line Monitor Trip Threshold	3		2.40	2.54	V
Under-Voltage Lockout Enable	1	V_S Decreasing	8.5	—	V
Under-Voltage Lockout Disable	1	V_S Increasing	—	10.5	V
Input Bias Current	3, 11, 12	V_{IN} = 2.0 V	—	-6.0	µA
		V_{IN} = 3.0 V	—	6.0	µA
	15	V_{IN} = 0	—	-50	µA
	16, 19	V_{IN} = -2.0 V, $V_{17} = V_{18}$ = 0 V	—	-2.0	µA
OUTPUT DRIVERS					
Output Saturation Voltage	5, 10	I_{SINK} = 5.0 mA	—	0.5	V
	8	I_{SINK} = 10 mA	—	0.5	V
	5, 8, 10	I_{SOURCE} = 500 µA	4.0	5.25	V
Output Leakage current	5, 8, 10	V_{OUT} = 35 V	—	50	µA
Line Fault Delay Current Source	4	V_4 = 2.0 V	160	350	µA
Line Fault Delay Current Sink	4	V_4 = 2.0 V	3.2	7.0	mA
Over-Voltage Delay Current Source	7	V_7 = 2.0 V	160	300	µA
Under-Voltage Delay Current Source	9	V_9 = 2.0 V	35	75	µA

*All inputs connected to 2.75 V except input being tested.

APPLICATIONS

The basic voltage monitors are based on a 2.5 V precision bandgap reference. External resistive dividers are used to present a nominal 2.5 V level to each under-voltage comparator at the minimum allowable under-voltage condition. The over-voltage reference is set up by another resistive divider at pin 15 determined by the tightest over-voltage tolerance requirement.

BASIC FORMULAS:

1. An under-voltage fault is detected, (pin 10 goes low), when the positive input voltage being monitored is less than:

$$V_{MON(LO)} = 2.5\ (R_1 + R_2)/R_2$$

2. The internal over-voltage threshold is defined as:

$$V_{OVT} = 2.5 \left[1 + \frac{R_A}{4(R_A + R_B)}\right]$$

where $R_A//R_B << 100\ k\Omega$.

3. An over-voltage fault is detected when the positive input voltage being monitored exceeds:

$$V_{MON(HI)} = V_{OVT}\ (R_1 + R_2)/R_2$$

4. Individual over-voltage thresholds can be increased by the addition of R_X with

$$R_X = R_1 \left[\frac{V_{OVT} - 2.5}{V_{MON(HI)} - V_{OVT}\left(\frac{R_1 + R_2}{R_2}\right)}\right]$$

5. To monitor negative supplies at SENSE 3 or SENSE 4, pin 17 or 18, respectively, is connected to ground. In this condition, an under-voltage fault indication will occur when the negative supply being monitored falls below:

$$V_{MON(LO)} = 2.5\ R_3/R_4$$

Note that for monitor purposes, under-voltage means the negative supply is actually going net positive, or toward ground.

6. For negative supplies, an over-voltage fault indication will occur when:

$$V_{MON(HI)} = V_{OVT}\ R_3/R_4$$

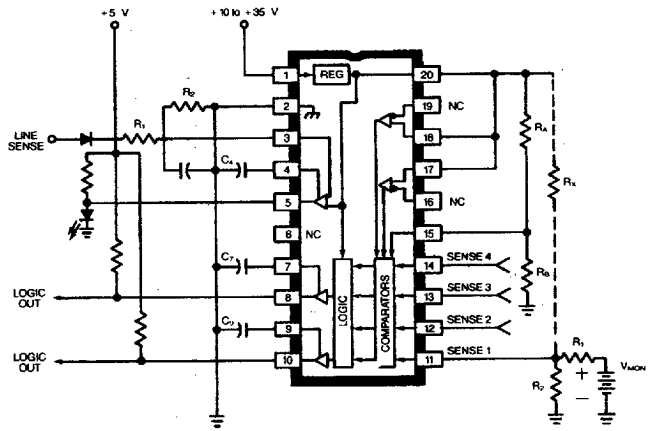
7. Fault delay capacitor values are determined by:

$$C_4 \text{ or } C_7 = \frac{200 \times 10^{-6} \times t}{2.5}$$

$$C_9 = \frac{55 \times 10^{-6} \times t}{2.5}$$

where t is the output delay in seconds.

LINE SENSE AND POSITIVE SUPPLY MONITORING (SENSE 1, 2, 3, and 4)



UNUSED INPUTS

Unused positive sense channel inputs (pins 3, 11-14) must not be left unconnected. They cannot be tied high (over-voltage fault indication), tied low (under-voltage fault indication), or tied to the internal reference (susceptible to noise and voltage offsets). Unused sense channel inputs should be connected to any operating sense channel input. For example, if channels 1, 2, and 4 are being used, the unused channel 3 sense input (pin 13) should be connected to the SENSE 2 or SENSE 4 input.

Unused negative sense channel inputs (pins 16 and 19) can be left open-circuited *provided* the associated ENABLE inputs (pins 17 and 18) are tied high and the associated positive sense channel inputs (pins 13 and 14) are utilized to monitor positive supplies or are connected as described above.

DESIGN EXAMPLE

As an example, consider the following set of monitoring conditions:

V_1 = +5 V (+10%, -5%)

V_2 = +12 V (±10%)

V_3 = +15 V (±5%)

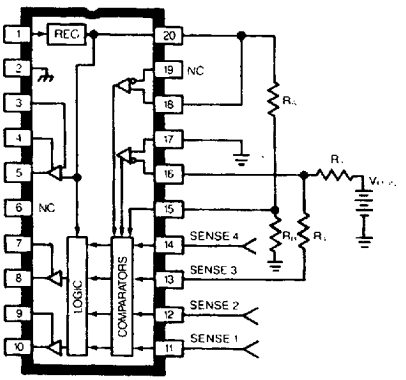
V_4 = +24 V (±10%)

The required input dividers are calculated per (1) to yield the resistor divider ratios, $R_2(R_1 + R_2)$, of: 0.5263, 0.2315, 0.1754 (Note 1), and 0.1157 respectively. The over-voltage threshold, V_{OVT}, would be dictated by the tightest tolerance supply which gives the lowest V_{OVT} from (3). Therefore, $V_{MON(HI)}$ = 15 x 1.05 = 15.75 V and V_{OVT} = 15.75 x 0.1754 = 2.763 V[1]. This is the voltage appearing at the SENSE terminal and is equal to the over-voltage threshold to be set via the resistor ratio at pin 15. From (2) $R_A/(R_A + R_B)$ is calculated to be 0.4096. It is good practice to keep the equivalent external impedances as low as possible, in order to minimize bias current and offset errors. For the purpose of this example, all resistor dividers will be taken to have an equivalent impedance of 1000 ohms. This being the case, the final values are:

R_A = 1.7 kΩ and R_B = 2.44 kΩ.

In order to provide accurate over-voltage sensing for the V_1, V_2, and V_4 supplies, resistors are connected from the respective input sense nodes and returned to the 2.5 V reference. Calculation is made by first picking values for the input dividers and then calculating the required value of R_X from (4). Again, assuming 1 kΩ equivalent divider

NEGATIVE SENSE MONITORING
SENSE 3 and 4 Only



Dwg. No. W-187

impedances and making the calculations, a summary of results is given below.

MONITORED SUPPLY	$V_{MON(HI)}$	$V_{MON(LO)}$	R_1	R_2	R_X
+5 V (+10%, -5%)	5.5 V	4.75 V	1.90 kΩ	2.11 kΩ	2.0 kΩ
+12 V (±10%)	13.2 V	10.8 V	4.32 kΩ	1.30 kΩ	900 Ω
+15 V (±5%)	15.75 V	14.25 V	5.70 kΩ	1.21 kΩ	∞
+24 V (±10%)	26.4 V	21.6 V	8.64 kΩ	1.13 kΩ	900 Ω

1. Note that the number 0.1754 is rounded off. Due to required accuracies in the external dividers, round off numbers only after final resistor values are calculated. For the same reason, use stable high-accuracy metal film resistors. Many applications may benefit from combining the ULN8131A and functionally trimmed resistor-capacitor networks.