NEC

MOS INTEGRATED CIRCUIT
μPD78P4038

16/8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78P4038, 78K/IV Series' product, is a one-time PROM or EPROM version of the μPD784035, μPD784036, μPD784037, and μPD784038 with internal masked ROM.

Since user programs can be written to PROM, this microcontroller is best suited for evaluation in system development, manufacture of small quantities of multiple products, and fast start-up of applications.

For specific functions and other detailed information, consult the following user's manual.
This manual is required reading for design work.

μPD784038, 784038Y Subseries User's Manual, Hardware : U11316E
78K/IV Series User's Manual, Instruction : U10905E

FEATURES

- Compatible with the μPD78P238, μPD78P4026, and μPD78P4038Y
- Internal PROM: 128 Kbytes
  - μPD78P4038KK-T : EPROM (best suited for system evaluation)
  - μPD78P4038GC-3B9 : One-time PROM (best suited for manufacture of small quantities)
    μPD78P4038GC-8BT : One-time PROM (best suited for manufacture of small quantities)
    μPD78P4038GK-BE9 : One-time PROM (best suited for manufacture of small quantities)
- Internal RAM : 4,352 bytes
- Power supply voltage : V_{DD} = 2.7 to 5.5 V
- QTOP^{TM} microcomputer (In the planning phase)

Remark The QTOP microcomputer is a microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification.

ORDERING INFORMATION

	Part number	Package	Internal ROM
	μPD78P4038GC-3B9	80-pin plastic QFP (14 × 14 × 2.7 mm)	One-time PROM
★	μPD78P4038GC-×××-3B9	80-pin plastic QFP (14 × 14 × 2.7 mm)	One-time PROM (QTOP microcomputer)
	μPD78P4038GC-8BT	80-pin plastic QFP (14 × 14 × 1.4 mm)	One-time PROM
	μPD78P4038GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	One-time PROM
★	μPD78P4038GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	One-time PROM (QTOP microcomputer)
	μPD78P4038KK-T	80-pin ceramic WQFN (14 × 14 mm)	EPROM

In this reference, all ROM components that are common to one-time PROM and EPROM are referred to as PROM.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

QUALITY GRADE

	Part number	Package	Quality grade
	μPD78P4038GC-3B9	80-pin plastic QFP (14 × 14 × 2.7 mm)	Standard (for general electronic equipment)
★	μPD78P4038GC-××-3B9	80-pin plastic QFP (14 × 14 × 2.7 mm)	Standard (for general electronic equipment)
	μPD78P4038GC-8BT	80-pin plastic QFP (14 × 14 × 1.4 mm)	Standard (for general electronic equipment)
	μPD78P4038GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	Standard (for general electronic equipment)
★	μPD78P4038GK-××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	Standard (for general electronic equipment)
	μPD78P4038KK-T	80-pin ceramic WQFN (14 × 14 mm)	Not applied (for function evaluation)

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

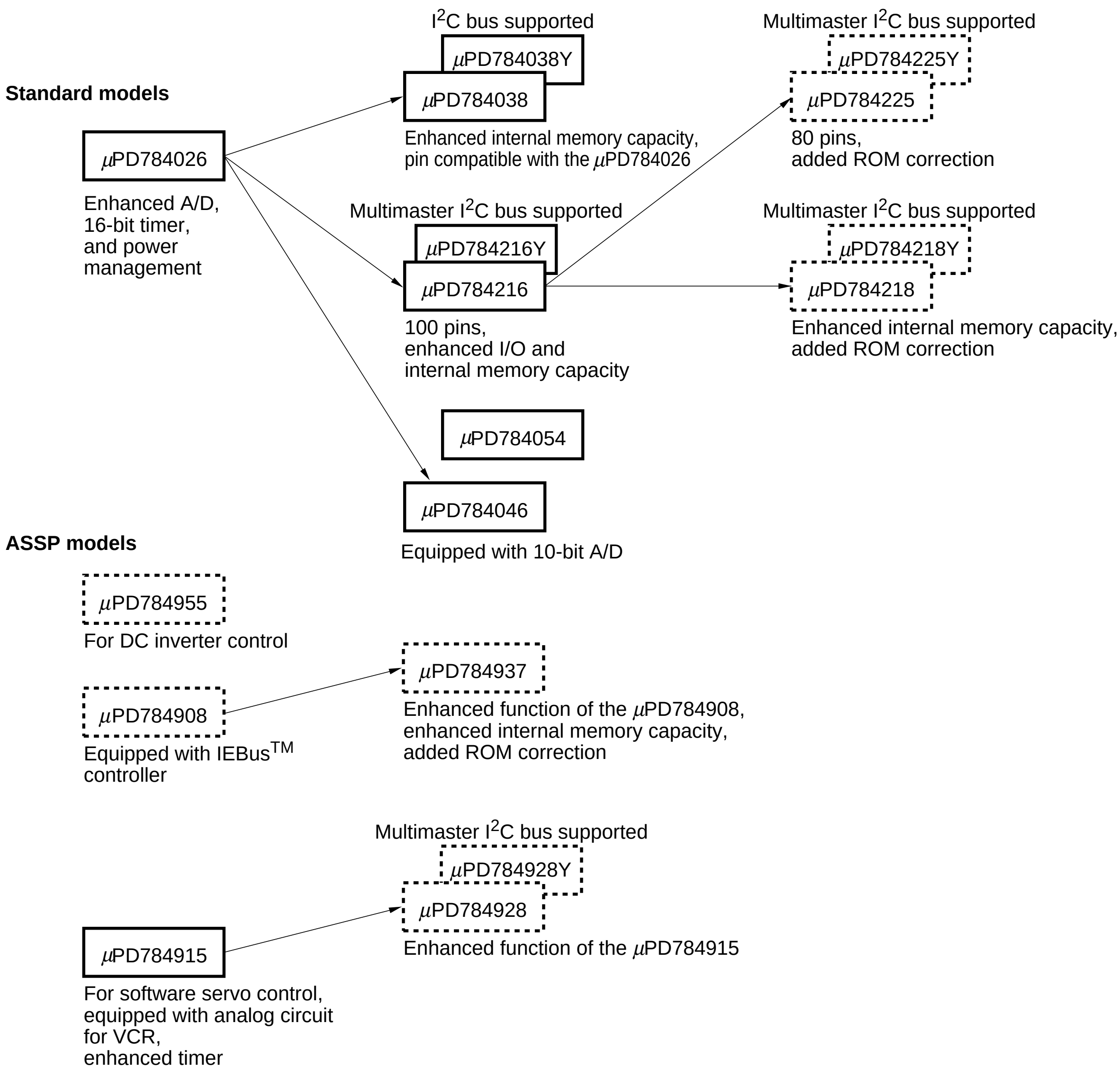
Caution The EPROM versions of the μPD78P4038 are not intended for use in mass-produced products; they do not have reliability high enough for such purposes. Their use should be restricted to functional evaluation in experiment or trial manufacture.

Remark ×× indicates ROM code suffix.

★ ## 78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM

: Under mass production

: Under development



FUNCTIONS

(1/2)

Item			Functions
Number of basic instructions (mnemonics)			113
General-purpose register			8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)
Minimum instruction execution time			125 ns/250 ns/500 ns/1,000 ns (at 32 MHz)
Internal memory	PROM		128 Kbytes (Can be changed to 48 K, 64 K, or 96 Kbytes by software)
	RAM		4,352 bytes (Can be changed to 2,048 or 3,584 bytes by software)
Memory space			Program and data: 1 Mbyte
I/O ports	Total		64
	Input		8
	Input/output		56
	Additional function pins[Note]	Pins with pull-up resistor	54
		LED direct drive outputs	24
		Transistor direct drive	8
Real-time output ports			4 bits × 2, or 8 bits × 1
Timer/counter			Timer/counter 0: (16 bits): Timer register × 1 Capture register × 1 Compare register × 2 Pulse output capability • Toggle output • PWM/PPG output • One-shot pulse output
			Timer/counter 1: (8/16 bits): Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1 Pulse output capability • Real-time output (4 bits × 2)
			Timer/counter 2: (8/16 bits): Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1 Pulse output capability • Toggle output • PWM/PPG output
			Timer 3 (8/16 bits): Timer register × 1 Compare register × 1
PWM outputs			12-bit resolution × 2 channels
Serial interface			UART/IOE (3-wire serial I/O): 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O, 2-wire serial I/O): 1 channel
A/D converter			8-bit resolution × 8 channels
D/A converter			8-bit resolution × 2 channels

Note Additional function pins are included in the I/O pins.

(2/2)

Item		Functions
Clock output		Selected from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (can be used as a 1-bit output port)
Watchdog timer		1 channel
Standby		HALT/STOP/IDLE mode
Interrupt	Hardware source	23 (16 internal, 7 external (sampling clock variable input: 1))
	Software source	BRK instruction, BRKCS instruction, operand error
	Nonmaskable	1 internal, 1 external
	Maskable	15 internal, 6 external
		• 4-level programmable priority • 3 operation statuses: vectored interrupt, macro service, context switching
Supply voltage		V_{DD} = 2.7 to 5.5 V
Package		80-pin plastic QFP (14 × 14 × 2.7 mm) 80-pin plastic QFP (14 × 14 × 1.4 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm) 80-pin ceramic WQFN (14 × 14 mm)

CONTENTS

1. DIFFERENCES BETWEEN μPD78P4038 AND MASKED ROM PRODUCTS

The μPD78P4038 is produced by replacing the masked ROM in the μPD784035, μPD784036, μPD784037, or μPD784038 with PROM to which data can be written. The functions of the μPD78P4038 are the same as those of the μPD784035, μPD784036, μPD784037, or μPD784038 except for the PROM specification such as writing and verification, except that the PROM size can be changed to 48 K, 64 K, or 96 Kbytes, and except that the internal RAM size can be changed to 2,048 or 3,584 bytes.

Table 1-1 shows the differences between these products.

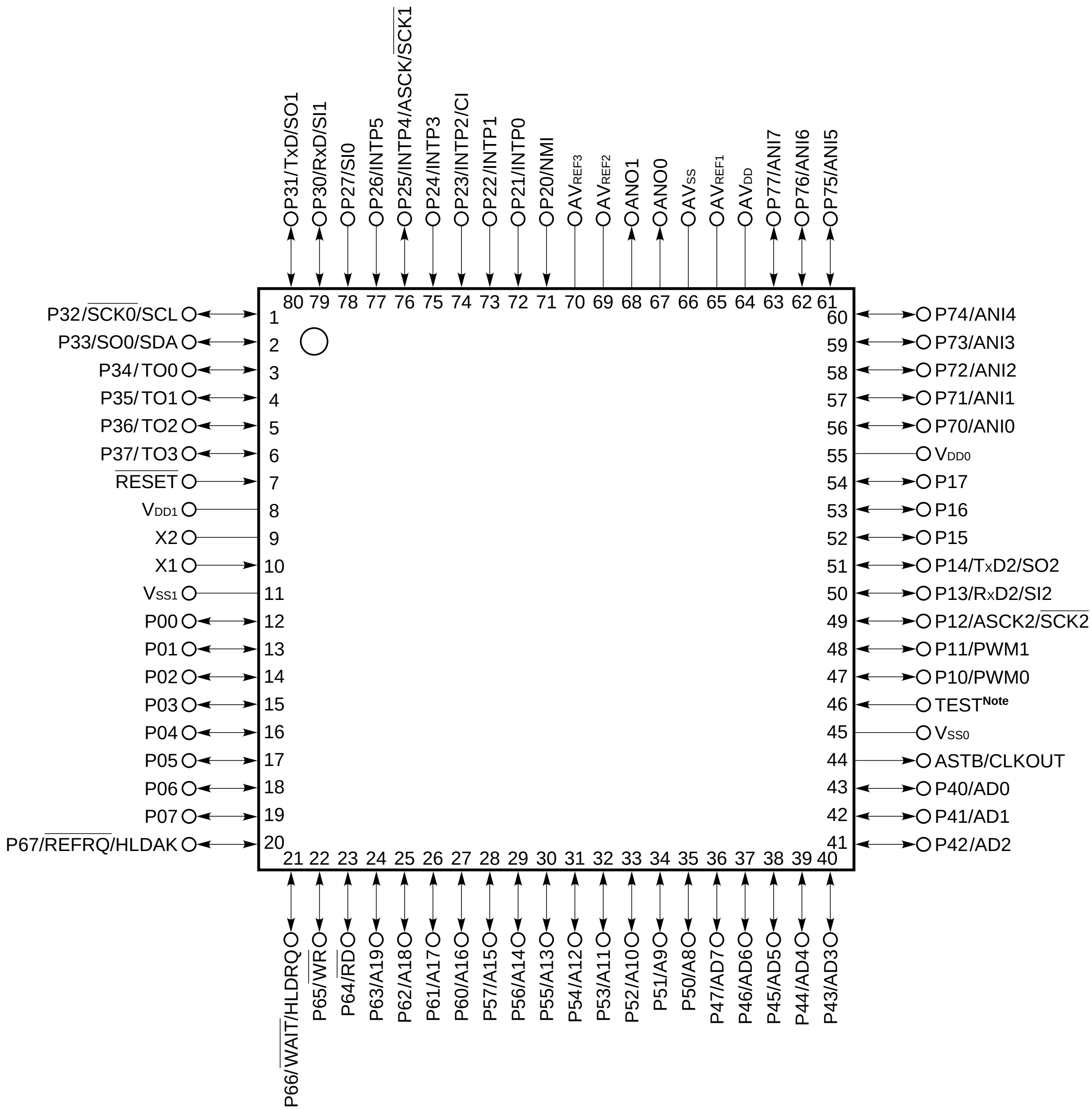
Table 1-1. Differences between the μPD78P4038 and Masked ROM Products

<table>
<tr><th>Item \ Product Name</th><th>μPD78P4038</th><th>μPD784035</th><th>μPD784036</th><th>μPD784037</th><th>μPD784038</th></tr>
<tr><td>Internal program memory</td><td>• 128-Kbyte PROM
• Can be changed to 48 K, 64 K, or 96 Kbytes by IMS</td><td>• 48-Kbyte masked ROM</td><td>• 64-Kbyte masked ROM</td><td>• 96-Kbyte masked ROM</td><td>• 128-Kbyte masked ROM</td></tr>
<tr><td>Internal RAM</td><td>• 4,352-byte internal RAM
• Can be changed to 2,048 or 3,584 bytes by IMS</td><td colspan="2">• 2,048-byte internal RAM</td><td>• 3,584-byte internal RAM</td><td>• 4,352-byte internal RAM</td></tr>
<tr><td rowspan="2">Package</td><td colspan="5">• 80-pin plastic QFP (14 × 14 × 2.7 mm)
• 80-pin plastic QFP (14 × 14 × 1.4 mm)
• 80-pin plastic TQFP (fine pitch) (12 × 12 mm)</td></tr>
<tr><td>80-pin ceramic WQFN (14 × 14 mm)</td><td colspan="4"></td></tr>
</table>

2. PIN CONFIGURATION (TOP VIEW)

(1) Normal operating mode

- **80-pin plastic QFP (14 × 14 × 2.7 mm)**
★ μPD78P4038GC-3B9, μPD78P4038GC-××× -3B9
- **80-pin plastic QFP (14 × 14 × 1.4 mm)**
μPD78P4038GC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
★ μPD78P4038GK-BE9, μPD78P4038GK-×××-BE9
- **80-pin ceramic WQFN (14 × 14 mm)**
μPD78P4038KK-T



Note Connect the TEST pin to V_{SS0} directly.

A8-A19	:	Address bus	P60-P67	:	Port 6
AD0-AD7	:	Address/data bus	P70-P77	:	Port 7
ANI0-ANI7	:	Analog input	PWM0, PWM1	:	Pulse width modulation output
ANO0, ANO1	:	Analog output	$\overline{\text{RD}}$	:	Read strobe
ASCK, ASCK2	:	Asynchronous serial clock	$\overline{\text{REFRQ}}$	:	Refresh request
ASTB	:	Address strobe	$\overline{\text{RESET}}$	:	Reset
AV_{DD}	:	Analog power supply	RxD, RxD2	:	Receive data
AV_{REF1}-AV_{REF3}	:	Reference voltage	$\overline{\text{SCK0}}$-$\overline{\text{SCK2}}$	:	Serial clock
AV_{SS}	:	Analog ground	SCL	:	Serial clock
CI	:	Clock input	SDA	:	Serial data
CLKOUT	:	Clock output	SI0-SI2	:	Serial input
HLDAK	:	Hold acknowledge	SO0-SO2	:	Serial output
HLDRQ	:	Hold request	TEST	:	Test
INTP0-INTP5	:	Interrupt from peripherals	TO0-TO3	:	Timer output
NMI	:	Non-maskable interrupt	TxD, TxD2	:	Transmit data
P00-P07	:	Port 0	V_{DD0}, V_{DD1}	:	Power supply
P10-P17	:	Port 1	V_{SS0}, V_{SS1}	:	Ground
P20-P27	:	Port 2	$\overline{\text{WAIT}}$	:	Wait
P30-P37	:	Port 3	$\overline{\text{WR}}$	:	Write strobe
P40-P47	:	Port 4	X1, X2	:	Crystal
P50-P57	:	Port 5			

(2) PROM programming mode

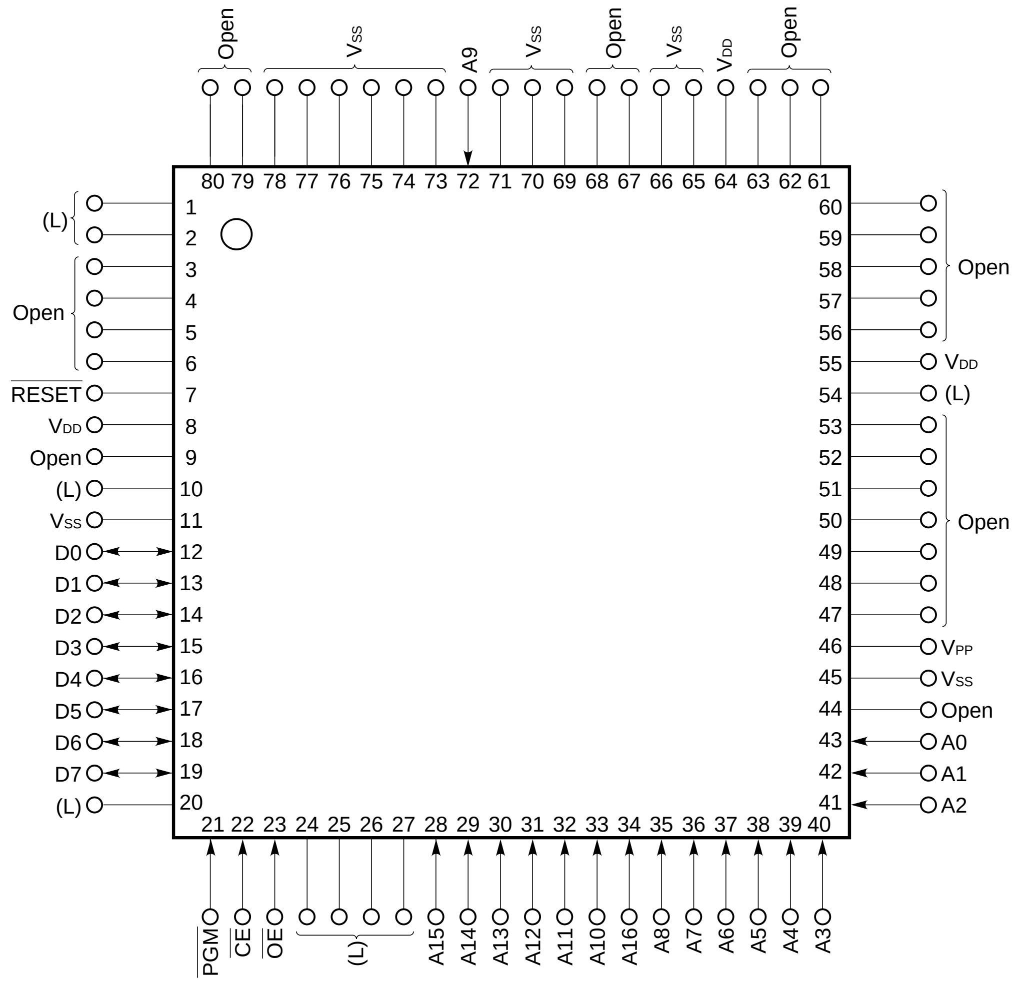
- **80-pin plastic QFP (14 × 14 × 2.7 mm)**

  ★ μPD78P4038GC-3B9, μPD78P4038GC-×××-3B9
- **80-pin plastic QFP (14 × 14 × 1.4 mm)**

  μPD78P4038GC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**

  ★ μPD78P4038GK-BE9, μPD78P4038GK-×××-BE9
- **80-pin ceramic WQFN (14 × 14 mm)**

  μPD78P4038KK-T



Caution L : Connect these pins separately to the V_{SS} pins through 10-kΩ pull-down resistors.

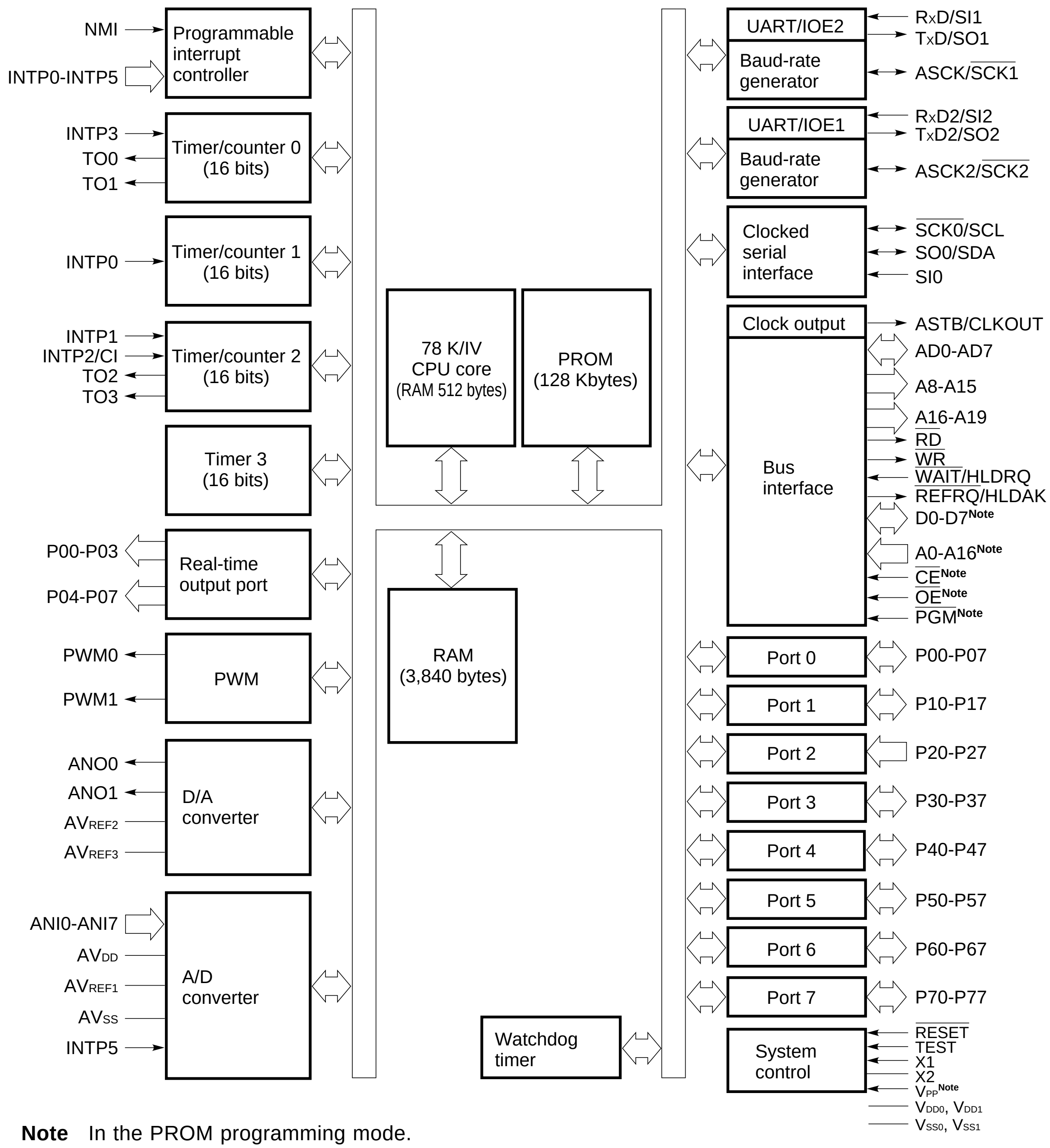
V_{SS} : To be connected to the ground.

Open : Nothing should be connected on these pins.

$\overline{\text{RESET}}$: Set a low-level input.

A0-A16	: Address bus	$\overline{\text{RESET}}$	: Reset
$\overline{\text{CE}}$	: Chip enable	V_{DD}	: Power supply
D0-D7	: Data bus	V_{PP}	: Programming power supply
$\overline{\text{OE}}$	: Output enable	V_{SS}	: Ground
$\overline{\text{PGM}}$	: Program		

3. BLOCK DIAGRAM



Note In the PROM programming mode.

4. LIST OF PIN FUNCTIONS

4.1 Pins for Normal Operating Mode

(1) Port pins (1/2)

Pin	I/O	Alternate-Function	Function
P00-P07	I/O	–	Port 0 (P0): • 8-bit I/O port. • Functions as a real-time output port (4 bits × 2). • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive a transistor.
P10	I/O	PWM0	Port 1 (P1): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive LED.
P11		PWM1	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15-P17		–	
P20	Input	NMI	Port 2 (P2): • 8-bit input-only port. • P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of the pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits). • The P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin functions as the $\overline{\text{SCK1}}$ output pin by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$/SCL	
P33		SO0/SDA	
P34-P37		TO0-TO3	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive LED.

(1) Port pins (2/2)

Pin	I/O	Alternate-Function	Function
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive LED.
P60-P63	I/O	A16-A19	Port 6 (P6): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P64		$\overline{\text{RD}}$	
P65		$\overline{\text{WR}}$	
P66		$\overline{\text{WAIT}}$/HLDRQ	
P67		$\overline{\text{REFRQ}}$/HLDAK	
P70-P77	I/O	ANI0-ANI7	Port 7 (P7): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit.

(2) Non-port pins (1/2)

Pin	I/O	Alternate-Function	Function	
TO0-TO3	Output	P34-P37	Timer output	
CI	Input	P23/INTP2	Input of a count clock for timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SDA	I/O	P33/SO0	Serial data I/O (2-wire serial I/O)	
SI0	Input	P27	Serial data input (3-wire serial I/O0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O2)	
SO0	Output	P33/SDA	Serial data output (3-wire serial I/O0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O2)	
$\overline{\text{SCK0}}$	I/O	P32/SCL	Serial clock I/O (3-wire serial I/O0)	
$\overline{\text{SCK1}}$		P25/INTP4/ASCK	Serial clock I/O (3-wire serial I/O1)	
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock I/O (3-wire serial I/O2)	
SCL		P32/$\overline{\text{SCK0}}$	Serial clock I/O (2-wire serial I/O)	
NMI	Input	P20	External interrupt request	–
INTP0		P21		• Input of a count clock for timer/counter 1 • Capture/trigger signal for CR11 or CR12
INTP1		P22		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR22
INTP2		P23/CI		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR21
INTP3		P24		• Input of a count clock for timer/counter 0 • Capture/trigger signal for CR02
INTP4		P25/ASCK/$\overline{\text{SCK1}}$		–
INTP5		P26		Input of a conversion start trigger for A/D converter
AD0-AD7	I/O	P40-P47	Time multiplexing address/data bus (for connecting external memory)	
A8-A15	Output	P50-P57	High-order address bus (for connecting external memory)	
A16-A19	Output	P60-P63	High-order address bus during address expansion (for connecting external memory)	
$\overline{\text{RD}}$	Output	P64	Strobe signal output for reading the contents of external memory	
$\overline{\text{WR}}$	Output	P65	Strobe signal output for writing on external memory	
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait signal insertion	
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{\text{WAIT}}$	Input of bus hold request	
HLDAK	Output	P67/$\overline{\text{REFRQ}}$	Output of bus hold response	
ASTB	Output	CLKOUT	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	
CLKOUT	Output	ASTB	Clock output	

(2) Non-port pins (2/2)

Pin	I/O	Alternate-Function	Function
$\overline{\text{RESET}}$	Input	–	Chip reset
X1	Input	–	Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.)
X2	–		
ANI0-ANI7	Input	P70-P77	Analog voltage inputs for the A/D converter
ANO0, ANO1	Output	–	Analog voltage inputs for the D/A converter
AV_{REF1}	–	–	Application of A/D converter reference voltage
AV_{REF2}, AV_{REF3}			Application of D/A converter reference voltage
AV_{DD}			Positive power supply for the A/D converter
AV_{SS}			Ground for the A/D converter
V_{DD0} **Note 1**			Positive power supply of the port part
V_{DD1} **Note 1**			Positive power supply except for the port part
V_{SS0} **Note 2**			Ground of the port part
V_{SS1} **Note 2**			Ground except for the port part
TEST			Directly connect to V_{SS0}. (The TEST pin is for the IC test.)

Notes 1. The potential of the V_{DD0} pin must be equal to that of the V_{DD1} pin.

2. The potential of the V_{SS0} pin must be equal to that of the V_{SS1} pin.

4.2 Pins for PROM Programming Mode ($V_{PP} \geq$ +5 V or +12.5 V, $\overline{\text{RESET}}$ = L)

4.2.1 Pin functions

Pin Name	I/O	Function
V_{PP}	–	PROM programming mode selection High voltage input during program write or verification
$\overline{\text{RESET}}$	Input	PROM programming mode selection
A0-A16		Address bus
D0-D7	I/O	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$		Read strobe input to PROM
$\overline{\text{PGM}}$		Program/program inhibit input during PROM programming mode
V_{DD}	–	Positive power supply
V_{SS}	–	GND

4.2.2 Pin functions

(1) V_{PP} (Programming power supply): Input

Input pin for setting the μPD78P4038 to the PROM programming mode. When the input voltage on this pin is +5 V or more and when $\overline{\text{RESET}}$ input goes low, the μPD78P4038 enters the PROM programming mode. When $\overline{\text{CE}}$ is made low for V_{PP} = +12.5 V and $\overline{\text{OE}}$ = high, program data on D0 to D7 can be written into the internal PROM cell selected by A0 to A16.

(2) $\overline{\text{RESET}}$ (Reset): Input

Input pin for setting the μPD78P4038 to the PROM programming mode. When input on this pin is low, and when the input voltage on the V_{PP} pin goes +5 V or more, the μPD78P4038 enters the PROM programming mode.

(3) A0 to A16 (Address bus): Input

Address bus that selects an internal PROM address (0000H to 1FFFFH)

(4) D0 to D7 (Data bus): I/O

Data bus through which a program is written on or read from internal PROM

(5) $\overline{\text{CE}}$ (Chip enable): Input

This pin inputs the enable signal from internal PROM. When this signal is active, a program can be written or read.

(6) $\overline{\text{OE}}$ (Output enable): Input

This pin inputs the read strobe signal to internal PROM. When this signal is made active for $\overline{\text{CE}}$ = low, a one-byte program in the internal PROM cell selected by A0 to A16 can be read onto D0 to D7.

(7) $\overline{\text{PGM}}$ (Program): Input

The input pin for the operation mode control signal of the internal PROM.
Upon activation, writing to the internal PROM is enabled.
Upon inactivation, reading from the internal PROM is enabled.

(8) V_{DD}

Positive power supply pin

(9) V_{SS}

Ground potential pin

4.3 I/O Circuits for Pins and Handling of Unused Pins

Table 4-1 describes the types of I/O circuits for pins and the handling of unused pins.

Figure 4-1 shows the configuration of these various types of I/O circuits.

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

Pin	I/O Circuit Type	I/O	Recommended Connection Method for Unused Pins
P00-P07	5-H	I/O	Input state: To be connected to V_{DD0} Output state: To be left open
P10/PWM0 P11/PWM1			
P12/ASCK2/$\overline{SCK2}$	8-C		
P13/R_xD2/SI2	5-H		
P14/T_xD2/SO2			
P15-P17			
P20/NMI	2	Input	To be connected to V_{DD0} or V_{SS0}
P21/INTP0			
P22/INTP1	2-C		To be connected to V_{DD0}
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-C	I/O	Input state: To be connected to V_{DD0} Output state: To be left open
P26/INTP5	2-C	Input	To be connected to V_{DD0}
P27/SI0			
P30/R_xD/SI1	5-H	I/O	Input state: To be connected to V_{DD0} Output state: To be left open
P31/T_xD/SO1			
P32/$\overline{SCK0}$/SCL	10-B		
P33/SO0/SDA			
P34/TO0-P37/TO3	5-H		
P40/AD0-P47/AD7			
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0-P77/ANI7	20-A	I/O	Input state: To be connected to V_{DD0} or V_{SS0} Output state: To be left open
ANO0, ANO1	12	Output	To be left open
ASTB/CLKOUT	4-B		

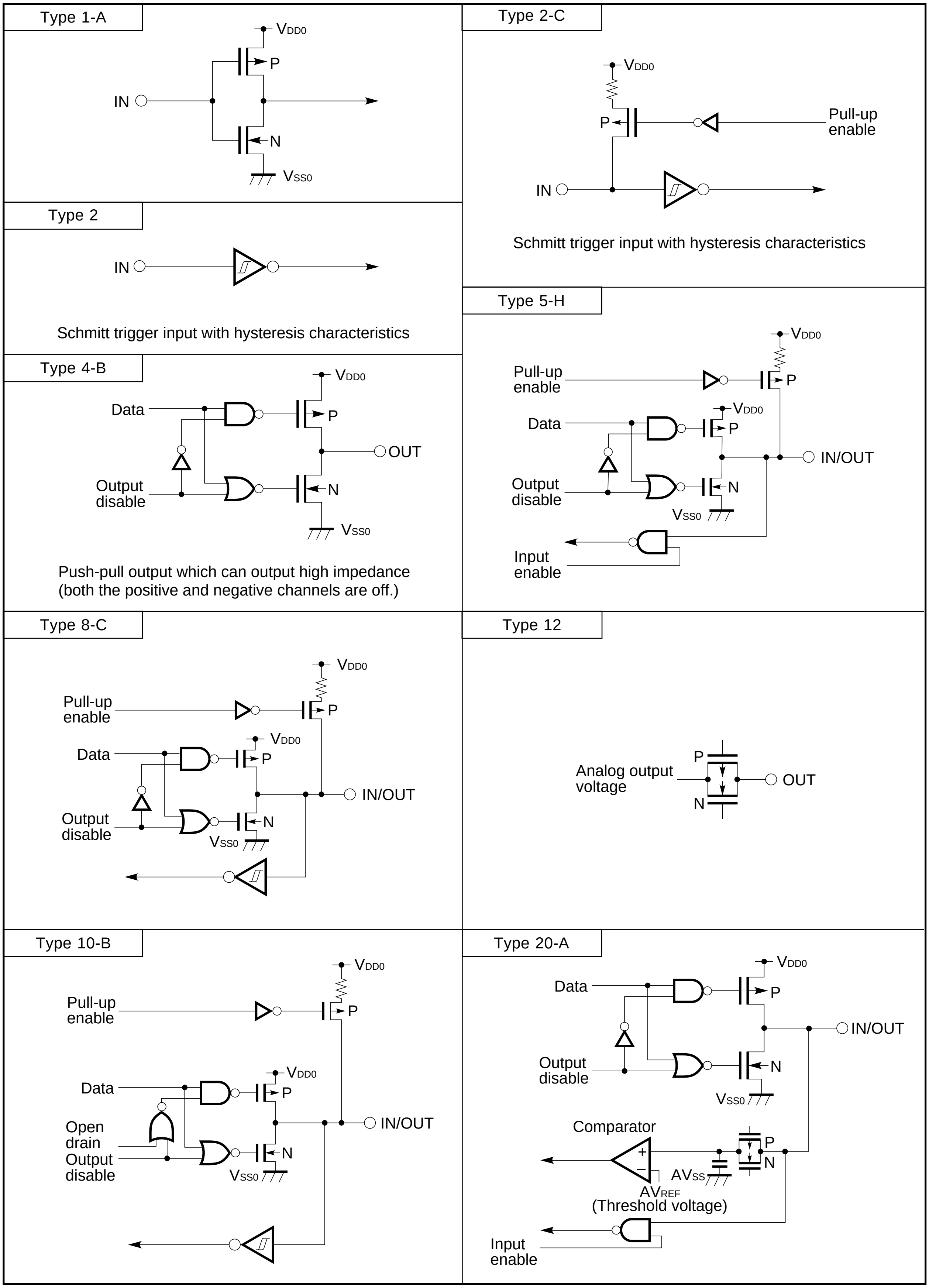
Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

Pin	I/O Circuit Type	I/O	Recommended Connection Method for Unused Pins
$\overline{\text{RESET}}$	2	Input	–
TEST	1-A		To be connected to V_{SS0} directly
AV_{REF1}-AV_{REF3}	–		To be connected to V_{SS0}
AV_{SS}			
AV_{DD}			To be connected to V_{DD0}

Caution When the I/O mode of an I/O alternate-function pin is unpredictable, connect the pin to V_{DD0} through a resistor of 10 to 100 kilohms (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

Remark Since type numbers are consistent in the 78K Series, those numbers are not always serial in each product. (Some circuits are not included.)

Figure 4-1. I/O Circuits for Pins



5. INTERNAL MEMORY SWITCHING REGISTER (IMS)

This register enables the software to avoid using part of the internal memory. IMS can be set to establish the same memory mapping as used in ROM products that have different internal memory (ROM and RAM) configurations.

IMS is set with 8-bit memory operation instructions.

$\overline{\text{RESET}}$ input sets IMS to FFH.

Figure 5-1. Internal Memory Switching Register (IMS)

	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	IMS7	IMS6	IMS5	IMS4	IMS3	IMS2	IMS1	IMS0	0FFFCH	FFH	W

IMS0-7	Memory Size
FFH	Same as the μPD784038
EEH	Same as the μPD784037
DCH	Same as the μPD784036
CCH	Same as the μPD784035

IMS is not contained in a mask ROM product (μPD784035, μPD784036, μPD784037, or μPD784038). But the action is not affected if the write command to IMS is executed to the mask ROM product.

6. PROM PROGRAMMING

The μPD78P4038 has an on-chip 128-KB PROM device for use as program memory. When programming, set the V_{PP} and $\overline{\text{RESET}}$ pins for PROM programming mode. See **(2)** in **Chapter 2** with regard to handling of other, unused pins.

6.1 Operation Mode

PROM programming mode is selected when +5 V or +12.5 V is added to the V_{PP} pin or low-level input is added to the $\overline{\text{RESET}}$ pin. This mode can be set to operation mode by setting the $\overline{\text{CE}}$ pin, $\overline{\text{OE}}$ pin, and $\overline{\text{PGM}}$ pin as shown in Table 6-1 below.

In addition, the PROM contents can be read by setting read mode.

Table 6-1. PROM Programming Operation Mode

Operation Mode \ Pin	$\overline{\text{RESET}}$	V_{PP}	V_{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

Remark × = L or H

(1) Read mode

Set $\overline{CE}$ to L and $\overline{OE}$ to L to set read mode.

(2) Output disable mode

Set $\overline{OE}$ to H to set high impedance for data output and output disable mode.
Consequently, if several μPD78P4038 devices are connected to a data bus, the $\overline{OE}$ pins can be controlled to select data output from any of the devices.

(3) Standby mode

Set $\overline{CE}$ to H to set standby mode.
In this mode, data output is set to high impedance regardless of the $\overline{OE}$ setting.

(4) Page data latch mode

At the beginning of page write mode, set $\overline{CE}$ to H, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set page data latch mode.
In this mode, 1 page (4 bytes) of data are latched to the internal address/data latch circuit.

(5) Page write mode

After latching the address and data for one page (4 bytes) using page data latch mode, adding a 0.1-ms program pulse (active, low) to the $\overline{PGM}$ pin with both $\overline{CE}$ and $\overline{OE}$ set to H causes page write to be executed. Later, setting both $\overline{CE}$ and $\overline{OE}$ to L causes program verification to be executed.
If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where $X \leq 10$).

(6) Byte write mode

Adding a 0.1-ms program pulse (active, low) to the $\overline{PGM}$ pin with both $\overline{CE}$ and $\overline{OE}$ set to H causes byte write to be executed. Later, setting $\overline{OE}$ to L causes program verification to be executed.
If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where $X \leq 10$).

(7) Program verify mode

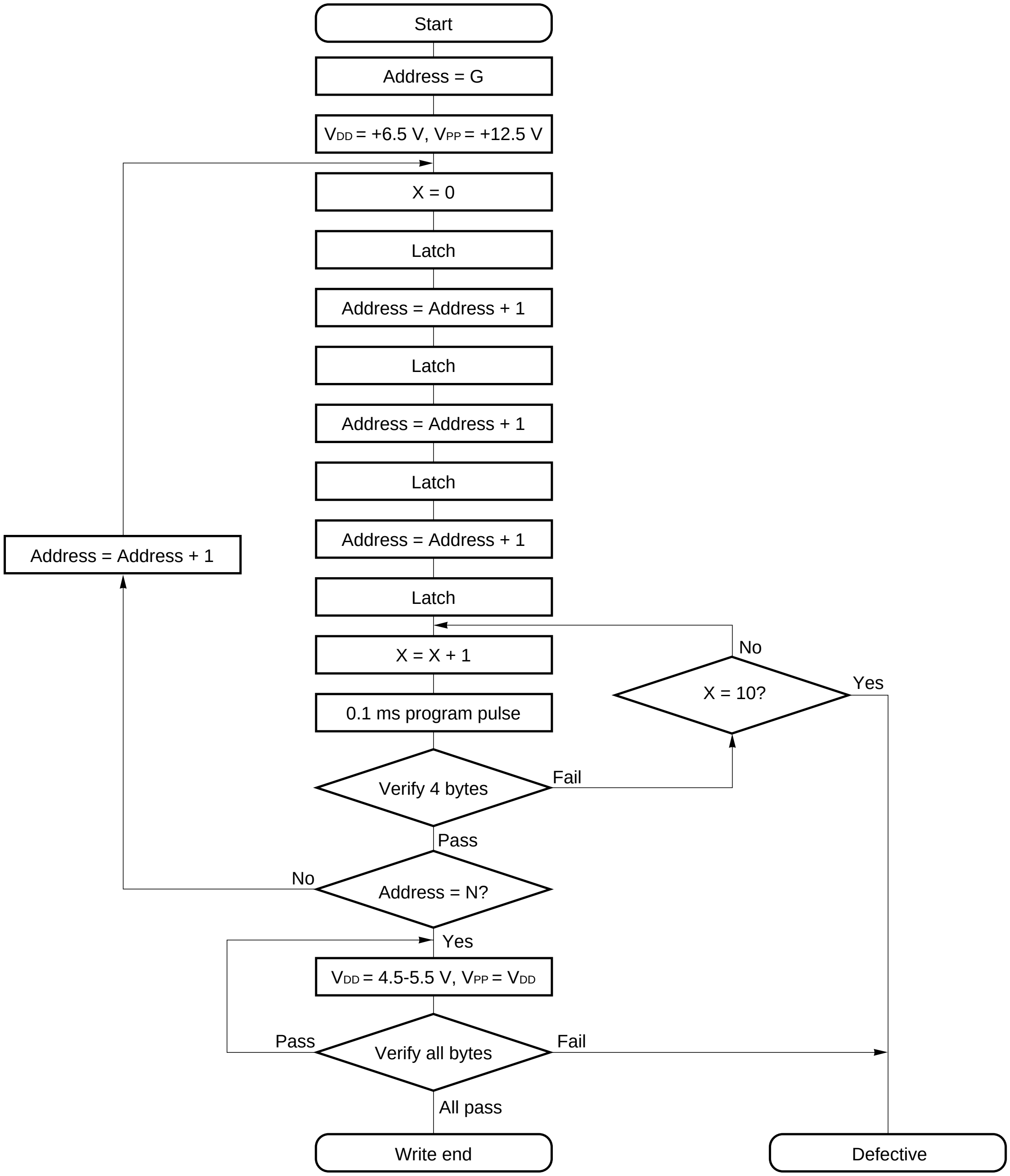
Set $\overline{CE}$ to L, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set program verify mode. Use verify mode for verification following each write operation.

(8) Program inhibit mode

Program inhibit mode is used to write to a single device when several μPD78P4038 devices are connected in parallel to $\overline{OE}$, V_{PP}, and D0 to D7 pins.
Use the page write mode or byte write mode described above for each write operation. Write operations cannot be done for devices in which the $\overline{PGM}$ pin has been set to H.

6.2 PROM Write Sequence

Figure 6-1. Page Program Mode Flowchart



Remark G = Start address
N = Program end address

Figure 6-2. Page Program Mode Timing

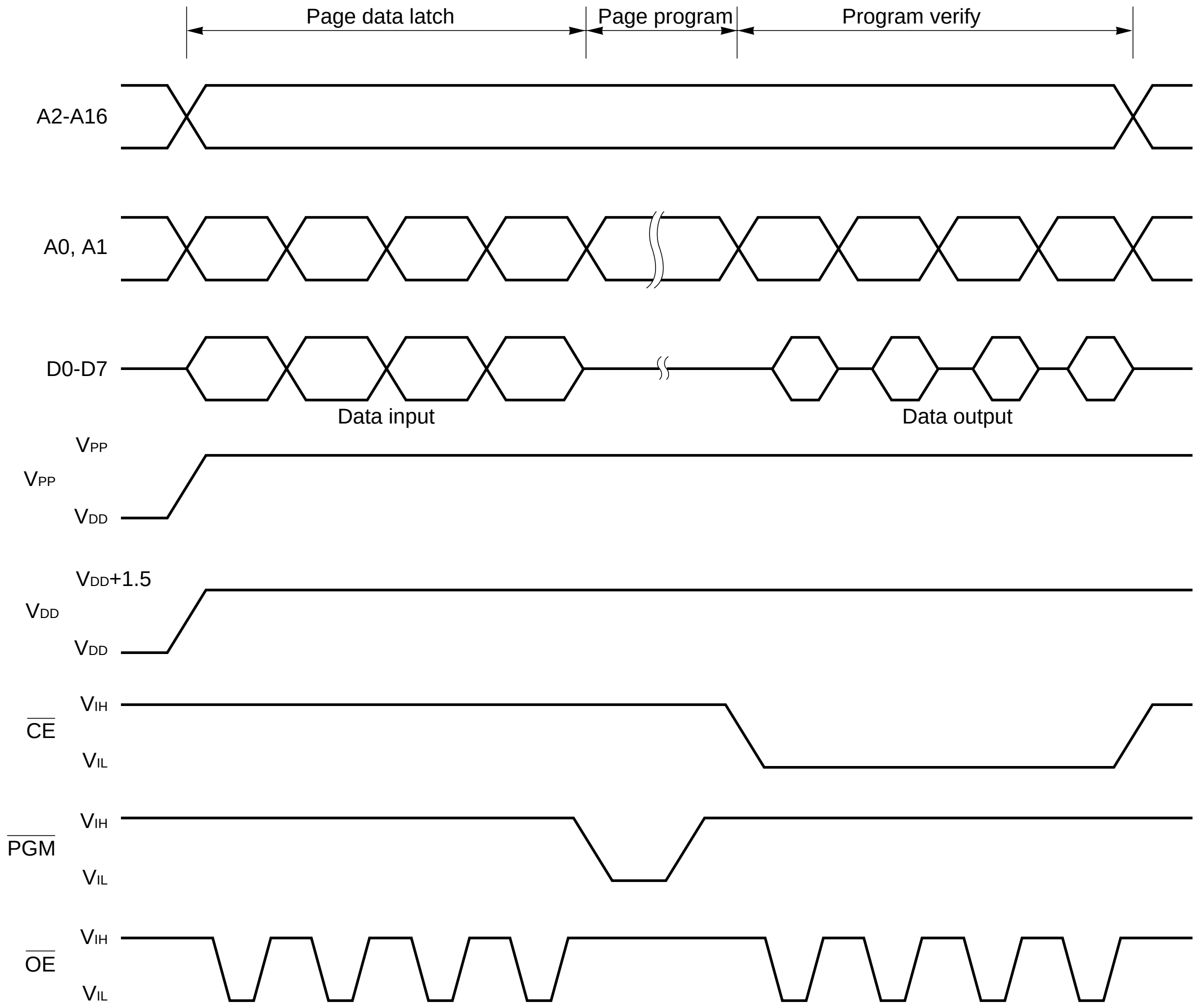
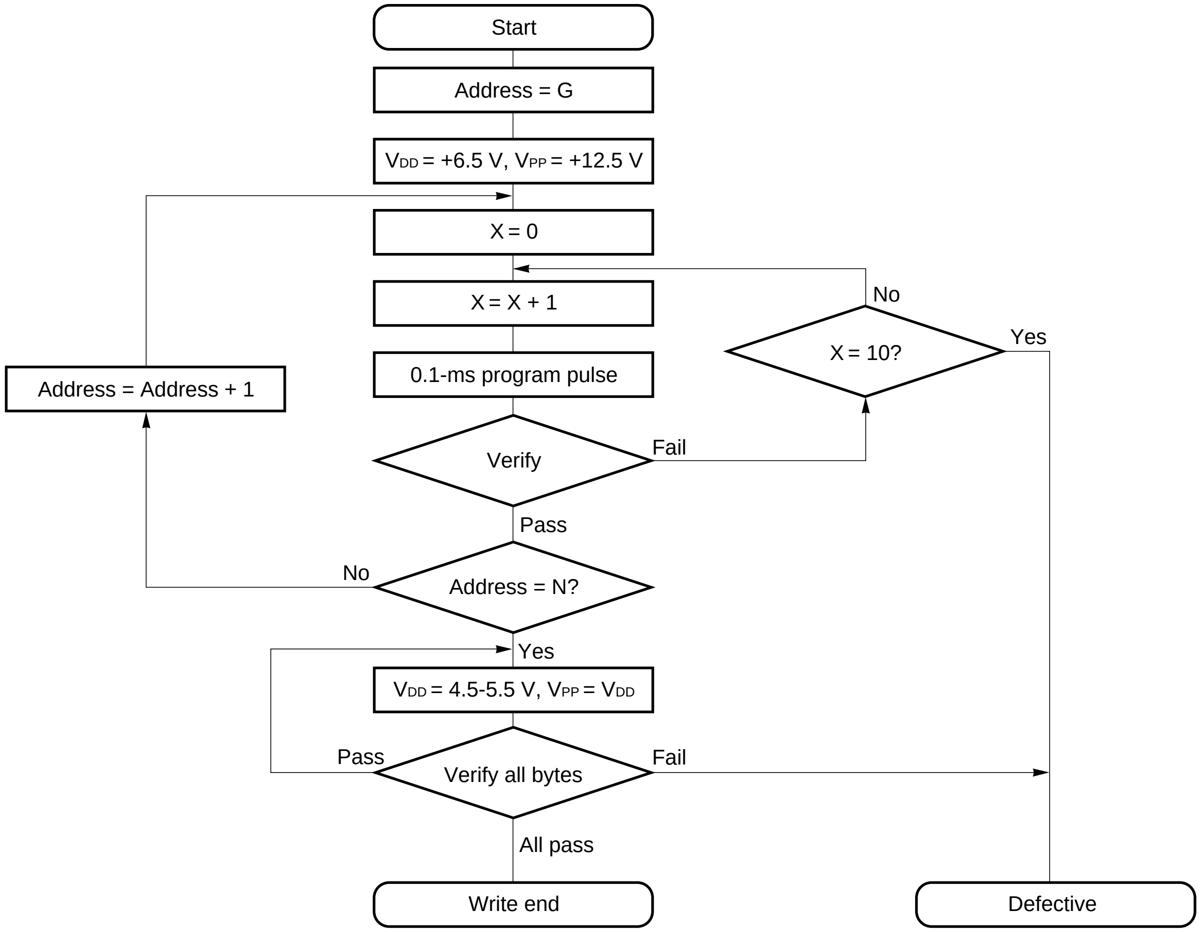
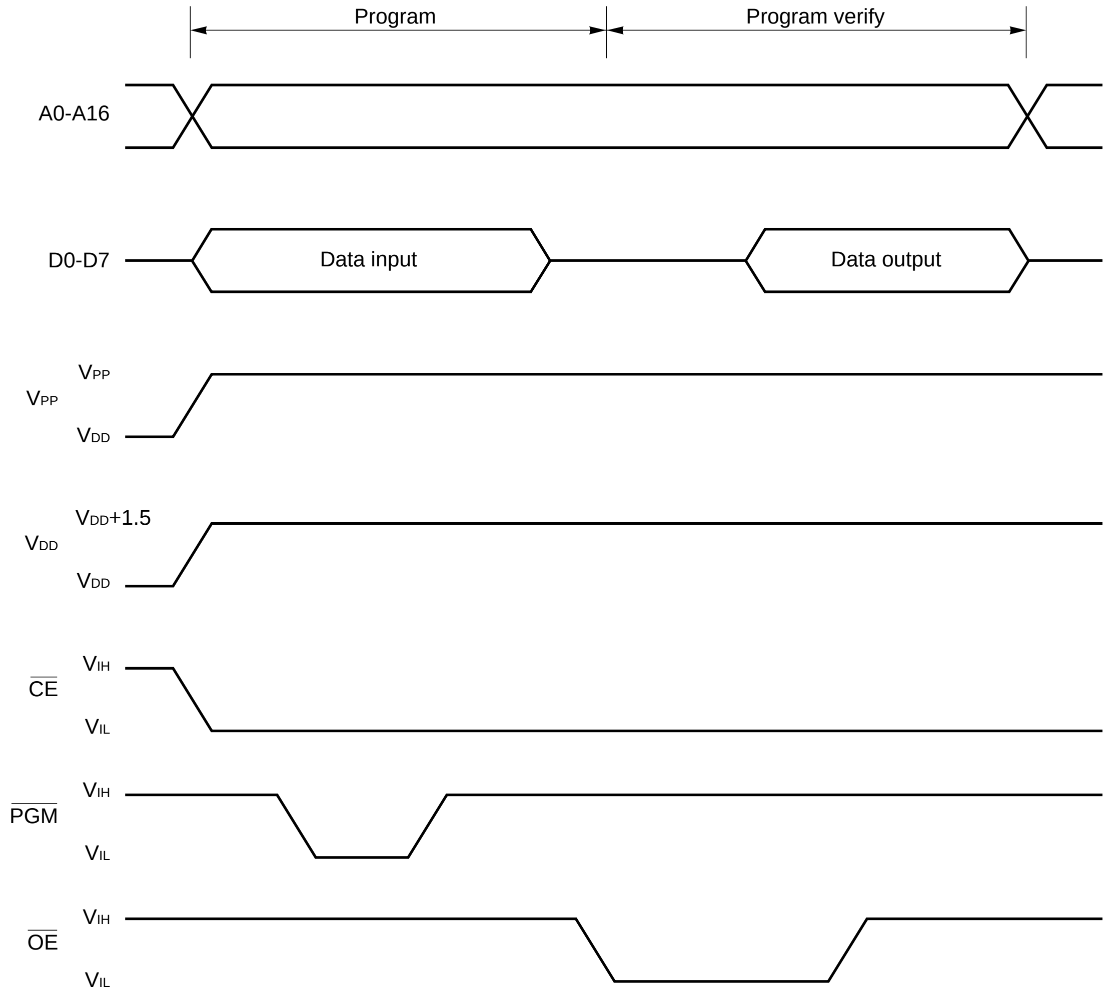


Figure 6-3. Byte Program Mode Flowchart



Remark G = Start address
N = Program end address

Figure 6-4. Byte Program Mode Timing



Cautions 1. Add V_{DD} before V_{PP}, and turn off the V_{DD} after V_{PP}.

2. Do not allow V_{PP} to exceed +13.5 V including overshoot.

3. Reliability problems may result if the device is inserted or pulled out while +12.5 V is applied at V_{PP}.

6.3 PROM Read Sequence

Follow this sequence to read the PROM contents to an external data bus (D0 to D7).

(1) Set the $\overline{\text{RESET}}$ pin to low level and add +5 V to the V_{PP} pin. See **(2)** in **Chapter 2** with regard to handling of other, unused pins.

(2) Add +5 V to the V_{DD} and V_{PP} pins.

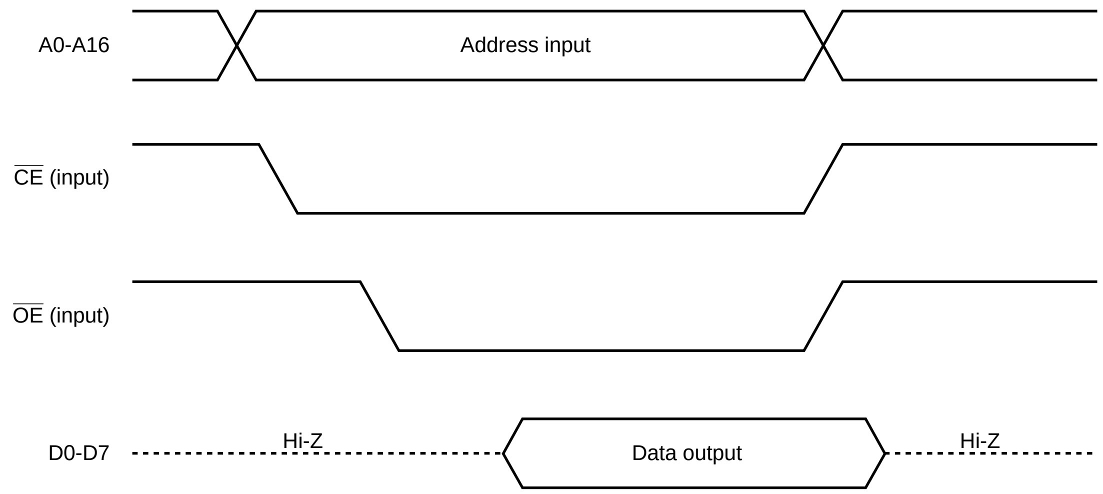
(3) Input the data address to be read to pins A0 to A16.

(4) Set read mode.

(5) Output the data to pins D0 to D7.

Figure 6-5 shows the timing of steps (2) to (5) above.

Figure 6-5. PROM Read Timing



7. ERASURE CHARACTERISTICS (μPD78P4038KK-T ONLY)

Data written in the μPD78P4038KK-T program memory can be erased (FFH); therefore users can write other data in the memory.

To erase the written data, expose the erasure window to light with a wavelength shorter than approx. 400 nm. Normally, ultraviolet light with a wavelength of 254 nm is employed. The amount of light required to completely erase the data is as follows:

- Intensity of ultraviolet light × erasing time: 57.6 W•s/cm^2 min.
- Erasing time: About 80 minutes (When using a 12,000 μW/cm^2 ultraviolet lamp. It may, however, take more time due to lamp deterioration, dirt on the erasure window, or the like.)

The ultraviolet lamp should be placed within 2.5 cm from the erasure window during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

8. PROTECTIVE FILM COVERING THE ERASURE WINDOW (μPD78P4038KK-T ONLY)

To prevent EPROM from being erased inadvertently by light other than that from the lamp used for erasing EPROM, or to prevent the internal circuits other than EPROM from malfunctioning by light, stick a protective film on the erasure window except when EPROM is to be erased.

9. QUALITY

The μPD78P4038KK-T is not intended for use in mass-produced products; they do not have reliability high enough for such purposes. Their use should be restricted to functional evaluation in experiment or trial manufacture.

10. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μPD78P4038GC-3B9, μPD78P4038GC-8BT, and μPD78P4038GK-BE9) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125°C for 24 hours.

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

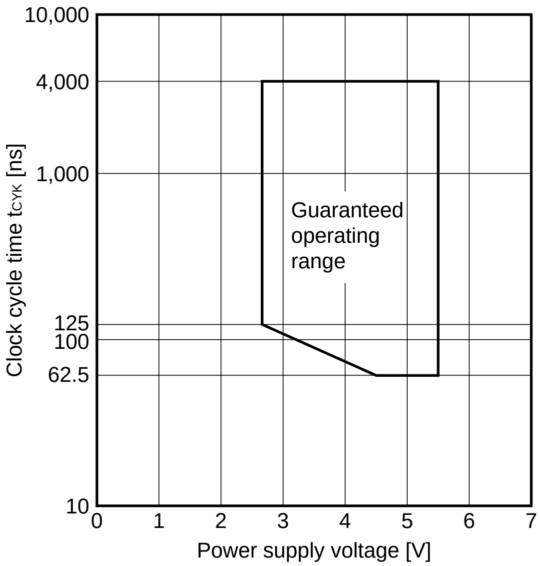
Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_{I1}		–0.5 to V_{DD} + 0.5	V
	V_{I2}	TEST/V_{PP} pin and P21/INTP0/A9 pin in PROM programming mode	–0.5 to +13.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Output low current	I_{OL}	At one pin	15	mA
		Total of all output pins	100	mA
Output high current	I_{OH}	At one pin	–10	mA
		Total of all output pins	–100	mA
A/D converter reference input voltage	AV_{REF1}		–0.5 to V_{DD} + 0.3	V
D/A converter reference input voltage	AV_{REF2}		–0.5 to V_{DD} + 0.3	V
	AV_{REF3}		–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

OPERATING CONDITIONS

- Operating ambient temperature (T_A) : –40 to +85°C
- Rise time and fall time (t_r, t_f) (at pins which are not specified) : 0 to 200 μs
- Power supply voltage and clock cycle time : See **Figure 11-1.**

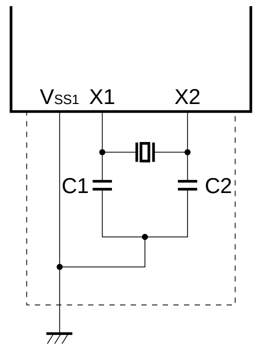
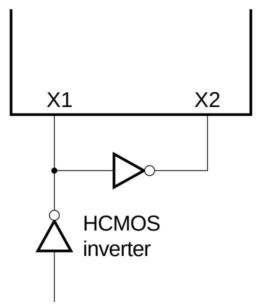
Figure 11-1. Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V on pins other than measured pins			10	pF
Output capacitance	C_O				10	pF
I/O capacitance	C_{IO}				10	pF

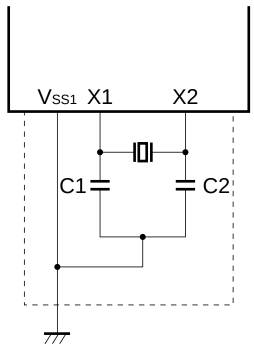
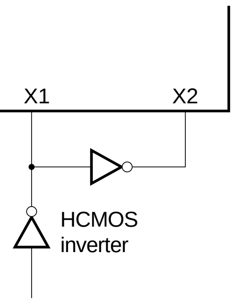
OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = +4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal		Oscillator frequency (f_{XX})	4	32	MHz
External clock		X1 input frequency (f_X)	4	32	MHz
		X1 input rise and fall times (t_{XR}, t_{XF})	0	10	ns
		X1 input high-level and low-level widths (t_{WXH}, t_{WXL})	10	125	ns

Caution When using the system clock generator, run wires in the portion surrounded by broken lines according to the following rules to avoid effects such as stray capacitance:

- **Minimize the wiring.**
- **Never cause the wires to cross other signal lines.**
- **Never cause the wires to run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS1}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = +2.7 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal		Oscillator frequency (f_{XX})	4	16	MHz
External clock		X1 input frequency (f_X)	4	16	MHz
		X1 input rise and fall times (t_{XR}, t_{XF})	0	10	ns
		X1 input high-level and low-level widths (t_{WXH}, t_{WXL})	10	125	ns

Caution When using the system clock generator, run wires in the portion surrounded by broken lines according to the following rules to avoid effects such as stray capacitance:

- **Minimize the wiring.**
- **Never cause the wires to cross other signal lines.**
- **Never cause the wires to run near a line carrying a large varying current.**
- **Cause the grounding point of the capacitor of the oscillator circuit to have the same potential as V_{SS1}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL1}	For pins other than those described in Notes 1, 2, 3, and 4	–0.3		$0.3V_{DD}$	V
	V_{IL2}	For pins described in Notes 1, 2, 3, and 4	–0.3		$0.2V_{DD}$	V
	V_{IL3}	V_{DD} = +5.0 V ± 10% For pins described in Notes 2, 3, and 4	–0.3		+0.8	V
Input high voltage	V_{IH1}	For pins other than those described in Note 1	$0.7V_{DD}$		V_{DD} + 0.3	V
	V_{IH2}	For pins described in Note 1	$0.8V_{DD}$		V_{DD} + 0.3	V
	V_{IH3}	V_{DD} = +5.0 V ± 10% For pins described in Notes 2, 3, and 4	2.2		V_{DD} + 0.3	V
Output low voltage	V_{OL1}	I_{OL} = 2 mA			0.4	V
	V_{OL2}	V_{DD} = +5.0 V ± 10% I_{OL} = 8 mA For pins described in Notes 2 and 5			1.0	V
Output high voltage	V_{OH1}	I_{OH} = –2 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = +5.0 V ± 10% I_{OH} = –5 mA For pins described in Note 4	V_{DD} – 1.4			V
X1 input low current	I_{IL}	EXTC = 0 0 V ≤ V_I ≤ V_{IL2}			–30	μA
X1 input high current	I_{IH}	EXTC = 0 V_{IH2} ≤ V_I ≤ V_{DD}			+30	μA

Notes 1. X1, X2, $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$/SCL, P33/SO0/SDA, TEST

2. P40/AD0 to P47/AD7, P50/A8 to P57/A15

3. P60/A16 to P63/A19, P64/$\overline{\text{RD}}$, P65/$\overline{\text{WR}}$, P66/$\overline{\text{WAIT}}$/HLDRQ, P67/$\overline{\text{REFRQ}}$/HLDAK

4. P00 to P07

5. P10 to P17

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	$0 V \le V_I \le V_{DD}$ For pins other than X1 when EXTC = 0				±10	μA
Output leakage current	I_{LO}	$0 V \le V_O \le V_{DD}$				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode	f_{XX} = 32 MHz V_{DD} = +5.0 V ± 10%		25	45	mA
			f_{XX} = 16 MHz V_{DD} = +2.7 to 3.3 V		12	25	mA
	I_{DD2}	HALT mode	f_{XX} = 32 MHz V_{DD} = +5.0 V ± 10%		13	26	mA
			f_{XX} = 16 MHz V_{DD} = +2.7 to 3.3 V		8	12	mA
	I_{DD3}	IDLE mode (EXTC = 0)	f_{XX} = 32 MHz V_{DD} = +5.0 V ± 10%			12	mA
			f_{XX} = 16 MHz V_{DD} = +2.7 to 3.3 V			8	mA
Pull-up resistor	R_L	V_I = 0 V		15		80	kΩ

AC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address setup time	t_{SAST}	V_{DD} = +5.0 V ± 10%	(0.5 + a) T – 15		ns
			(0.5 + a) T – 31		ns
ASTB high-level width	t_{WSTH}	V_{DD} = +5.0 V ± 10%	(0.5 + a) T – 17		ns
			(0.5 + a) T – 40		ns
Address hold time (to ASTB↓)	t_{HSTLA}	V_{DD} = +5.0 V ± 10%	0.5T – 24		ns
			0.5T – 34		ns
Address hold time (to $\overline{RD}$↑)	t_{HRA}		0.5T – 14		ns
Delay from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = +5.0 V ± 10%	(1 + a) T – 9		ns
			(1 + a) T – 15		ns
Address float time (to $\overline{RD}$↓)	t_{FRA}			0	ns
Delay from address to data input	t_{DAID}	V_{DD} = +5.0 V ± 10%		(2.5 + a + n) T – 37	ns
				(2.5 + a + n) T – 52	ns
Delay from ASTB↓ to data input	t_{DSTID}	V_{DD} = +5.0 V ± 10%		(2 + n) T – 40	ns
				(2 + n) T – 60	ns
Delay from $\overline{RD}$↓ to data input	t_{DRID}	V_{DD} = +5.0 V ± 10%		(1.5 + n) T – 50	ns
				(1.5 + n) T – 70	ns
Delay from ASTB↓ to $\overline{RD}$↓	t_{DSTR}		0.5T – 9		ns
Data hold time (to $\overline{RD}$↑)	t_{HRID}		0		ns
Delay from $\overline{RD}$↑ to address active	t_{DRA}	After program is read, V_{DD} = +5.0 V ± 10%	0.5T – 8		ns
		After program is read	0.5T – 12		ns
		After data is read, V_{DD} = +5.0 V ± 10%	1.5T – 8		ns
		After data is read	1.5T – 12		ns
Delay from $\overline{RD}$↑ to ASTB↑	t_{DRST}		0.5T – 17		ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = +5.0 V ± 10%	(1.5 + n) T – 30		ns
			(1.5 + n) T – 40		ns
Address hold time (to $\overline{WR}$↑)	t_{HWA}		0.5T – 14		ns
Delay from address to $\overline{WR}$↓	t_{DAW}	V_{DD} = +5.0 V ± 10%	(1 + a) T – 5		ns
			(1 + a) T – 15		ns
Delay from ASTB↓ to data output	t_{DSTOD}	V_{DD} = +5.0 V ± 10%		0.5T + 19	ns
				0.5T + 35	ns
Delay from $\overline{WR}$↓ to data output	t_{DWOD}			0.5T – 11	ns
Delay from ASTB↓ to $\overline{WR}$↓	t_{DSTW}		0.5T – 9		ns

Remarks T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (to $\overline{WR}$↑)	t_{SODW}	V_{DD} = +5.0 V ± 10%	(1.5 + n) T – 30		ns
			(1.5 + n) T – 40		ns
Data hold time (to $\overline{WR}$↑)**Note**	t_{HWOD}	V_{DD} = +5.0 V ± 10%	0.5T – 5		ns
			0.5T – 25		ns
Delay from $\overline{WR}$↑ to ASTB↑	t_{DWST}		0.5T – 12		ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = +5.0 V ± 10%	(1.5 + n) T – 30		ns
			(1.5 + n) T – 40		ns

Note The hold time includes the time during which V_{OH1} and V_{OL1} are held under the load conditions of C_L = 50 pF and R_L = 4.7 kΩ.

Remarks T: T_{CYK} (system clock cycle time)
n: Number of wait states (n ≥ 0)

(2) Bus hold timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay from HLDRQ↑ to float	t_{FHQC}			(6 + a + n) T + 50	ns
Delay from HLDRQ↑ to HLDAK↑	$t_{DHQHHAH}$	V_{DD} = +5.0 V ± 10%		(7 + a + n) T + 30	ns
				(7 + a + n) T + 40	ns
Delay from float to HLDAK↑	t_{DCFHA}			1T + 30	ns
Delay from HLDRQ↓ to HLDAK↓	$t_{DHQLHAL}$	V_{DD} = +5.0 V ± 10%		2T + 40	ns
				2T + 60	ns
Delay from HLDAK↓ to active	t_{DHAC}	V_{DD} = +5.0 V ± 10%	1T – 20		ns
			1T – 30		ns

Remarks T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

(3) External wait timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay from address to $\overline{\text{WAIT}}$↓ input	t_{DAWT}	V_{DD} = +5.0 V ± 10%		(2 + a) T – 40	ns
				(2 + a) T – 60	ns
Delay from ASTB↓ to $\overline{\text{WAIT}}$↓ input	t_{DSTWT}	V_{DD} = +5.0 V ± 10%		1.5T – 40	ns
				1.5T – 60	ns
Hold time from ASTB↓ to $\overline{\text{WAIT}}$	t_{HSTWTH}	V_{DD} = +5.0 V ± 10%	(0.5 + n) T + 5		ns
			(0.5 + n) T +10		ns
Delay from ASTB↓ to $\overline{\text{WAIT}}$↑	t_{DSTWTH}	V_{DD} = +5.0 V ± 10%		(1.5 + n) T – 40	ns
				(1.5 + n) T – 60	ns
Delay from $\overline{\text{RD}}$↓ to $\overline{\text{WAIT}}$↓ input	t_{DRWTL}	V_{DD} = +5.0 V ± 10%		T – 50	ns
				T – 70	ns
Hold time from $\overline{\text{RD}}$↓ to $\overline{\text{WAIT}}$↓	t_{HRWT}	V_{DD} = +5.0 V ± 10%	nT + 5		ns
			nT + 10		ns
Delay from $\overline{\text{RD}}$↓ to $\overline{\text{WAIT}}$↑	t_{DRWTH}	V_{DD} = +5.0 V ± 10%		(1 + n) T – 40	ns
				(1 + n) T – 60	ns
Delay from $\overline{\text{WAIT}}$↑ to data input	t_{DWTID}	V_{DD} = +5.0 V ± 10%		0.5T – 5	ns
				0.5T – 10	ns
Delay from $\overline{\text{WAIT}}$↑ to $\overline{\text{WR}}$↑	t_{DWTW}		0.5T		ns
Delay from $\overline{\text{WAIT}}$↑ to $\overline{\text{RD}}$↑	t_{DWTR}		0.5T		ns
Delay from $\overline{\text{WR}}$↓ to $\overline{\text{WAIT}}$↓ input	t_{DWWTL}	V_{DD} = +5.0 V ± 10%		T – 50	ns
				T – 75	ns
Hold time from $\overline{\text{WR}}$↓ to $\overline{\text{WAIT}}$	t_{HWWT}	V_{DD} = +5.0 V ± 10%	nT + 5		ns
			nT + 10		ns
Delay from $\overline{\text{WR}}$↓ to $\overline{\text{WAIT}}$↑	t_{DWWTH}	V_{DD} = +5.0 V ± 10%		(1 + n) T – 40	ns
				(1 + n) T – 70	ns

Remarks T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

(4) Refresh timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Random read/write cycle time	t_{RC}		3T		ns
$\overline{\text{REFRQ}}$ low-level pulse width	t_{WRFQL}	V_{DD} = +5.0 V ± 10%	1.5T – 25		ns
			1.5T – 30		ns
Delay from ASTB↓ to $\overline{\text{REFRQ}}$	t_{DSTRFQ}		0.5T – 9		ns
Delay from $\overline{\text{RD}}$↑ to $\overline{\text{REFRQ}}$	t_{DRRFQ}		1.5T – 9		ns
Delay from $\overline{\text{WR}}$↑ to $\overline{\text{REFRQ}}$	t_{DWRFQ}		1.5T – 9		ns
Delay from $\overline{\text{REFRQ}}$↑ to ASTB	t_{DRFQST}		0.5T – 15		ns
$\overline{\text{REFRQ}}$ high-level pulse width	t_{WRFQH}	V_{DD} = +5.0 V ± 10%	1.5T – 25		ns
			1.5T – 30		ns

Remark T: T_{CYK} (system clock cycle time)

SERIAL OPERATION (T_A = –40 to +85°C, V_{DD} = +2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

(1) CSI

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK0}$)	t_{CYSK0}	Input	External clock When $\overline{SCK0}$ and SO0 are CMOS I/O	$10/f_{XX}$ + 380		ns
		Output		T		μs
Serial clock low-level width ($\overline{SCK0}$)	t_{WSKL0}	Input	External clock When $\overline{SCK0}$ and SO0 are CMOS I/O	$5/f_{XX}$ + 150		ns
		Output		0.5T – 40		μs
Serial clock high-level width ($\overline{SCK0}$)	t_{WSKH0}	Input	External clock When $\overline{SCK0}$ and SO0 are CMOS I/O	$5/f_{XX}$ + 150		ns
		Output		0.5T – 40		μs
SI0 setup time (to $\overline{SCK0}$↑)	t_{SSSK0}			40		ns
SI0 hold time (to $\overline{SCK0}$↑)	t_{HSSK0}			$5/f_{XX}$ + 40		ns
SO0 output delay time (to $\overline{SCK0}$↓)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	$5/f_{XX}$ + 150	ns
	t_{DSBSK2}	Open-drain output (2-wire serial I/O mode), R_L = 1 kΩ		0	$5/f_{XX}$ + 400	ns

Remarks 1. The values in this table are those when C_L is 100 pF.

2. T : Serial clock cycle set by software. The minimum value is $16/f_{XX}$.

3. f_{XX} : Oscillator frequency

(2) IOE1, IOE2

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	Input	V_{DD} = +5.0 V ± 10%	250		ns
				500		ns
		Output	Internal, divided by 16	T		ns
Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}	Input	V_{DD} = +5.0 V ± 10%	85		ns
				210		ns
		Output	Internal, divided by 16	0.5T – 40		ns
Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}	Input	V_{DD} = +5.0 V ± 10%	85		ns
				210		ns
		Output	Internal, divided by 16	0.5T – 40		ns
Setup time for SI1 and SI2 (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}			40		ns
Hold time for SI1 and SI2 (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}			40		ns
Output delay time for SO1 and SO2 (to $\overline{SCK1}$, $\overline{SCK2}$↓)	t_{DSOSK}			0	50	ns
Output hold time for SO1 and SO2 (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK}	When data is transferred		$0.5t_{CYSK1}$ – 40		ns

Remarks 1. The values in this table are those when C_L is 100 pF.

2. T: Serial clock cycle set by software. The minimum value is $16/f_{XX}$.

(3) UART, UART2

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASCK clock input cycle time	t_{CYASK}	V_{DD} = +5.0 V ± 10%	125		ns
			250		ns
ASCK clock low-level width	t_{WASKL}	V_{DD} = +5.0 V ± 10%	52.5		ns
			85		ns
ASCK clock high-level width	t_{WASKH}	V_{DD} = +5.0 V ± 10%	52.5		ns
			85		ns

CLOCK OUTPUT OPERATION

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLKOUT cycle time	t_{CYCL}		nT		ns
CLKOUT low-level width	t_{CLL}	V_{DD} = +5.0 V ± 10%	$0.5t_{CYCL} - 10$		ns
			$0.5t_{CYCL} - 20$		ns
CLKOUT high-level width	t_{CLH}	V_{DD} = +5.0 V ± 10%	$0.5t_{CYCL} - 10$		ns
			$0.5t_{CYCL} - 20$		ns
CLKOUT rise time	t_{CLR}	V_{DD} = +5.0 V ± 10%		10	ns
				20	ns
CLKOUT fall time	t_{CLF}	V_{DD} = +5.0 V ± 10%		10	ns
				20	ns

Remarks n: Divided frequency ratio set by software in the CPU (n = 1, 2, 4, 8, 16)
T: T_{CYK} (system clock cycle time)

OTHER OPERATIONS

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
★ INTP0 low-level width	t_{WIT0L}		$4t_{CYSMP}$		ns
★ INTP0 high-level width	t_{WIT0H}		$4t_{CYSMP}$		ns
★ Low-level width for INTP1-INTP3 and CI	t_{WIT1L}		$4t_{CYCPU}$		ns
★ High-level width for INTP1-INTP3 and CI	t_{WIT1H}		$4t_{CYCPU}$		ns
Low-level width for INTP4 and INTP5	t_{WIT2L}		10		μs
High-level width for INTP4 and INTP5	t_{WIT2H}		10		μs
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

Remarks t_{CYSMP}: Sampling clock set by software
t_{CYCPU}: CPU operation clock set by software in the CPU

A/D CONVERTER CHARACTERISTICS

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Total error[Note]		V_{DD} = AV_{DD} = +5.0 V ± 10%			1.0	%
		V_{DD} = AV_{DD} = +2.7 to 4.5 V T_A = –10 to +85°C			1.0	%
Linearity calibration[Note]					0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	FR = 1	120			t_{CYK}
		FR = 0	180			t_{CYK}
Sampling time	t_{SAMP}	FR = 1	24			t_{CYK}
		FR = 0	36			t_{CYK}
Analog input voltage	V_{IAN}		–0.3		AV_{REF1} + 0.3	V
Analog input impedance	R_{AN}			1,000		MΩ
AV_{REF1} current	AI_{REF1}			0.5	1.5	mA
AV_{DD} supply current	AI_{DD1}	f_{XX} = 32 MHz, CS = 1		2.0	5.0	mA
	AI_{DD2}	STOP mode, CS = 0		1.0	20	μA

Note Quantization error is not included. This parameter is indicated as the ratio to the full-scale value.

Remark t_{CYK}: System clock cycle time

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

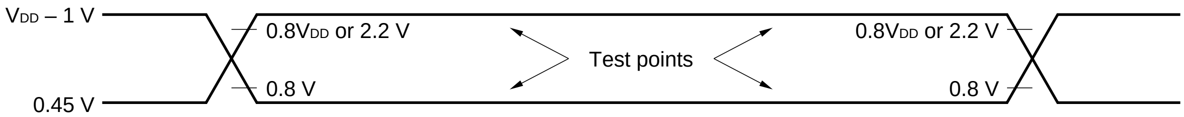
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8			bit
Total error		Load conditions: 4 MΩ, 30 pF	V_{DD} = AV_{DD} = AV_{REF2} = +2.7 to 5.5 V AV_{REF3} = 0 V			0.6	%
			V_{DD} = AV_{DD} = +2.7 to 5.5 V AV_{REF2} = 0.75V_{DD} AV_{REF3} = 0.25V_{DD}			0.8	%
		Load conditions: 2 MΩ, 30 pF	V_{DD} = AV_{DD} = AV_{REF2} = +2.7 to 5.5 V AV_{REF3} = 0 V			0.8	%
			V_{DD} = AV_{DD} = +2.7 to 5.5 V AV_{REF2} = 0.75V_{DD} AV_{REF3} = 0.25V_{DD}			1.0	%
Settling time		Load conditions: 2 MΩ, 30 pF				10	μs
Output resistance	R_O	DACS0, 1 = 55 H			10		kΩ
Analog reference voltage	AV_{REF2}			0.75V_{DD}		V_{DD}	V
	AV_{REF3}			0		0.25V_{DD}	V
Resistance of AV_{REF2} and A_{VREF3}	R_{AIREF}	DACS0, 1 = 55 H		4	8		kΩ
Reference power supply input current	AI_{REF2}			0		5	mA
	AI_{REF3}			–5		0	mA

DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = +2.7 to 5.5 V		30	50	μA
		V_{DDDR} = +2.5 V		10	40	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (to STOP mode setting)	t_{HVD}		0			ms
STOP clear signal input time	t_{DREL}		0			ms
Oscillation settling time	t_{WAIT}	Crystal	30			ms
		Ceramic resonator	5			ms
Input low voltage	V_{IL}	Specific pins**Note**	0		$0.1V_{DDDR}$	V
Input high voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

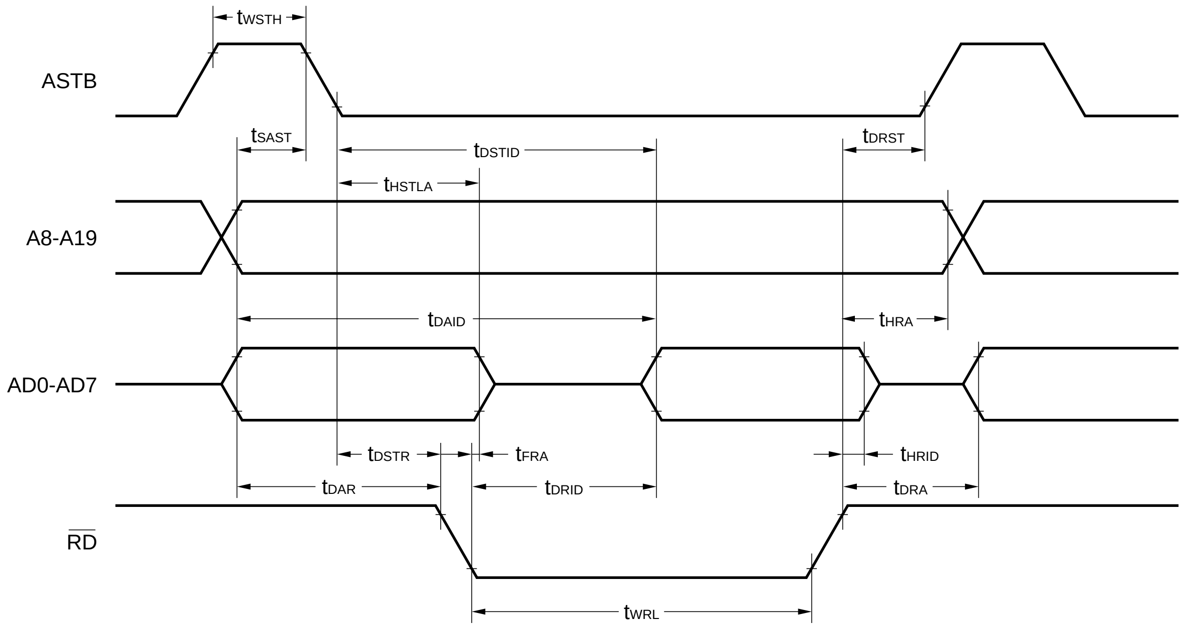
Note $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$/SCL, and P33/SO0/SDA pins

AC TIMING TEST POINTS

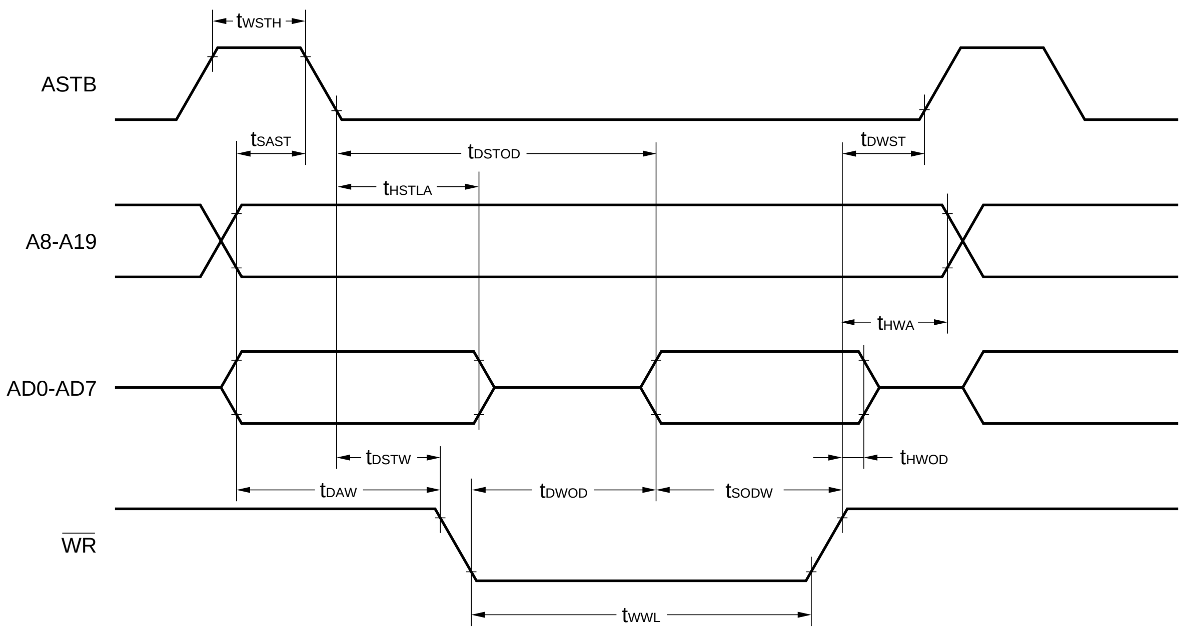


TIMING WAVEFORM

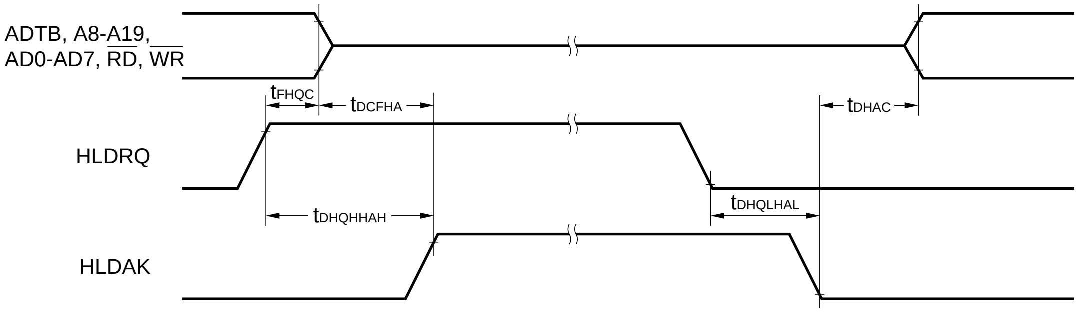
(1) Read operation



(2) Write operation

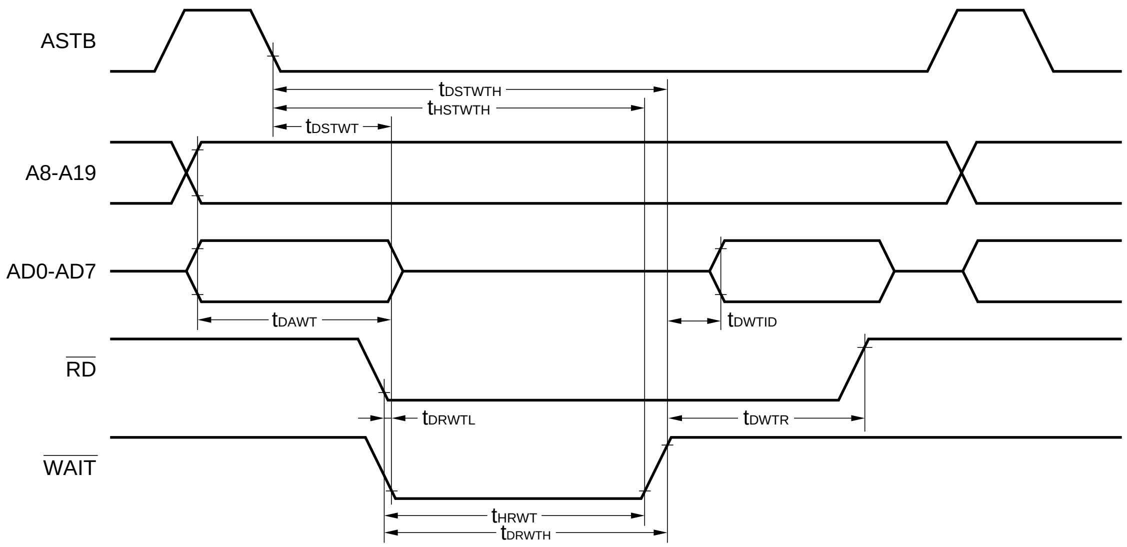


HOLD TIMING

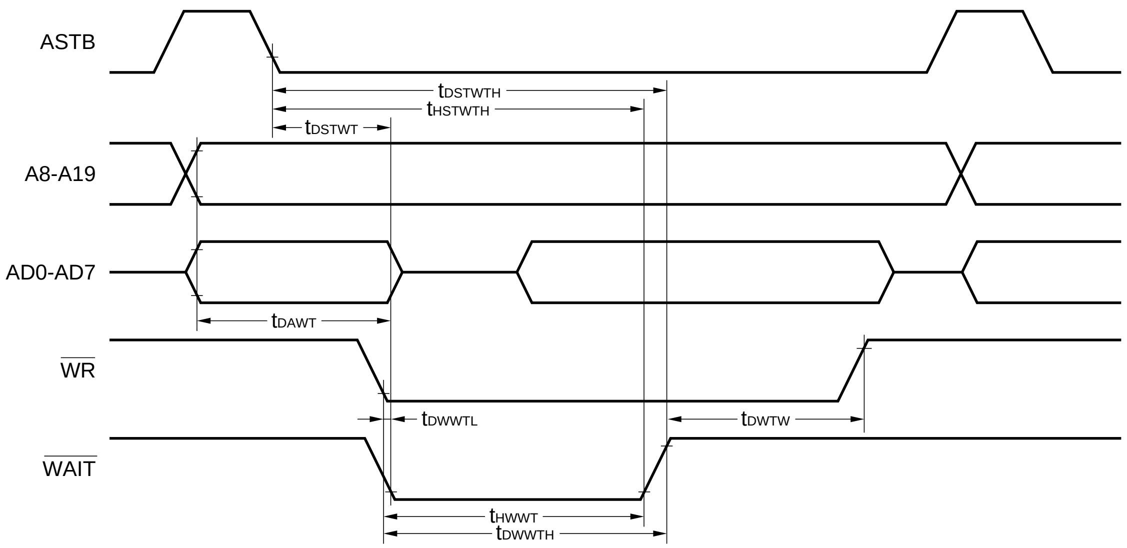


EXTERNAL WAIT SIGNAL INPUT TIMING

(1) Read operation

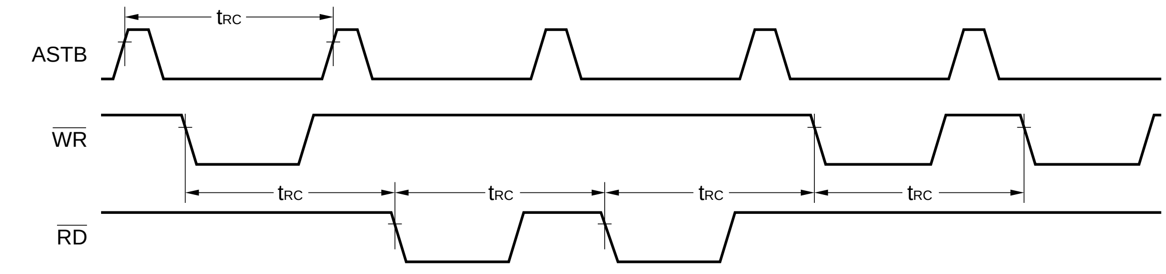


(2) Write operation

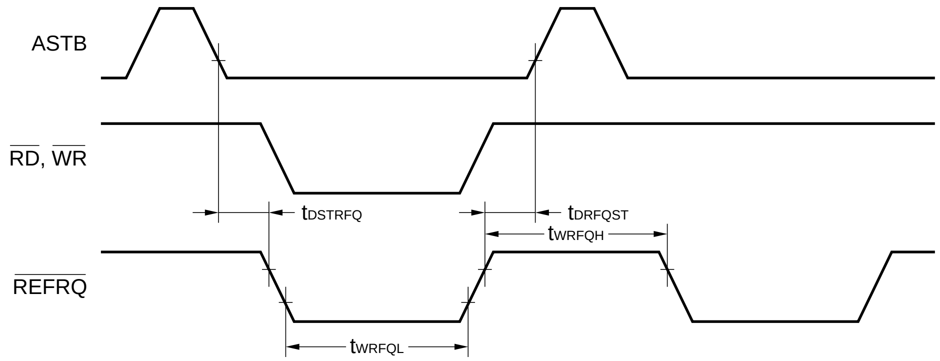


REFRESH TIMING WAVEFORM

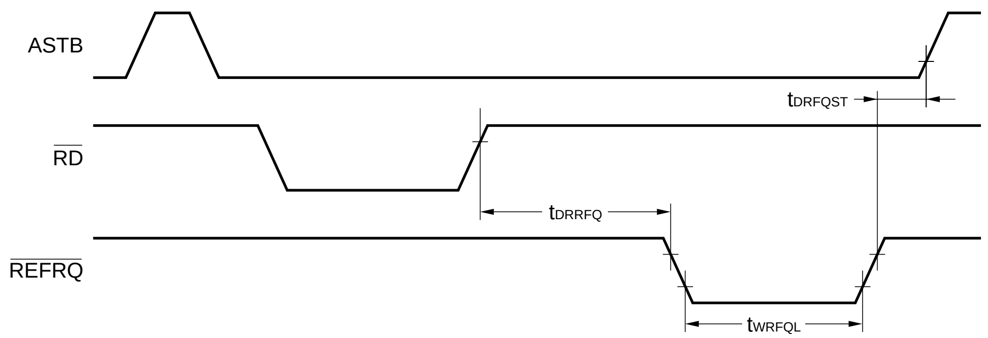
(1) Random read/write cycle



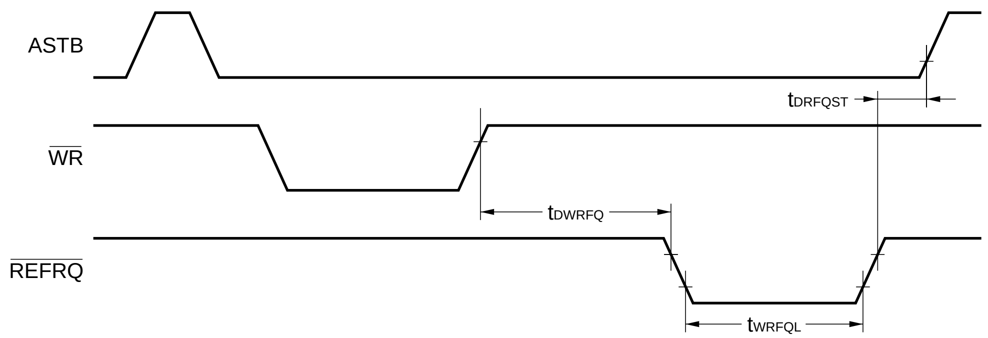
(2) When refresh memory is accessed for a read and write at the same time



(3) Refresh after a read

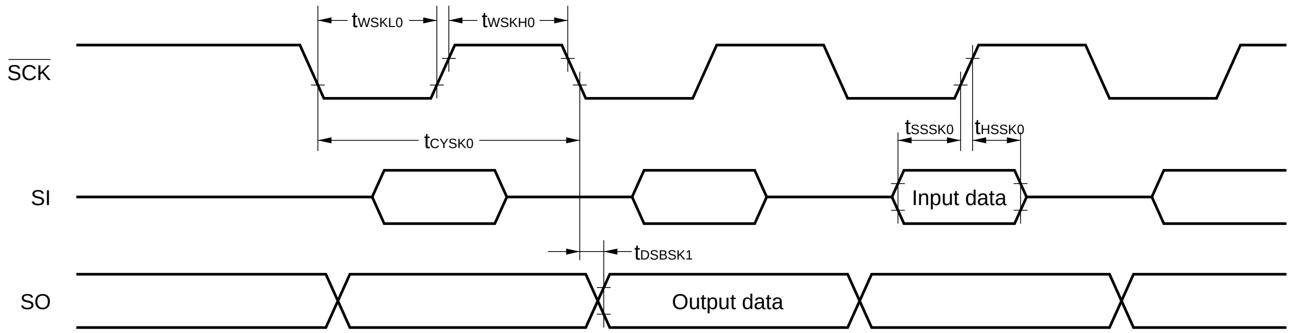


(4) Refresh after a write

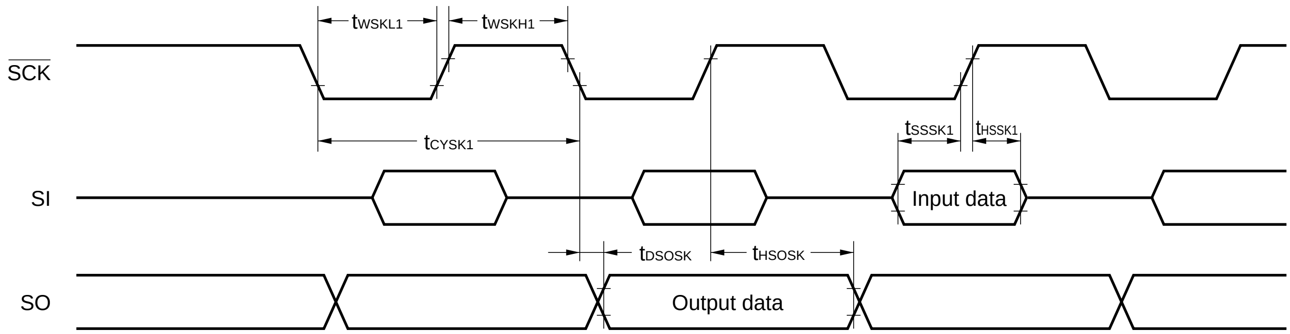


SERIAL OPERATION

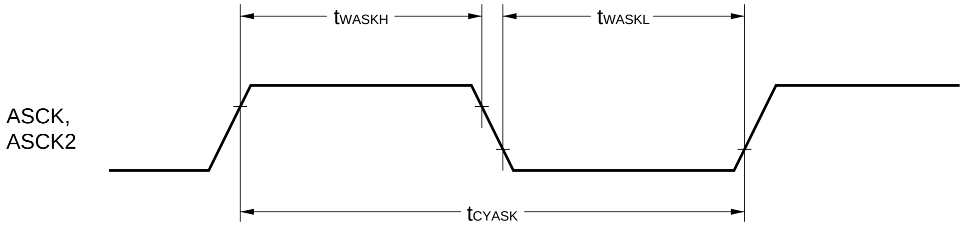
★ (1) CSI



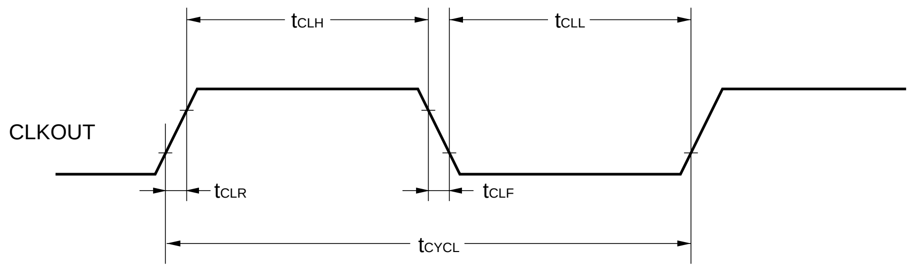
(2) IOE1, IOE2



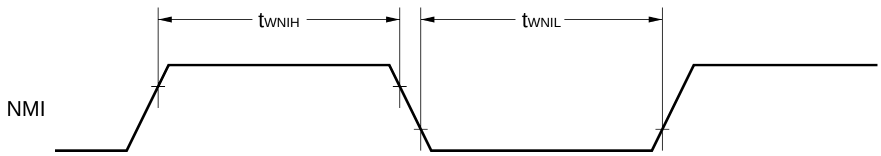
(3) UART, UART2

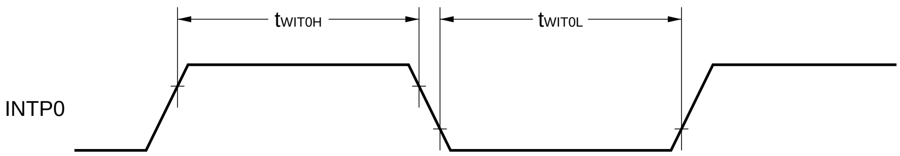


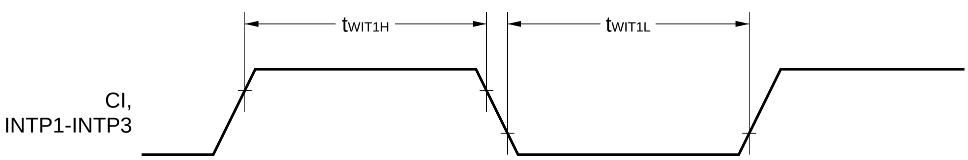
CLOCK OUTPUT TIMING

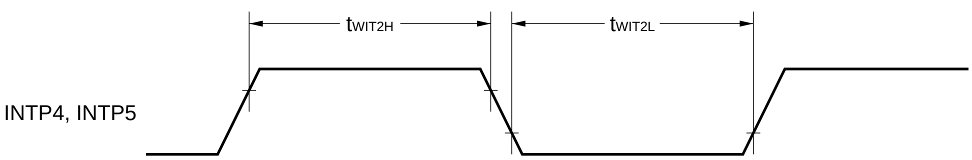


INTERRUPT INPUT TIMING

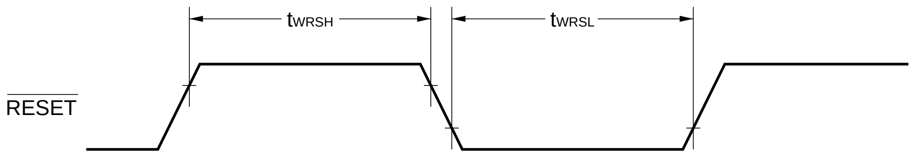




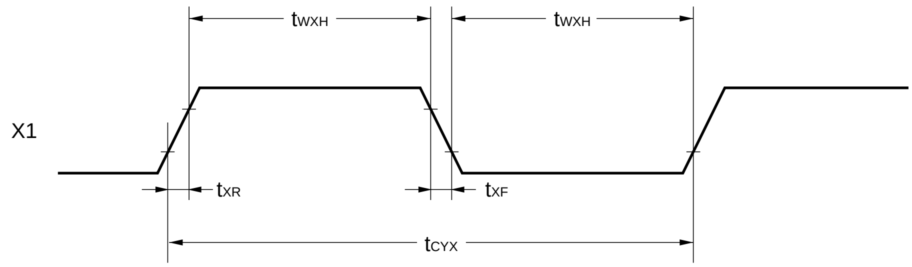




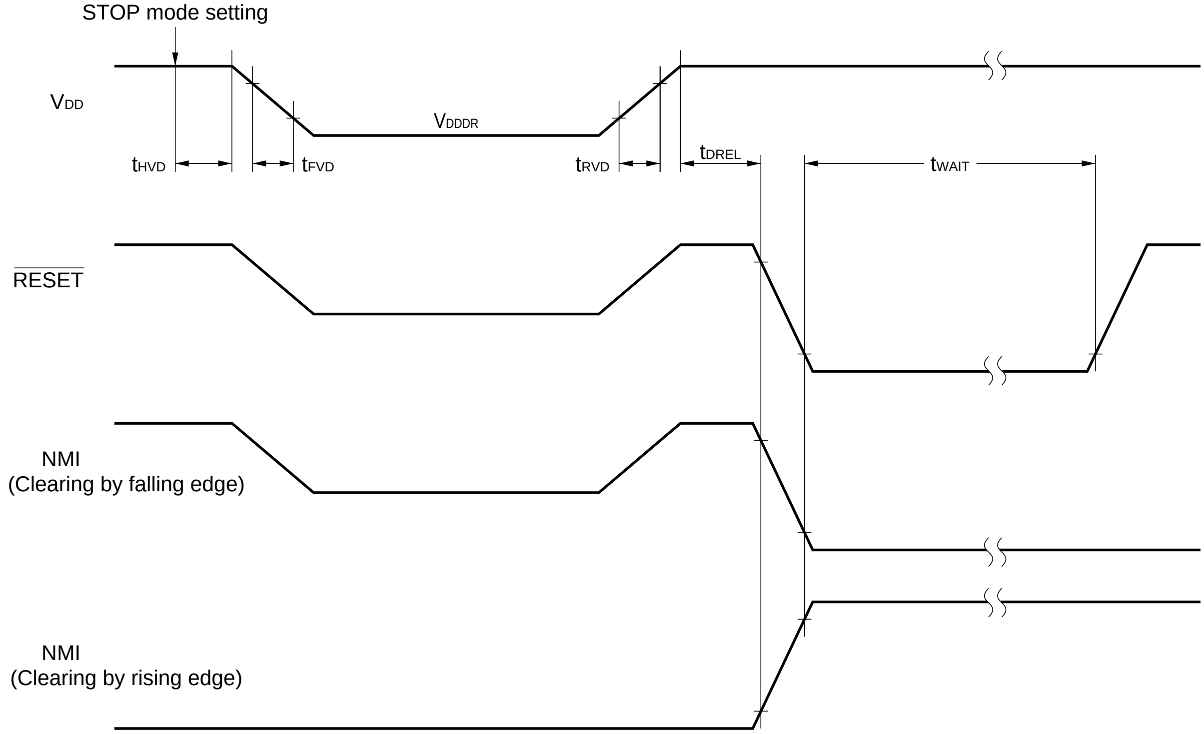
RESET INPUT TIMING



EXTERNAL CLOCK TIMING



DATA RETENTION CHARACTERISTICS



DC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5°C, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.2		V_{DDP} + 0.3	V
Low-level input voltage	V_{IL}	V_{IL}		–0.3		+0.8	V
Input leakage current	I_{LIP}	I_{LI}	0 ≤ V_I ≤ V_{DDP}[Note 2]			±10	μA
High-level output voltage	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}	–	0 ≤ V_O ≤ V_{DDP}, $\overline{OE}$ = V_{IH}			±10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} supply current	I_{DD}	I_{DD}	Program memory write mode		10	40	mA
			Program memory read mode		10	40	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode		5	50	mA
			Program memory read mode		1.0	100	μA

Notes 1. Symbols for the corresponding μPD27C1001A

2. The V_{DDP} represents the V_{DD} pin as viewed in the programming mode.

AC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5°C, V_{SS} = 0 V)

PROM Write Mode (Page Program Mode)

Parameter	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		130	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}			1	2	ns
$\overline{OE}$ pulse width in the data latch	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the corresponding μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Write Mode (Byte Program Mode)

Parameter	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		130	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}			1	2	ns

Notes 1. These symbols (except t_{VDS}) correspond to those of the corresponding μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

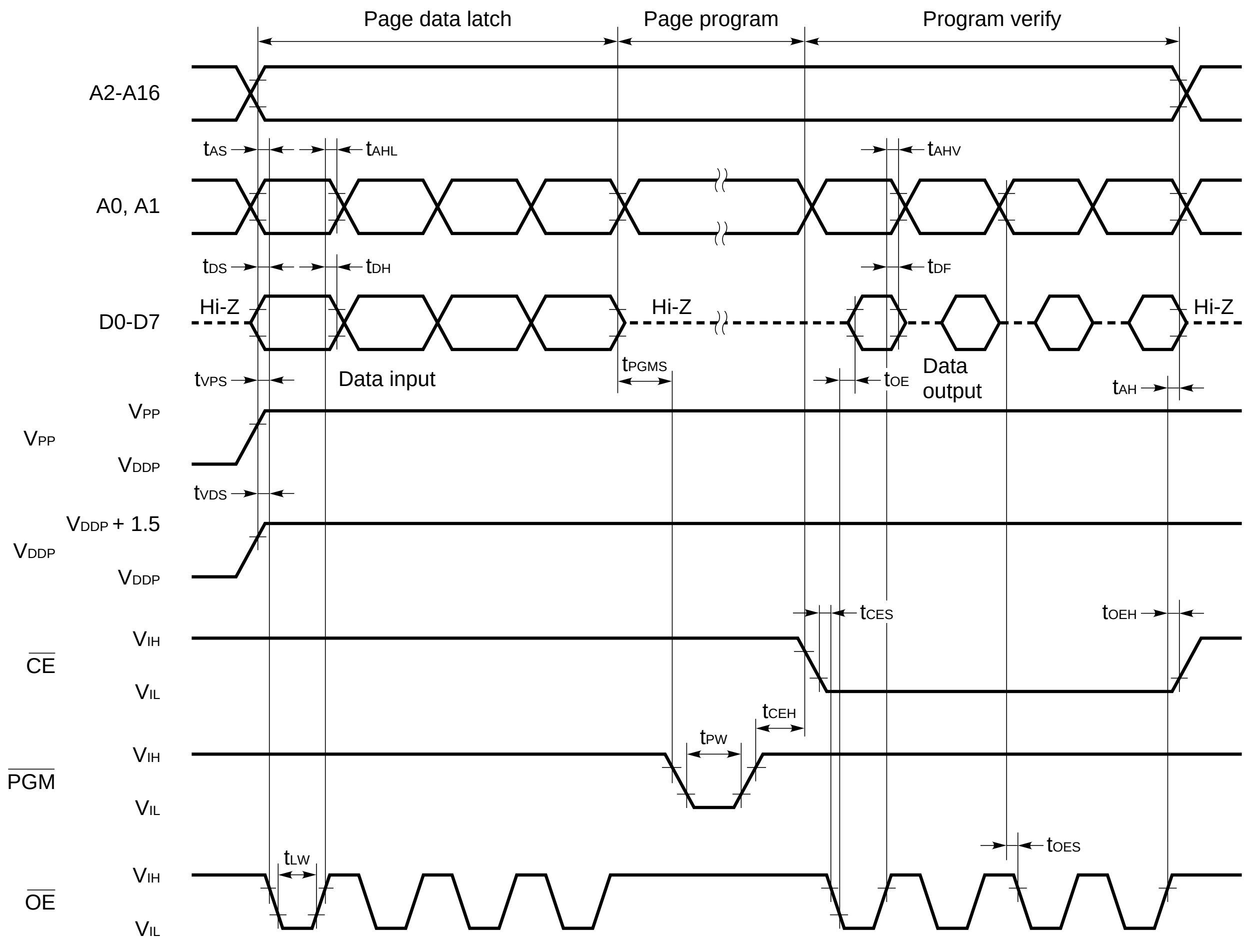
PROM Read Mode

Parameter	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
Data output time from address	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			200	ns
Delay from $\overline{CE}$ ↓ to data output	t_{CE}	$\overline{OE} = V_{IL}$		1	2	μs
Delay from $\overline{OE}$ ↓ to data output	t_{OE}	$\overline{CE} = V_{IL}$		1	2	μs
Data hold time to $\overline{OE}$↑ or $\overline{CE}$↑[Note 2]	t_{DF}	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$	0		60	ns
Data hold time to address	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

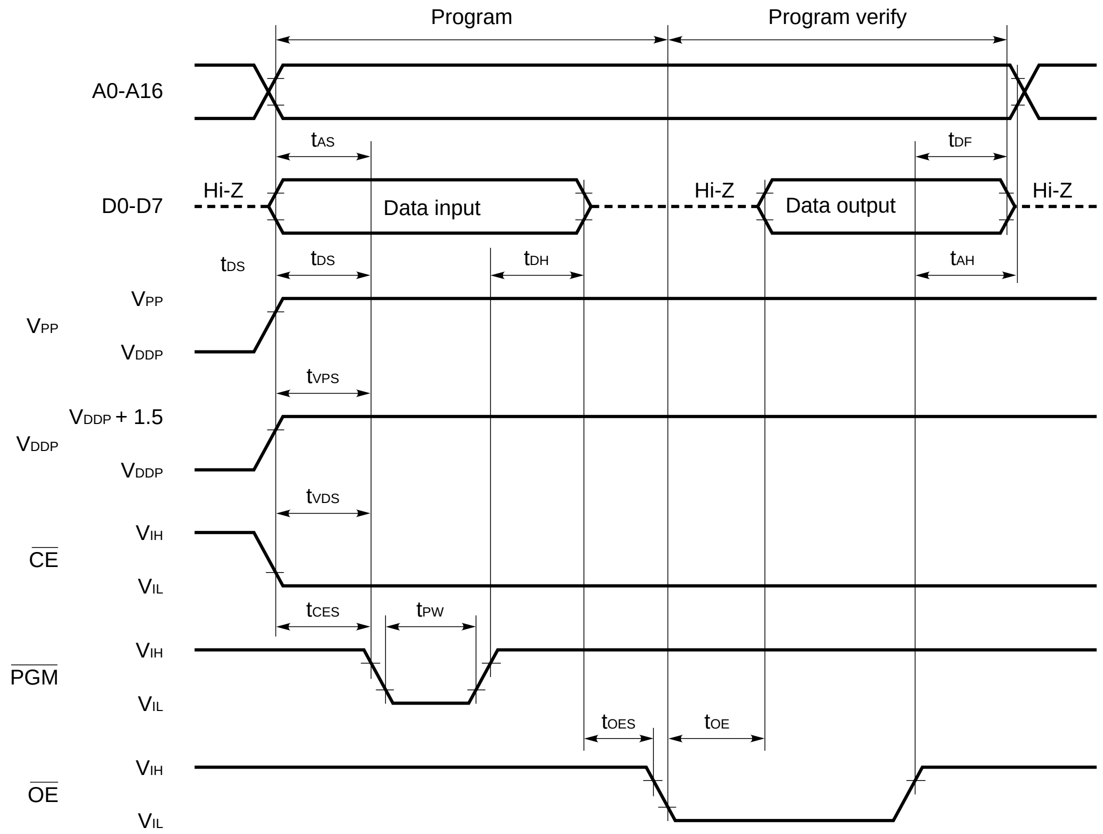
Notes 1. These symbols correspond to those of the corresponding μPD27C1001A.

2. t_{DF} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

PROM Write Mode Timing (Page Program Mode)



PROM Write Mode Timing (Byte Program Mode)

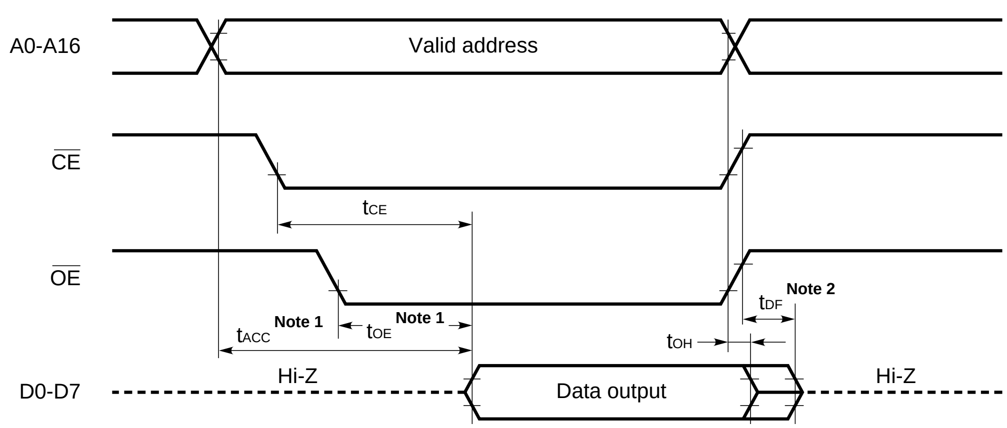


Cautions 1. V_{DDP} must be applied before V_{PP}, and must be cut after V_{PP}.

2. V_{PP} including overshoot must not exceed +13.5 V.

3. Plugging in or out the board with the V_{PP} pin supplied with +12.5 V may adversely affect its reliability.

PROM Read Mode Timing

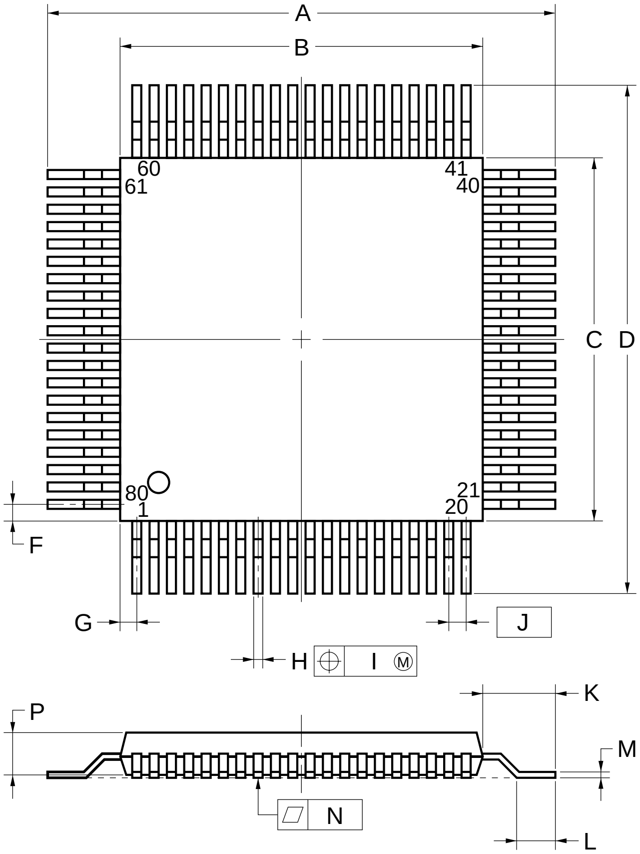


Notes 1. For reading within t_{ACC}, the delay of the $\overline{OE}$ input from falling edge of $\overline{CE}$ must be within t_{ACC}-t_{OE}.

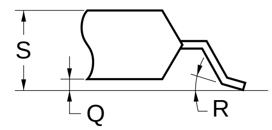
2. t_{DF} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

12. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14x14)



detail of lead end



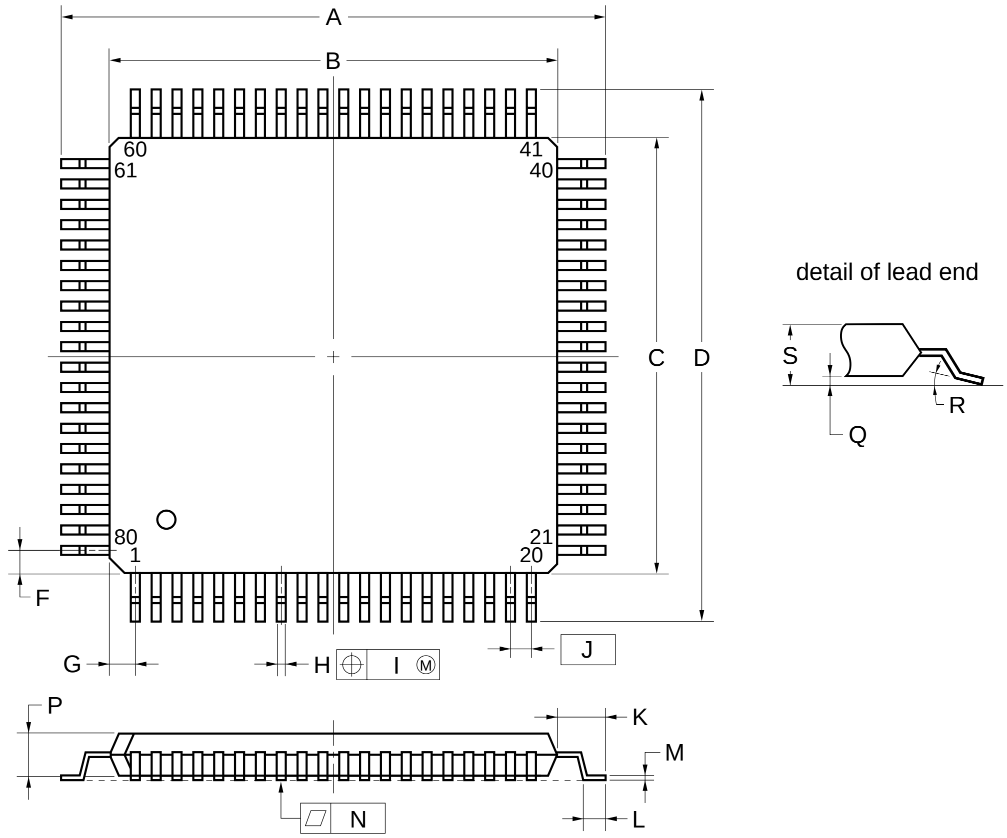
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-5

80 PIN PLASTIC QFP (14×14)



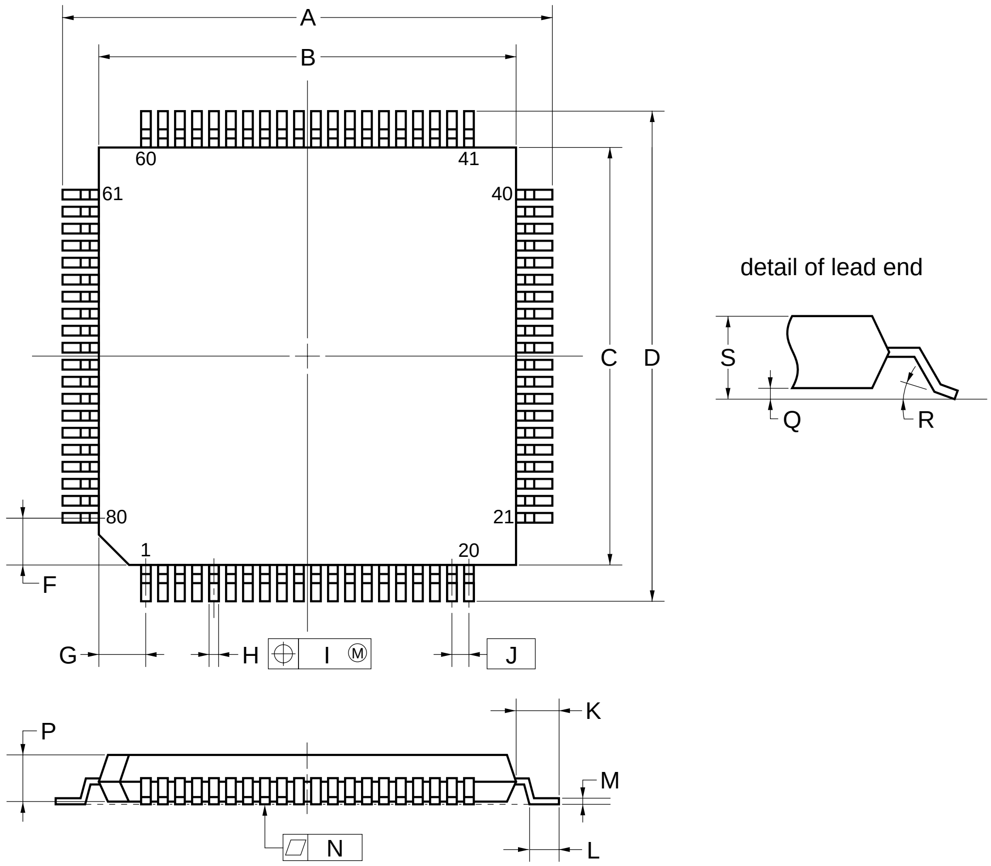
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (12×12)



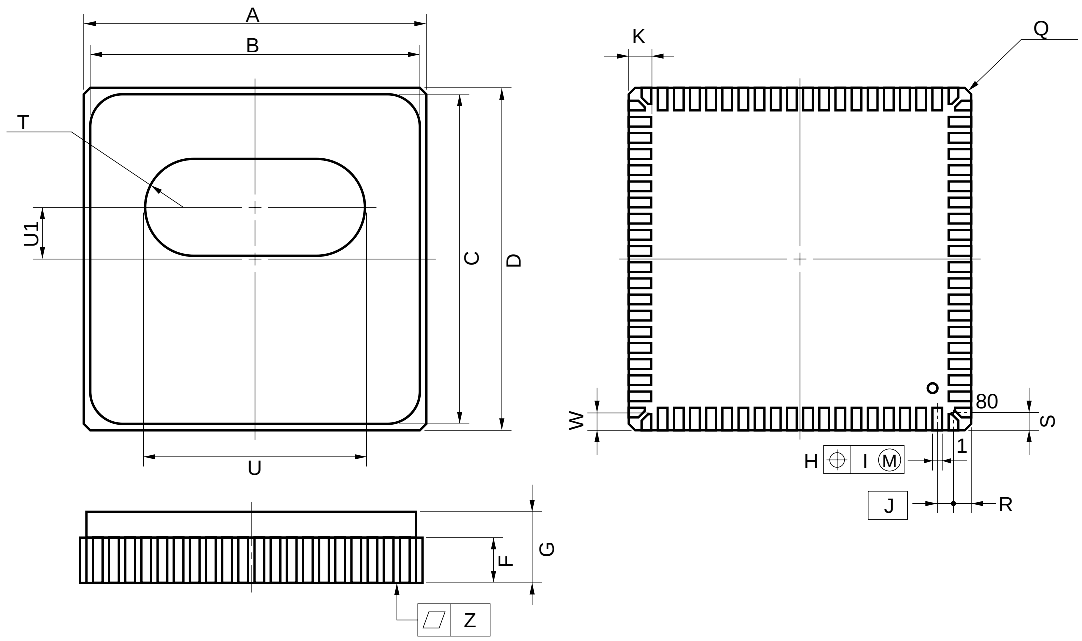
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.00±0.20	0.551±0.008
B	12.00±0.20	$0.472^{+0.009}_{-0.008}$
C	12.00±0.20	$0.472^{+0.009}_{-0.008}$
D	14.00±0.20	0.551±0.008
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.10±0.05	0.004±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-5

80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

13. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78P4038.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 13-1. Soldering Conditions for Surface-Mount Devices (1/2)

(1) μPD78P4038GC-3B9: 80-pin plastic QFP (14 × 14 × 2.7 mm)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 3	IR35-00-3
VPS	Peak package's surface temperature: 215°C Reflow time: 40 seconds or less (200°C or more) Maximum allowable number of reflow processes: 3	VP15-00-3
Wave soldering	Solder temperature: 260°C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120°C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300°C or less Heat time: 3 seconds or less (for one side of a device)	–

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

(2) μPD78P4038GC-8BT: 80-pin plastic QFP (14 × 14 × 1.4 mm)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 2	IR35-00-2
VPS	Peak package's surface temperature: 215°C Reflow time: 40 seconds or less (200°C or more) Maximum allowable number of reflow processes: 2	VP15-00-2
Wave soldering	Solder temperature: 260°C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120°C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300°C or less Heat time: 3 seconds or less (for one side of a device)	–

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

Table 13-1. Soldering Conditions for Surface-Mount Devices (2/2)

(3) μPD78P4038GK-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125°C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-107-2
VPS	Peak package's surface temperature: 215°C Reflow time: 40 seconds or less (200°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125°C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-107-2
Partial heating method	Terminal temperature: 300°C or less Heat time: 3 seconds or less (for one side of a device)	–

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

★ ## APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78P4038.
See also **(5)**.

(1) Language processing software

RA78K4	Assembler package for all 78K/IV Series models
CC78K4	C compiler package for all 78K/IV Series models
DF784038	Device file for μPD784038 Subseries models
CC78K4-L	C compiler library source file for all 78K/IV Series models

(2) PROM write tools

PG-1500	PROM programmer
PA-78P4026GC PA-78P4038GK PA-78P4026KK	Programmer adaptor, connects to PG-1500
PG-1500 controller	Control program for PG-1500

(3) Debugging tools

- **When using the in-circuit emulator IE-78K4-NS**

IE-78K4-NS	In-circuit emulator for all 78K/IV Series models
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine
IE-70000-CD-IF	PC card and interface cable when a PC-9800 series notebook is used as the host machine
IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT™ or compatible is used as the host machine
IE-784038-NS-EM1 **Note**	Emulation board for evaluating μPD784038 Subseries models
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-3B9 and GC-8BT types)
NP-80GK **Note**	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Socket for mounting on target system board made for 80-pin plastic QFP (GC-3B9 and GC-8BT types)
TGK-080SDW	Adapter for mounting on target system board made for 80-pin plastic TQFP (fine pitch) (GK-BE9 type)
EV-9900	Tool used to remove the μPD78P4038KK-T from the EV-9200GC-80
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator for all 78K/IV Series models
DF784038	Device file for μPD784038 Subseries models

Note Under development

- **When using the in-circuit emulator IE-784000-R**

IE-784000-R	In-circuit emulator for all 78K/IV Series models
IE-70000-98-IF-B IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine
IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series notebook is used as the host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT or compatible is used as the host machine
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
IE-784038-NS-EM1 Note IE-784038-R-EM1	Emulation board for evaluating μPD784038 Subseries models
IE-78400-R-EM	Emulation board for all 78K/IV Series models
IE-78K4-R-EX2 Note	Conversion board for 80 pins to use the IE-784038-NS-EM1 on the IE-784000-R. The board is not needed when the conventional product IE-784038-R-EM1 is used.
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-3B9 and GC-8BT types)
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (fine pitch) (GK-BE9 type) for all μPD784038 Subseries
EV-9200GC-80	Socket for mounting on target system board made for 80-pin plastic QFP (GC-3B9 and GC-8BT types)
TGK-080SDW	Adapter for mounting on target system board made for 80-pin plastic TQFP (fine pitch) (GK-BE9 type)
EV-9900	Tool used to remove the μPD78P4038KK-T from the EV-9200GC-80
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator for all 78K/IV Series models
DF784038	Device file for μPD784038 Subseries models

Note Under development

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series models
MX78K4	OS for 78K/IV Series models

(5) **Notes when using development tools**

- The ID78K4-NS, ID78K4, and SM78K4 can be used in combination with the DF784038.
- The CC78K4 and RX78K/IV can be used in combination with the RA78K4 and DF784038.
- The NP-80GC is a product from Naito Densei Machida Mfg. Co., Ltd. (044-822-3813). Consult the NEC sales representative for purchasing.
- The TGK-080SDW is a product from TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd.
  Tokyo Electronic Components Division (03-3820-7112)
  Osaka Electronic Components Division (06-244-6672)
- The host machines and operating systems corresponding to each software are shown below.

Host Machine [OS] / Software	PC	EWS
	PC-9800 Series [Windows™] IBM PC/AT and compatibles [Windows]	HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	○Note	○
CC78K4	○Note	○
PG-1500 controller	○Note	–
ID78K4-NS	○	–
ID78K4	○	○
SM78K4	○	–
RX78K/IV	○Note	○
MX78K4	○Note	○

Note Software under MS-DOS

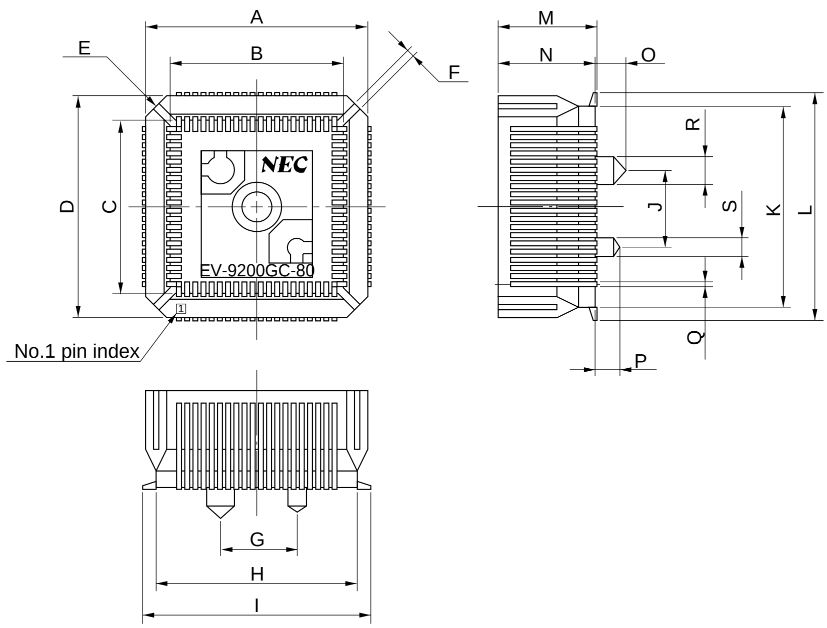
APPENDIX B CONVERSION SOCKET (EV-9200GC-80) AND CONVERSION ADAPTER (TGK-080SDW)

(1) Conversion socket (EV-9200GC-80) package drawings and recommended pattern to mount the socket

Connect the μPD78P4038YKK-T (80-pin ceramic WQFN (14 × 14 mm)) and EP-78230GC-R to the circuit board in combination with the EV-9200GC-80.

Figure B-1. Package Drawings of EV-9200GC-80 (Reference) (unit: mm)

Based on EV-9200GC-80
(1) Package drawing (in mm)

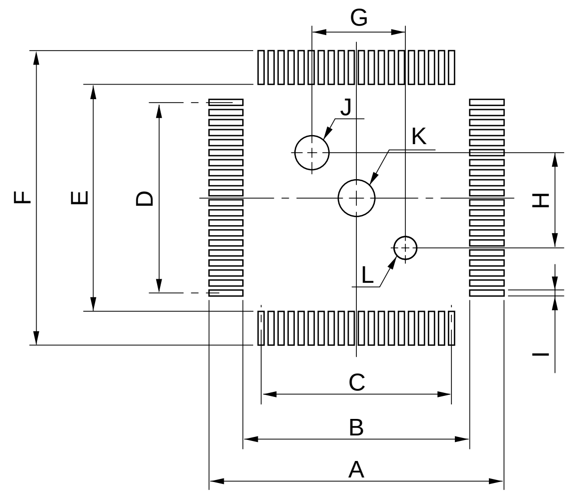


EV-9200GC-80-G0E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	1.5	0.059

Figure B-2. Recommended Pattern to Mount EV-9200GC-80 on a Substrate (Reference) (unit: mm)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002}$ × 0.748=0.486 $^{+0.003}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002}$ 0.748=0.486 $^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0±0.05	$0.236^{+0.003}_{-0.002}$
H	6.0±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

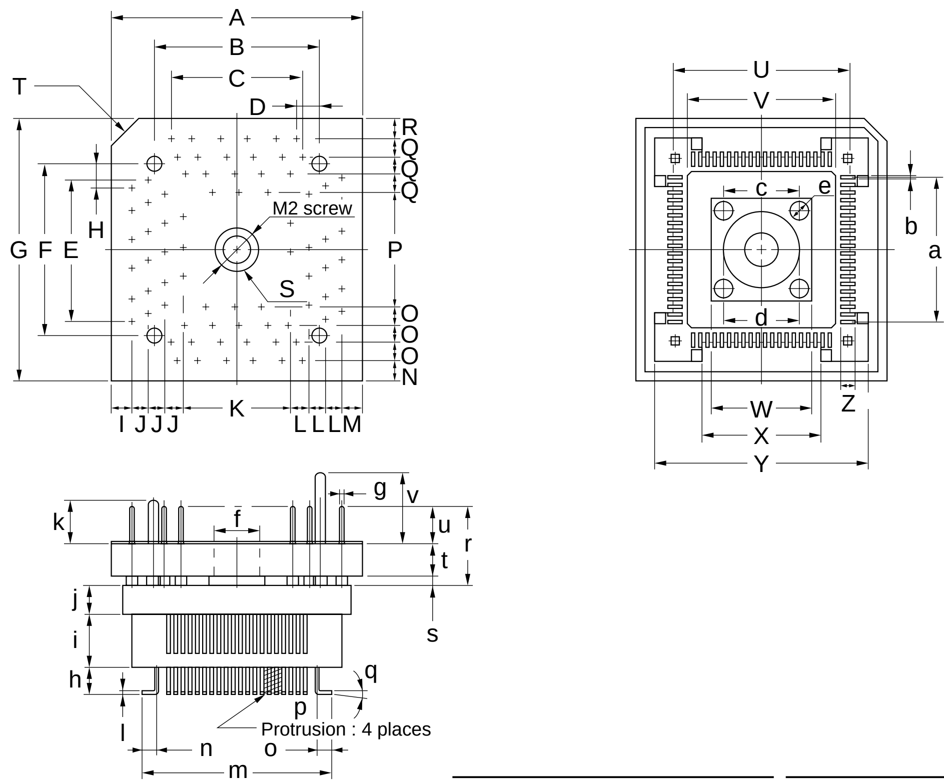
Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

(2) Conversion adapter (TGK-080SDW) package drawings

Connect the μPD78P4038GK-BE9 (80-pin plastic TQFP (fine pitch: 12 × 12 mm)) to the circuit board in combination with the TGK-080SDW.

Figure B-3. Package Drawings of TGK-080SDW (Reference) (unit: mm)

TGK-080SDW (TQPACK080SD + TQSOCKET080SDW)
Package dimension (unit: mm)



ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	11.77	0.463
C	0.5x19=9.5	0.020x0.748=0.374
D	0.5	0.020
E	0.5x19=9.5	0.020x0.748=0.374
F	11.77	0.463
G	18.0	0.709
H	0.5	0.020
I	1.58	0.062
J	1.2	0.047
K	7.64	0.301
L	1.2	0.047
M	1.58	0.062
N	1.58	0.062
O	1.2	0.047
P	7.64	0.301
Q	1.2	0.047
R	1.58	0.062
S	φ3.55	φ0.140
T	C 2.0	C 0.079
U	12.31	0.485
V	10.17	0.400
W	6.8	0.268
X	8.24	0.324
Y	14.8	0.583
Z	1.4±0.2	0.055±0.008

ITEM	MILLIMETERS	INCHES
a	0.5x19=9.5±0.10	0.020x0.748=0.374±0.004
b	0.25	0.010
c	φ5.3	φ0.209
d	φ5.3	φ0.209
e	φ1.3	φ0.051
f	φ3.55	φ0.140
g	φ0.3	φ0.012
h	1.85±0.2	0.073±0.008
i	3.5	0.138
j	2.0	0.079
k	3.0	0.118
l	0.25	0.010
m	14.0	0.551
n	1.4±0.2	0.055±0.008
o	1.4±0.2	0.055±0.008
p	h=1.8 φ1.3	h=0.071 φ0.051
q	0~5°	0.000~0.197°
r	5.9	0.232
s	0.8	0.031
t	2.4	0.094
u	2.7	0.106
v	3.9	0.154

TGK-080SDW-G1E

note: Product by TOKYO ELETECH CORPORATION.

APPENDIX C RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	English	Japanese
μPD784031 Data Sheet	U11507E	U11507J
μPD784035, 784036, 784037, 784038 Data Sheet	U10847E	U10847J
μPD78P4038 Data Sheet	This manual	U10848J
μPD784038, 784038Y Sub-Series User's Manual, Hardware	U11316E	U11316J
μPD784038 Sub-Series Special Function Registers	–	U11090J
78K/IV Series User's Manual, Instruction	U10905E	U10905J
78K/IV Series Instruction Summary Sheet	–	U10594J
78K/IV Series Instruction Set	–	U10595J
78K/IV Series Application Note, Software Basic	–	U10095J

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Documents Related to Development Tools (User's Manual)

Document Name		Document No.	
		English	Japanese
RA78K4 Assembler Package	Operation	U11334E	U11334J
	Language	U11162E	U11162J
RA78K Series Structured Assembler Preprocessor		U11743E	U11743J
CC78K4 Series	Operation	U11572E	U11572J
	Language	U11571E	U11571J
CC78K Series Library Source File		U12322E	U12322J
PG-1500 PROM Programmer		U11940E	U11940J
PG-1500 Controller PC-9800 Series (MS-DOS™) Base		EEU-1291	EEU-704
PG-1500 Controller IBM PC Series (PC DOS™) Base		U10540E	EEU-5008
IE-78K4-NS		To be released soon	U13356J
IE-784000-R		EEU-1534	U12903J
IE-784038-NS-EM1		To be created	To be created
IE-784038-R-EM1		U11383E	U11383J
EP-78230		EEU-1515	EEU-985
EP-78054GK-R		EEU-1468	EEU-932
SM78K4 System Simulator Windows Base	Reference	U10093E	U10093J
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092E	U10092J
ID78K4-NS Integrated Debugger	Reference	U12796E	U12796J
ID78K4 Integrated Debugger Windows Base	Reference	U10440E	U10440J
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Base	Reference	U11960E	U11960J

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

Documents Related to Software to Be Incorporated into the Product (User's Manual)

Document Name		Document No.	
		English	Japanese
78K/IV Series Real-Time OS	Basic	U10603E	U10603J
	Installation	U10604E	U10604J
	Debugger	–	U10364J
OS for 78K/IV Series MX78K4	Basic	–	U11779J

★ Other Documents

Document Name	Document No.	
	English	Japanese
IC PACKAGE MANUAL	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Device	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Semiconductor Device Quality Control/Reliability Handbook	–	C12769J
Guide for Products Related to Microcomputer: Other Companies	–	U11416J

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

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