Single-Supply, Rail-to-Rail Low Power FET-Input Op Amp

AD822

FEATURES
True Single-Supply Operation
- **Output Swings Rail-to-Rail**
- **Input Voltage Range Extends Below Ground**
- **Single-Supply Capability from 3 V to 36 V**
- **Dual-Supply Capability from ±1.5 V to ±18 V**

High Load Drive
- **Capacitive Load Drive of 350 pF, G = +1**
- **Minimum Output Current of 15 mA**

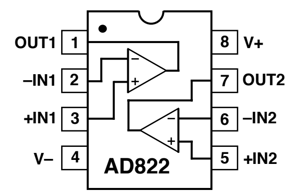
Excellent AC Performance for Low Power
- **800 μA Max Quiescent Current per Amplifier**
- **Unity Gain Bandwidth: 1.8 MHz**
- **Slew Rate of 3.0 V/ms**

Good DC Performance
- **800 μV Max Input Offset Voltage**
- **2 μV/°C Typ Offset Voltage Drift**
- **25 pA Max Input Bias Current**

Low Noise
13 nV/√Hz @ 10 kHz
No Phase Inversion

APPLICATIONS
Battery-Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

CONNECTION DIAGRAM
8-Lead Plastic DIP, MSOP, and SOIC



GENERAL DESCRIPTION

The AD822 is a dual precision, low power FET input op amp that can operate from a single supply of 3.0 V to 36 V or dual supplies of ±1.5 V to ±18 V. It has true single-supply capability with an input voltage range extending below the negative rail, allowing the AD822 to accommodate input signals below ground in the Single-Supply Mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.

Offset voltage of 800 μV maximum, offset voltage drift of 2 μV/°C, input bias currents below 25 pA, and low input voltage noise provide dc precision with source impedances up to a gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz, and 3 V/μs slew rate are provided with a low supply current of 800 μA per amplifier. The AD822 drives up to 350 pF of direct capacitive load as a follower and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. Its combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single-supply user.

The AD822 is available in two performance grades. The A and B grades are rated over the industrial temperature range of –40°C to +85°C.

The AD822 is offered in three varieties of 8-lead packages: plastic PDIP, MSOP, and SOIC.

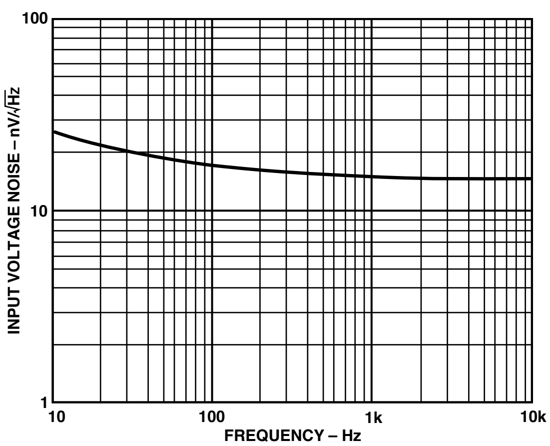


Figure 1. Input Voltage Noise vs. Frequency

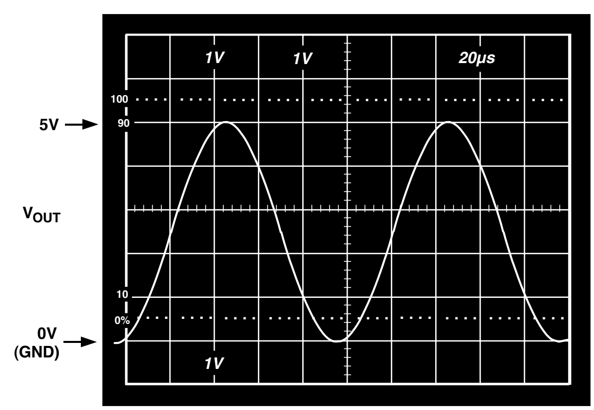


Figure 2. Gain-of-2 Amplifier; V_S = 5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 V, R_L = 100 kΩ

REV. E

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AD822–SPECIFICATIONS (V_S = 0, 5 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V, unless otherwise noted.)

Parameter	Conditions	AD822A Min	AD822A Typ	AD822A Max	AD822B Min	AD822B Typ	AD822B Max	Unit
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V							
	R_L = 100 kΩ	500	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10 kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1 kΩ	15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ to 2.5 V							
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4		μs
to 0.01%			1.8			1.8		μs
MATCHING CHARACTERISTICS								
Initial Offset				1.0			0.5	mV
Max Offset over Temperature				1.6			1.3	mV
Offset Drift			3			3		μV/°C
Input Bias Current				20			10	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130		dB
f = 100 kHz			–93			–93		dB
INPUT CHARACTERISTICS								
Input Voltage Range[1]		–0.2		+4	–0.2		+4	V
T_{MIN} to T_{MAX}		–0.2		+4	–0.2		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 2 V	66	80		69	80		dB
T_{MIN} to T_{MAX}	V_{CM} = 0 V to 2 V	66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current T_{MIN} to T_{MAX}			1.24	1.6		1.24	1.6	mA
Power Supply Rejection	V_S+ = 5 V to 15 V	66	80		70	80		dB
T_{MIN} to T_{MAX}		66			70			dB

Specifications subject to change without notice.

SPECIFICATIONS (V_S = ±5 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0 V, unless otherwise noted.)

Parameter	Conditions	AD822A Min	AD822A Typ	AD822A Max	AD822B Min	AD822B Typ	AD822B Max	Unit
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Max Offset over Temperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_{CM} = –5 V to +4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = –4 V to +4 V							
	R_L = 100 kΩ	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10 kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1 kΩ	20	30		20	30		V/mV
T_{MIN} to TMAX		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_O = ±4.5 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4		μs
to 0.01%			1.8			1.8		μs
MATCHING CHARACTERISTICS								
Initial Offset				1.0			0.5	mV
Max Offset over Temperature				3			2	mV
Offset Drift			3			3		μV/°C
Input Bias Current				25			10	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130		dB
f = 100 kHz			–93			–93		dB
INPUT CHARACTERISTICS								
Input Voltage Range[1]		–5.2		+4	–5.2		+4	V
T_{MIN} to T_{MAX}		–5.2		+4	–5.2		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = –5 V to +2 V	66	80		69	80		dB
T_{MIN} to T_{MAX}	V_{CM} = –5 V to +2 V	66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current T_{MIN} to T_{MAX}			1.3	1.6		1.3	1.6	mA
Power Supply Rejection	V_S+ = 5 V to 15 V	66	80		70	80		dB
T_{MIN} to T_{MAX}		66			70			dB

Specifications subject to change without notice.

SPECIFICATIONS (V_S = ±15 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0 V, unless otherwise noted.)

Parameter	Conditions	AD822A Min	AD822A Typ	AD822A Max	AD822B Min	AD822B Typ	AD822B Max	Unit
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.5	mV
Max Offset over Temperature			0.5	3		0.5	2.5	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	12	pA
	V_{CM} = –10 V		40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	12	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = +10 V to –10 V							
R_L = 100 kΩ	500	2000		500	2000		V/mV	
T_{MIN} to T_{MAX}		500			500			V/mV
R_L = 10 kΩ	100	500		100	500		V/mV	
T_{MIN} to T_{MAX}		100			100			V/mV
R_L = 1 kΩ	30	45		30	45		V/mV	
T_{MIN} to T_{MAX}		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_O = ±10 V		–85			–85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1		µs
to 0.01%			4.5			4.5		µs
MATCHING CHARACTERISTICS								
Initial Offset				3			2	mV
Max Offset over Temperature				4			2.5	mV
Offset Drift			3			3		µV/°C
Input Bias Current				25			12	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130		dB
f = 100 kHz			–93			–93		dB
INPUT CHARACTERISTICS								
Input Voltage Range[1]		–15.2		+14	–15.2		+14	V
T_{MIN} to T_{MAX}		–15.2		+14	–15.2		+14	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = –15 V to +12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}	V_{CM} = –15 V to +12 V		70			74		dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current T_{MIN} to T_{MAX}			1.4	1.8		1.4	1.8	mA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

Specifications subject to change without notice.

SPECIFICATIONS (V_S = 0, 3 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V, unless otherwise noted.)

Parameter	Conditions	Typ	Unit
DC PERFORMANCE			
Initial Offset		0.2	mV
Max Offset over Temperature		0.5	mV
Offset Drift		1	µV/°C
Input Bias Current	V_{CM} = 0 V to 2 V	2	pA
at T_{MAX}		0.5	nA
Input Offset Current		2	pA
at T_{MAX}		0.5	nA
Open-Loop Gain	V_O = 0.2 V to 2 V		
R_L = 100 kΩ		1000	V/mV
R_L = 10 kΩ		150	V/mV
R_L = 1 kΩ		30	V/mV
NOISE/HARMONIC PERFORMANCE			
Input Voltage Noise			
0.1 Hz to 10 Hz		2	µV p-p
f = 10 Hz		25	nV/√Hz
f = 100 Hz		21	nV/√Hz
f = 1 kHz		16	nV/√Hz
f = 10 kHz		13	nV/√Hz
Input Current Noise			
0.1 Hz to 10 Hz		18	fA p-p
f = 1 kHz		0.8	fA/√Hz
Harmonic Distortion	R_L = 10 kΩ to 1.5 V		
f = 10 kHz	V_O = ±1.25 V	–92	dB
DYNAMIC PERFORMANCE			
Unity Gain Frequency		1.5	MHz
Full Power Response	V_O p-p = 2.5 V	240	kHz
Slew Rate		3	V/µs
Settling Time			
to 0.1%	V_O = 0.2 V to 2.5 V	1	µs
to 0.01%		1.4	µs
MATCHING CHARACTERISTICS			
Offset Drift		2	µV/°C
Crosstalk @ f = 1 kHz	R_L = 5 kΩ	–130	dB
f = 100 kHz		–93	dB
INPUT CHARACTERISTICS			
CMRR	V_{CM} = 0 V to 1 V	74	dB
Input Impedance			
Differential		10^{13}‖0.5	Ω‖pF
Common Mode		10^{13}‖2.8	Ω‖pF
OUTPUT CHARACTERISTICS			
Output Saturation Voltage[2]			
V_{OL}–V_{EE}	I_{SINK} = 20 µA	5	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA	10	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA	40	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA	80	mV
V_{OL}–V_{EE}	I_{SINK} = 10 mA	200	mV
V_{CC}–V_{OH}	I_{SOURCE} = 10 mA	500	mV
Capacitive Load Drive		350	pF
POWER SUPPLY			
Quiescent Current		1.24	mA
Power Supply Rejection	V_S+ = 3 V to 15 V	80	dB

NOTES

[1]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($+V_S$ – 1 V) to $+V_S$. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

[2]V_{OL}–V_{EE} is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). V_{CC}–V_{OH} is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Plastic DIP (N) . . . . Observe Derating Curves
  SOIC (R) . . . . Observe Derating Curves
Input Voltage . . . . ($+V_S$ + 0.2 V) to –(20 V + V_S)
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . ±30 V
Storage Temperature Range (N) . . . . –65°C to +125°C
Storage Temperature Range (R, RM) . . . . . –65°C to +150°C
Operating Temperature Range
  AD822A/AD822B . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) . . . . 260°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Lead Plastic DIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 160°C/W
8-Lead MSOP Package: θ_{JA} = 190°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD822 is limited by the associated rise in junction temperature. For plastic packages, the maximum safe junction temperature is 145°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves shown in TPC 24.

While the AD822 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. With power supplies ±12 V (or less) at an ambient temperature of 25°C or less, if the output node is shorted to a supply rail, then the amplifier will not be destroyed, even if this condition persists for an extended period.

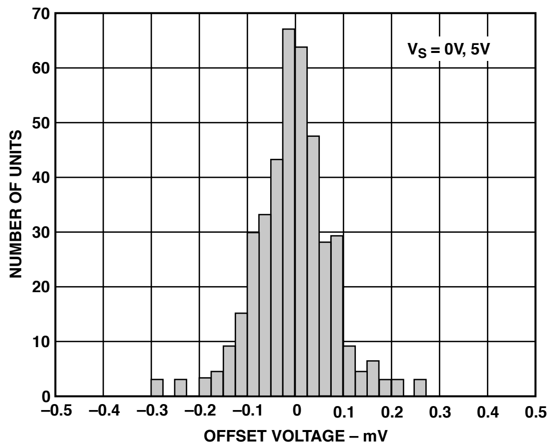
ORDERING GUIDE

Model*	Temperature Range	Package Description	Package Option	Branding Information
AD822AN	–40°C to +85°C	8-Lead PDIP	N-8	
AD822AR	–40°C to +85°C	8-Lead SOIC	R-8	
AD822ARM	–40°C to +85°C	8-Lead MSOP	RM-8	B4A
AD822BR	–40°C to +85°C	8-Lead SOIC	R-8	

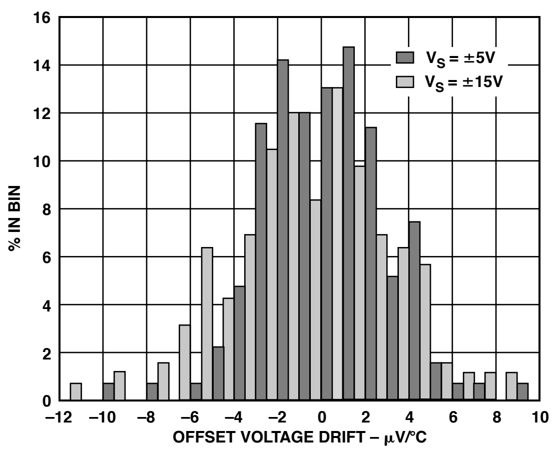
*SPICE model is available at www.analog.com.

CAUTION

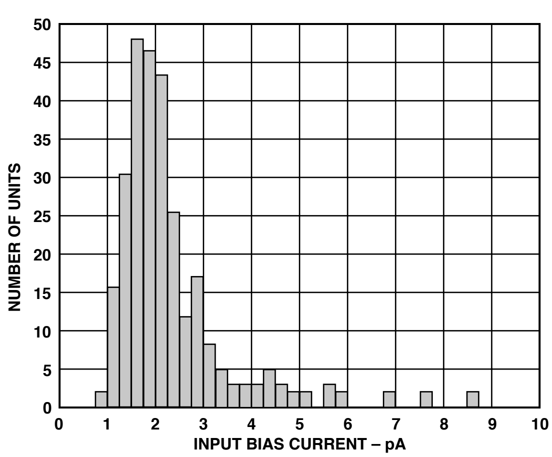
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD822 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



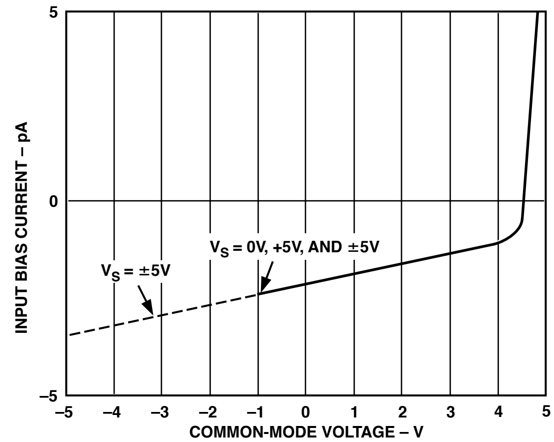
TPC 1. Typical Distribution of Offset Voltage (390 Units)



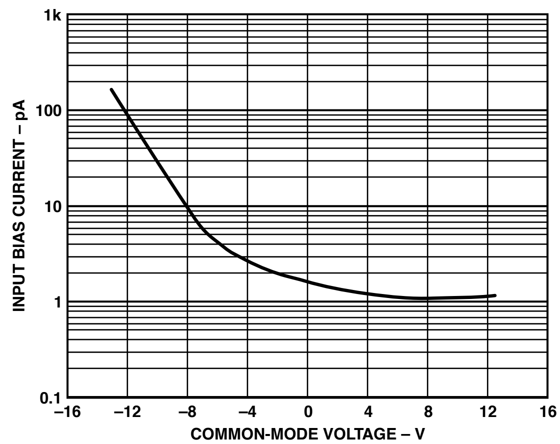
TPC 2. Typical Distribution of Offset Voltage Drift (100 Units)



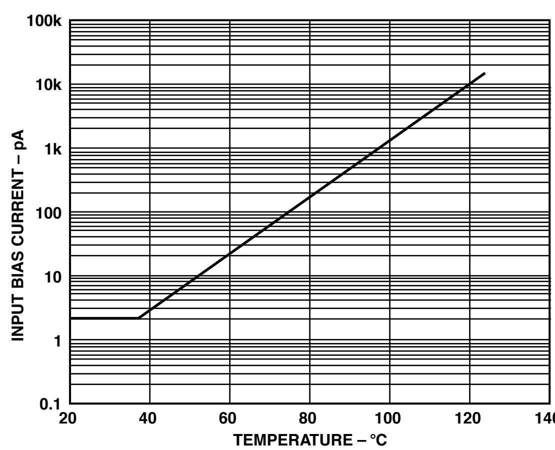
TPC 3. Typical Distribution of Input Bias Current (213 Units)



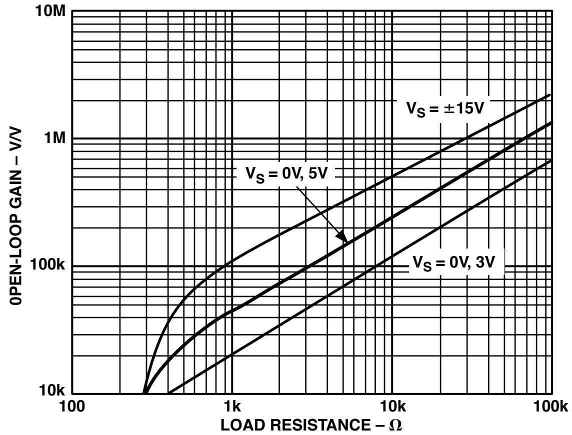
TPC 4. Input Bias Current vs. Common-Mode Voltage; V_S = 5 V, 0 V, and V_S = ±5 V



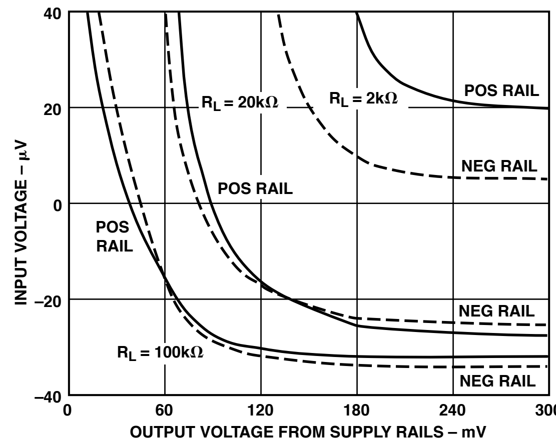
TPC 5. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V



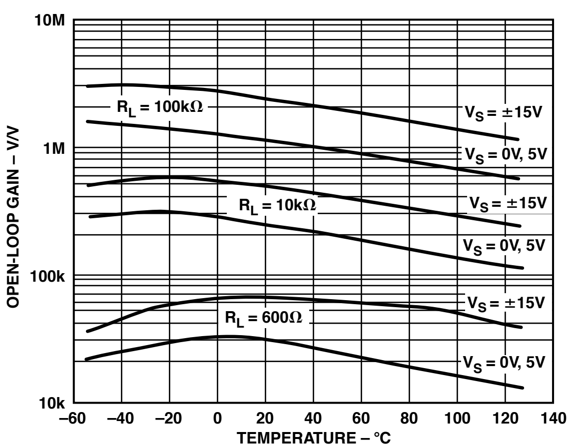
TPC 6. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0



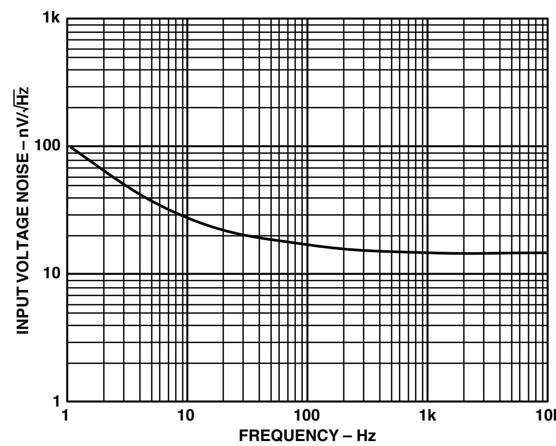
TPC 7. Open-Loop Gain vs. Load Resistance



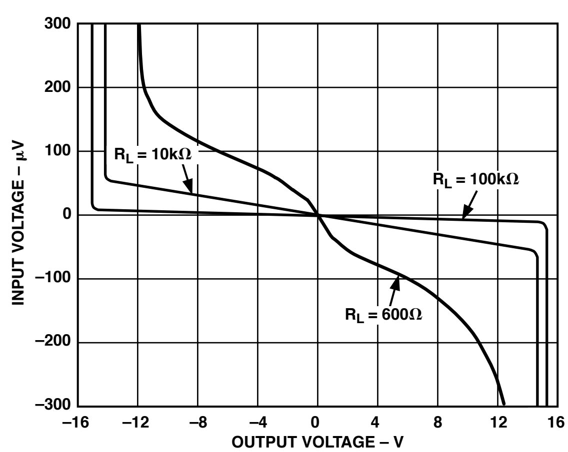
TPC 10. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; $V_S = \pm5$ V



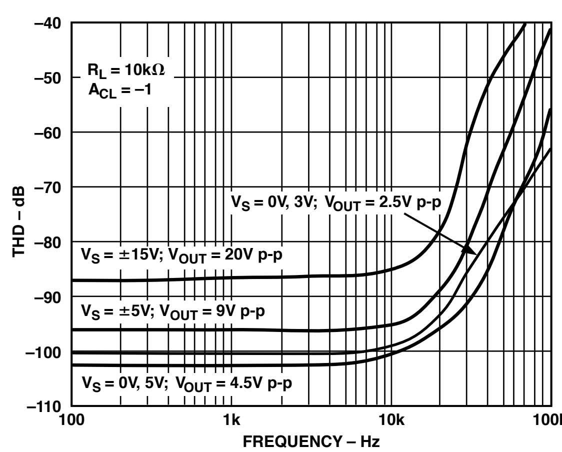
TPC 8. Open-Loop Gain vs. Temperature



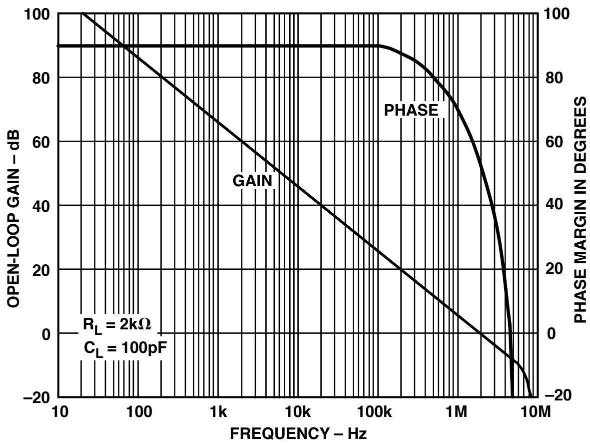
TPC 11. Input Voltage Noise vs. Frequency



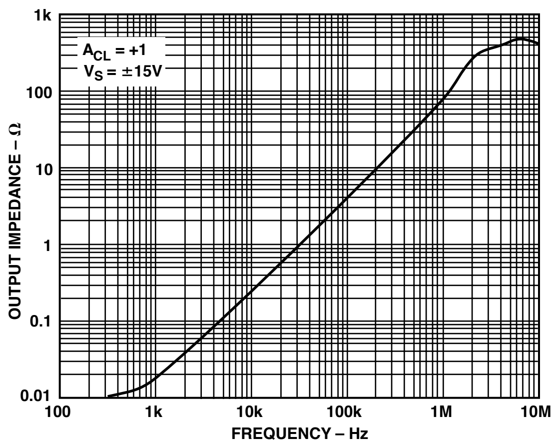
TPC 9. Input Error Voltage vs. Output Voltage for Resistive Loads



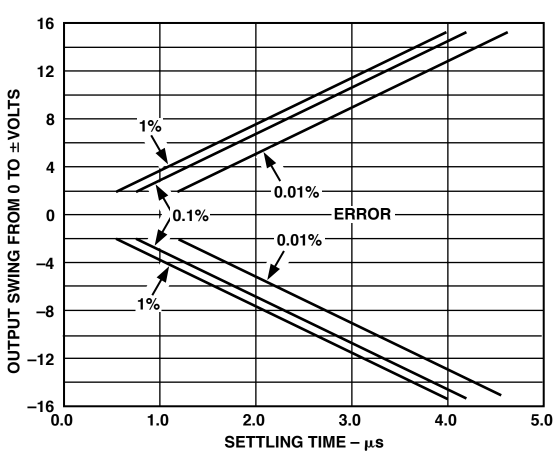
TPC 12. Total Harmonic Distortion vs. Frequency



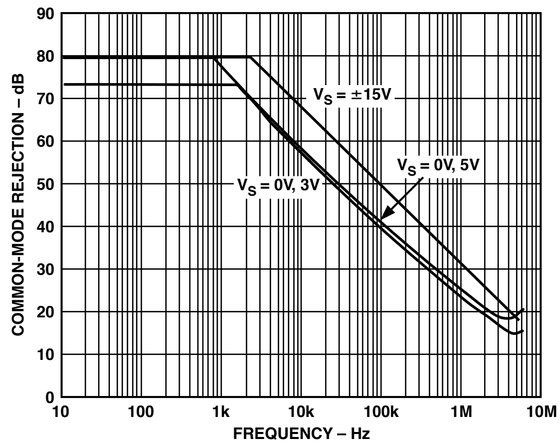
TPC 13. Open-Loop Gain and Phase Margin vs. Frequency



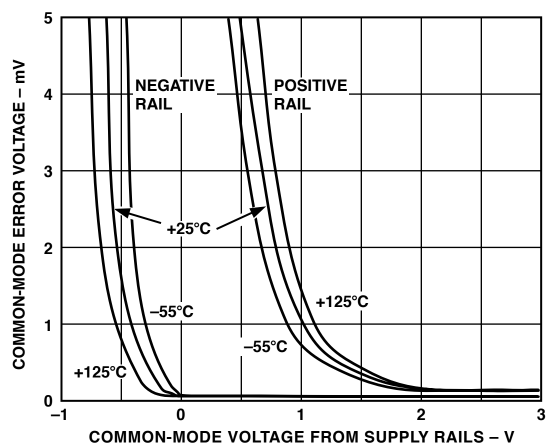
TPC 14. Output Impedance vs. Frequency



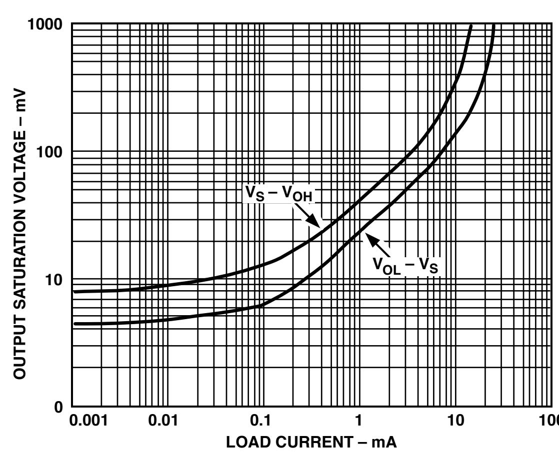
TPC 15. Output Swing and Error vs. Settling Time



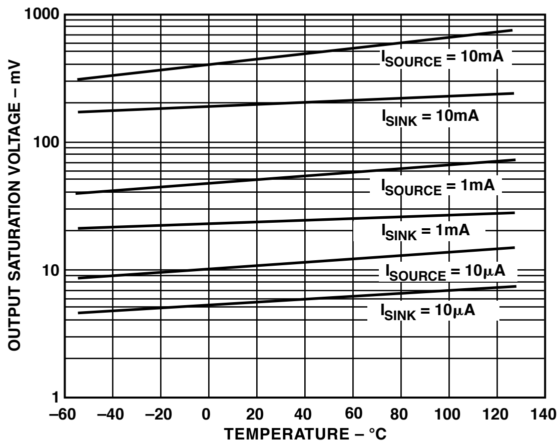
TPC 16. Common-Mode Rejection vs. Frequency



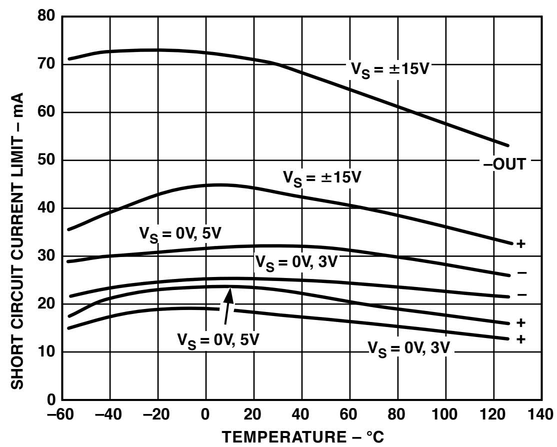
TPC 17. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S – V_{CM}$)



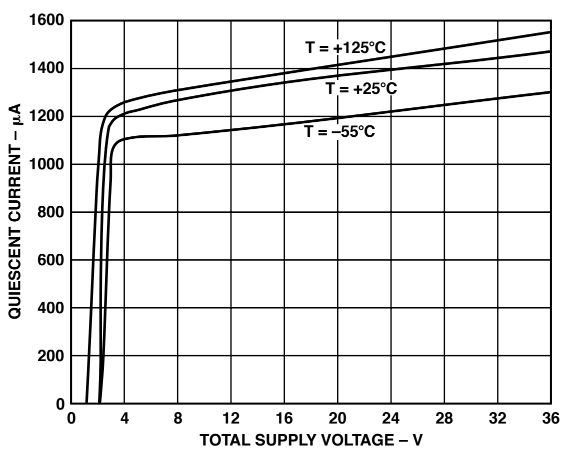
TPC 18. Output Saturation Voltage vs. Load Current



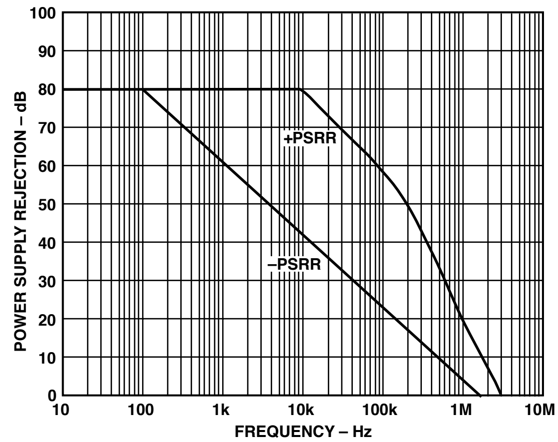
TPC 19. Output Saturation Voltage vs. Temperature



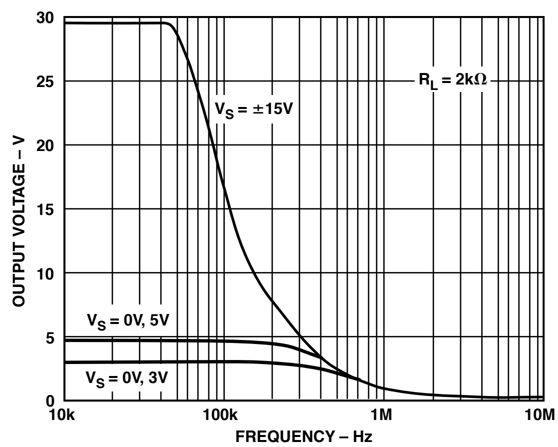
TPC 20. Short Circuit Current Limit vs. Temperature



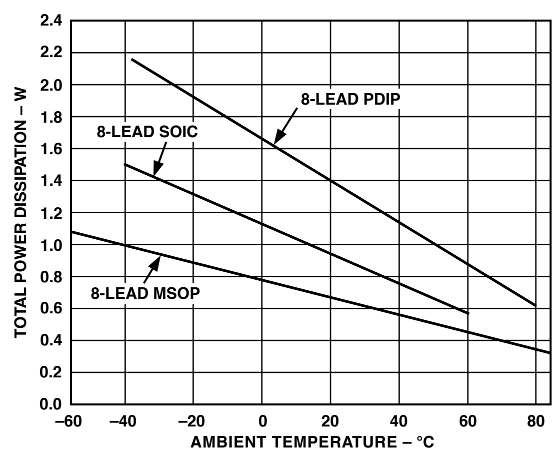
TPC 21. Quiescent Current vs. Supply Voltage vs. Temperature



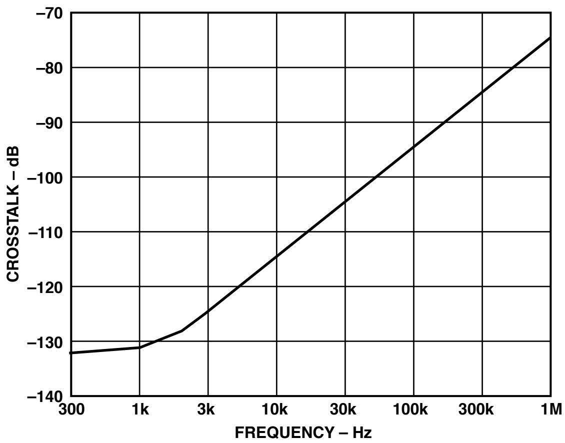
TPC 22. Power Supply Rejection vs. Frequency



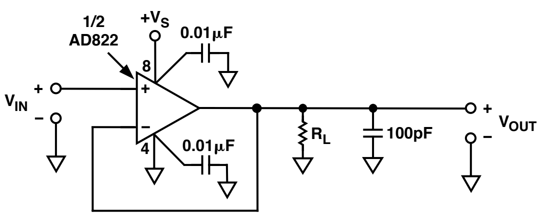
TPC 23. Large Signal Frequency Response



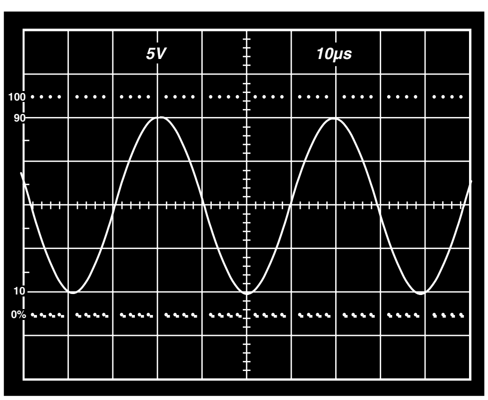
TPC 24. Maximum Power Dissipation vs. Temperature for Plastic Packages



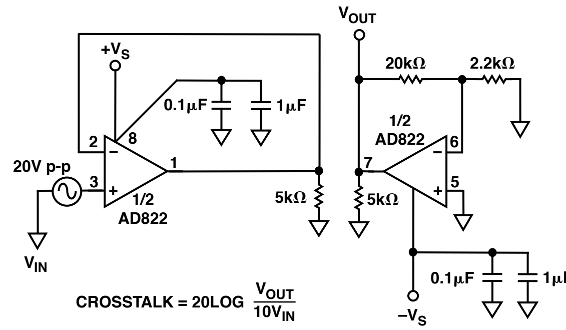
TPC 25. Crosstalk vs. Frequency



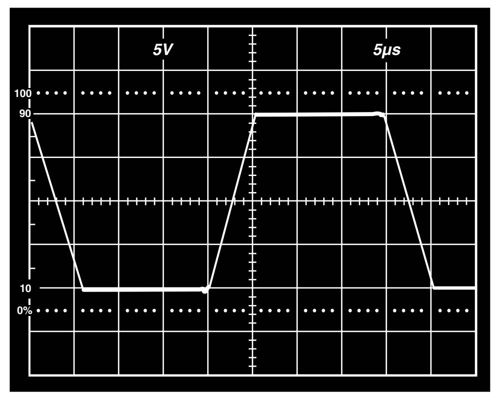
TPC 26. Unity Gain Follower



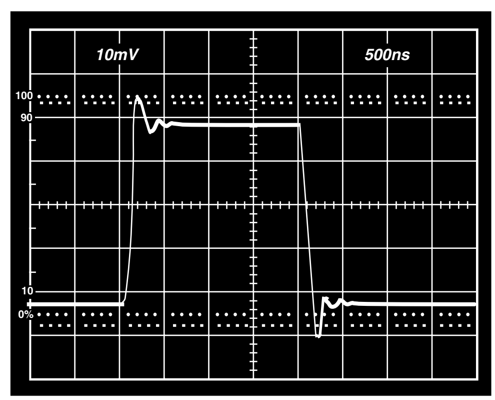
TPC 27. 20 V p-p, 25 kHz Sine Wave Input; Unity Gain Follower; R_L = 600 Ω, V_S = ±15 V



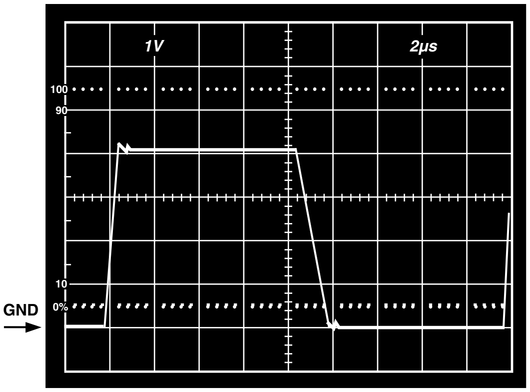
TPC 28. Crosstalk Test Circuit



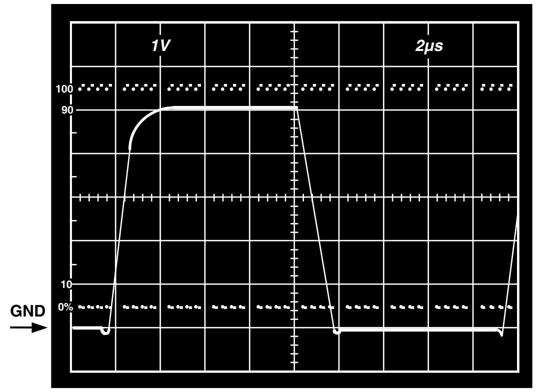
TPC 29. Large Signal Response Unity Gain Follower; V_S = ±15 V, R_L = 10 kΩ



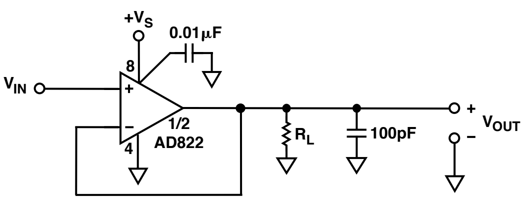
TPC 30. Small Signal Response Unity Gain Follower; V_S = ±15 V, R_L = 10 kΩ



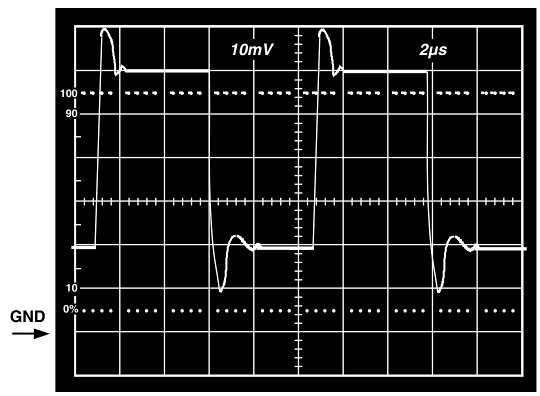
TPC 31. V_S = 5 V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step



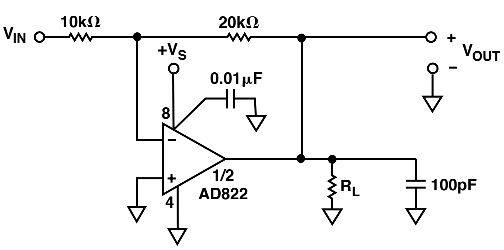
TPC 34. V_S = 5 V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step



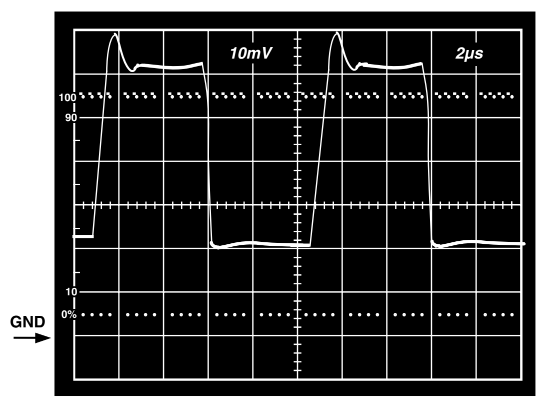
TPC 32. Unity Gain Follower



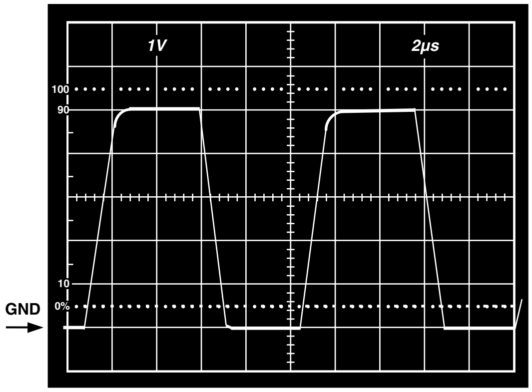
TPC 35. V_S = 5 V, 0 V; Unity Gain Follower Response, to 40 mV Step Centered 40 mV above Ground, R_L = 10 kΩ



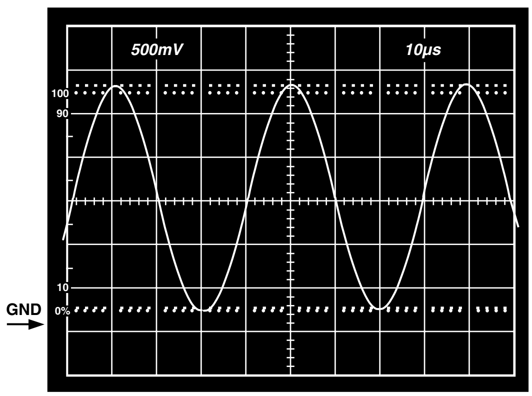
TPC 33. Gain-of-T2 Inverter



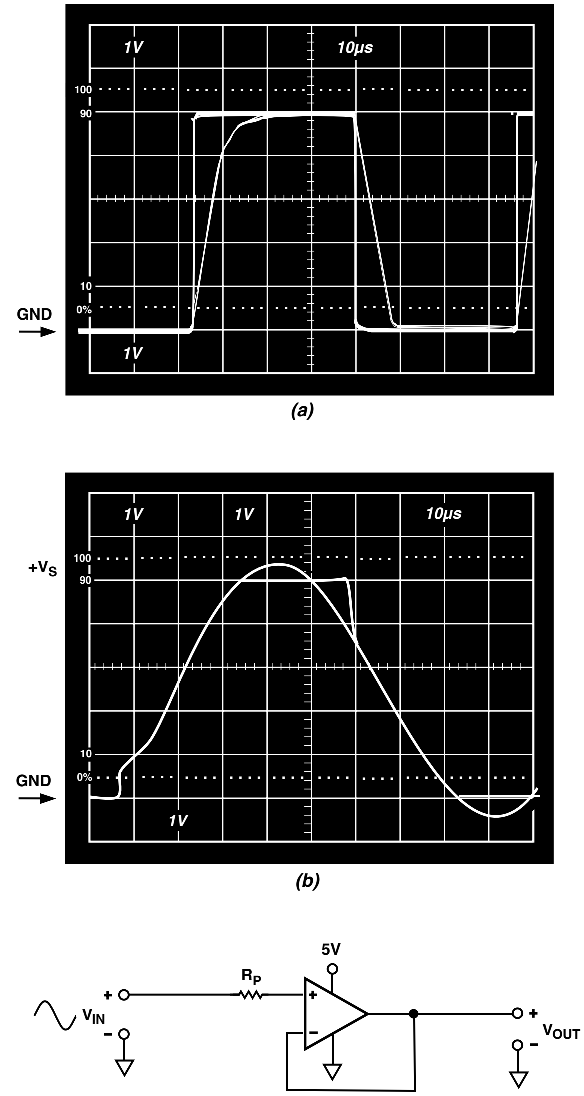
TPC 36. V_S = 5 V, 0 V; Gain-of-2 Inverter Response to 20 mV Step, Centered 20 mV below Ground, R_L = 10 kΩ



TPC 37. V_S = 5 V, 0 V; Gain-of-2 Inverter Response to 2.5 V Step Centered –1.25 V below Ground, R_L = 10 kΩ



TPC 38. V_S = 3 V, 0 V; Gain-of-2 Inverter, V_{IN} = 1.25 V, 25 kHz, Sine Wave Centered at –0.75 V, R_L = 600 Ω



TPC 39. (a) Response with R_P = 0; V_{IN} from 0 to $+V_S$
(b) V_{IN} = 0 to $+V_S$ + 200 mV
V_{OUT} = 0 to $+V_S$
R_P = 49.9 kΩ

APPLICATION NOTES

Input Characteristics

In the AD822, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $–V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in TPCs 31 and 34) and increased common-mode voltage error as illustrated in TPC 17.

The AD822 does not exhibit phase reversal for input voltages up to and including $+V_S$. TPC 39a shows the response of an AD822 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output waveform. For input voltages greater than $+V_S$, a resistor in series with the AD822's noninverting input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in TPC 39b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S$ – 0.4 V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in TPC 4.

A current limiting resistor should be used in series with the input of the AD822 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD822 when $\pm V_S$ = 0. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below the negative supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 V. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD822 is designed for 13 nV/$\sqrt{Hz}$ wideband input voltage noise and maintains low noise performance to low frequencies (refer to TPC 11). This noise performance, along with the AD822's low input current and current noise, means that the AD822 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 3.

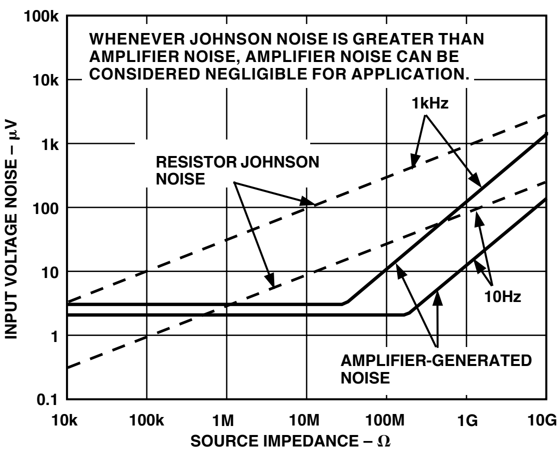


Figure 3. Total Noise vs. Source Impedance

Output Characteristics

The AD822's unique bipolar rail-to-rail output stage swings within 5 mV of the negative supply and 10 mV of the positive supply with no external resistive load. The AD822's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV; when sinking 5 mA, the saturation voltage to the negative rail will be 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in TPCs 7 to 10. For load resistances over 20 kΩ, the AD822's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD822's output is overdriven so as to saturate either of the output devices, the amplifier will recover within 2 µs of its input returning to the amplifier's linear operating region.

Direct capacitive loads will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 4 shows the AD822's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects.

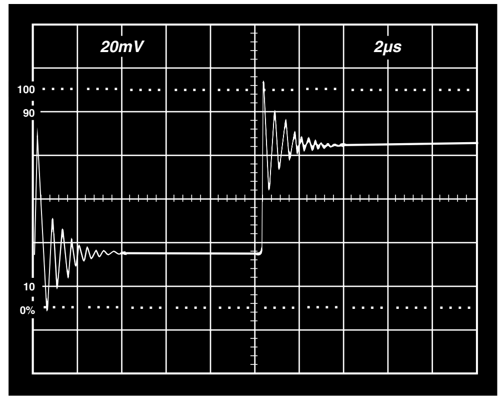


Figure 4. Small Signal Response of AD822 as Unity Gain Follower Driving 350 pF

Figure 5 is a plot of capacitive load that will result in a 20° phase margin versus noise gain for the AD822. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

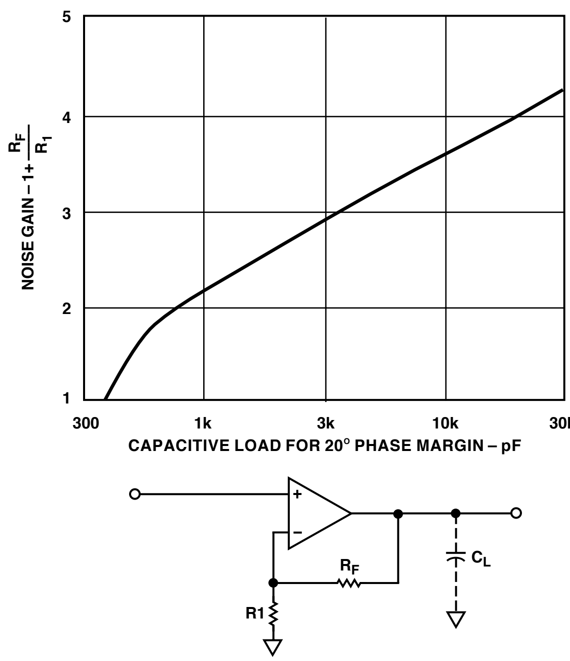


Figure 5. Capacitive Load Tolerance vs. Noise Gain

Figure 6 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

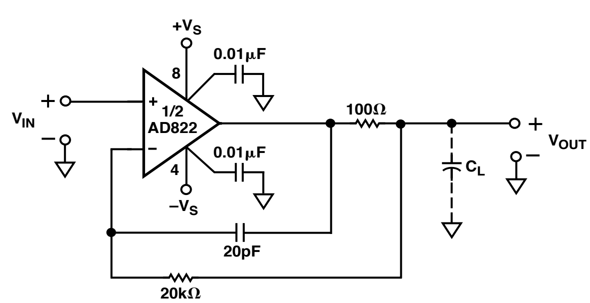


Figure 6. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

APPLICATIONS

Single-Supply Voltage-to-Frequency Converter

The circuit shown in Figure 7 uses the AD822 to drive a low power timer that produces a stable pulse of width t_1. The positive going output pulse is integrated by R1–C1 and used as one input to the AD822 that is connected as a differential integrator. The other input (nonloading) is the unknown voltage, V_{IN}. The AD822 output drives the timer trigger input, closing the overall feedback loop.

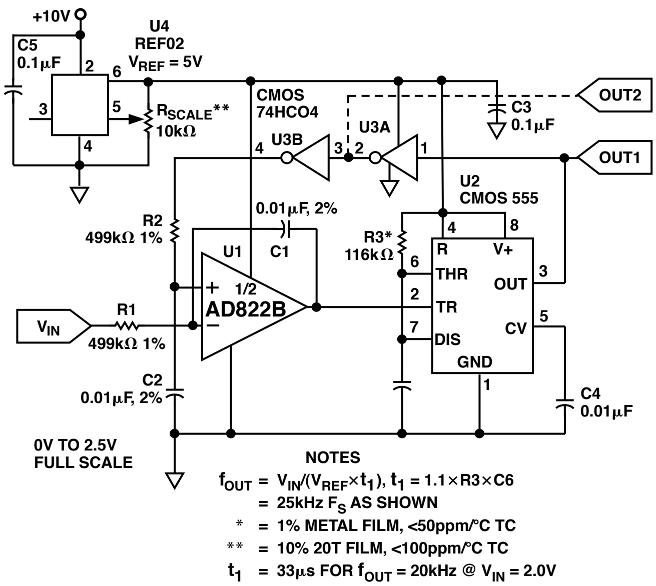


Figure 7. Single-Supply Voltage-to-Frequency Converter

Typical AD822 bias currents of 2 pA allow megohm-range source impedances with negligible dc errors. Linearity errors on the order of 0.01% full scale can be achieved with this circuit. This performance is obtained with a 5 V single supply that delivers less than 1 mA to the entire circuit.

Single-Supply Programmable Gain Instrumentation Amplifier

The AD822 can be configured as a single-supply instrumentation amplifier that is able to operate from single supplies down to 3 V or dual supplies up to ±15 V. Using only one AD822 rather than three separate op amps, this circuit is cost and power efficient. AD822 FET inputs' 2 pA bias currents minimize offset errors caused by high unbalanced source impedances.

An array of precision thin-film resistors sets the in amp gain to be either 10 or 100. These resistors are laser trimmed to ratio match to 0.01% and have a maximum differential TC of 5 ppm/°C.

Table I. In Amp Performance

Parameters	V_S = 3 V, 0 V	V_S = 65 V
CMRR 74 dB	80 dB	
Common-Mode Voltage Range	–0.2 V to +2 V	–5.2 V to +4 V
3 dB BW, G = 10	180 kHz	180 kHz
G = 100	18 kHz	18 kHz
$t_{SETTLING}$		
2 V Step (V_S = 0 V, 3 V)	2 µs	
5 V (V_S = ±5 V)		5 µs
Noise @ f = 1 kHz, G = 10	270 nV/√Hz	270 nV/√Hz
G = 100	2.2 µV/√Hz	2.2 µV/√Hz
I_{SUPPLY} (Total) 1.10 mA	1.15 mA	

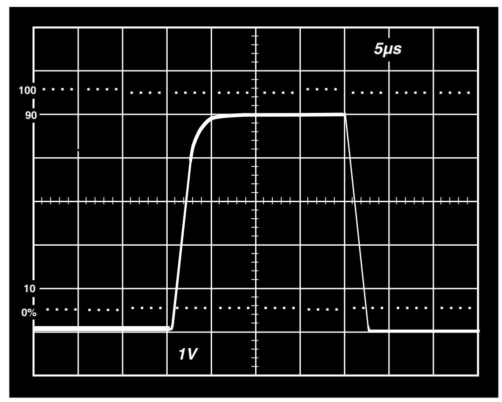


Figure 8a. Pulse Response of In Amp to a 500 mV p-p Input Signal; V_S = 5 V, 0 V; Gain = 10

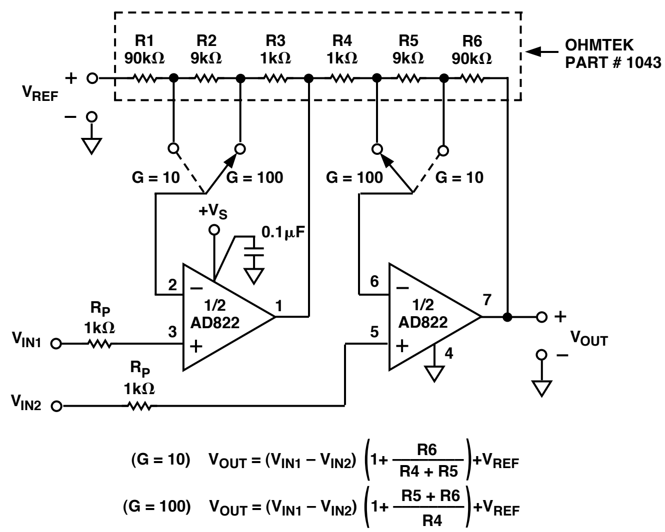


Figure 8b. A Single-Supply Programmable Instrumentation Amplifier

3 V, Single-Supply Stereo Headphone Driver

The AD822 exhibits good current drive and THD + N performance, even at 3 V single supplies. At 1 kHz, total harmonic distortion plus noise (THD + N) equals –62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single-supply op amps that consume more power and cannot run on 3 V power supplies.

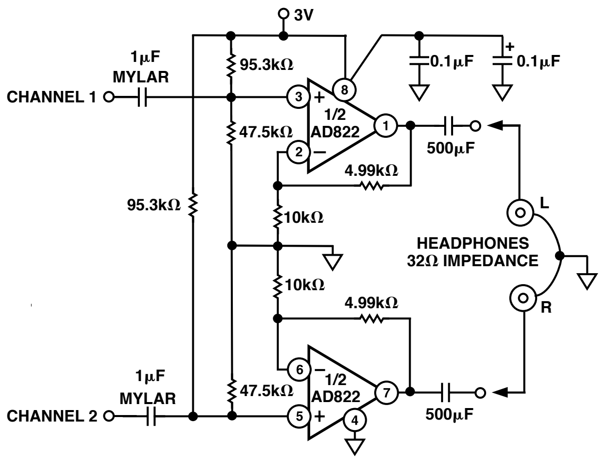


Figure 9. 3 V Single-Supply Stereo Headphone Driver

In Figure 9, each channel's input signal is coupled via a 1 µF Mylar capacitor. Resistor dividers set the dc voltage at the noninverting inputs so that the output voltage is midway between the power supplies (1.5 V). The gain is 1.5. Each half of the AD822 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 µF capacitors and the headphones that can be modeled as 32 Ω load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz to 20 kHz) are delivered to the headphones.

Low Dropout Bipolar Bridge Driver

The AD822 can be used for driving a 350 Ω Wheatstone bridge. Figure 10 shows one half of the AD822 being used to buffer the AD589—a 1.235 V low power reference. The output of 4.5 V can be used to drive an A/D converter front end. The other half of the AD822 is configured as a unity gain inverter and generates the other bridge input of –4.5 V. Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor RG and determined by:

$$G = \frac{49.4k\Omega}{R_G} + 1$$

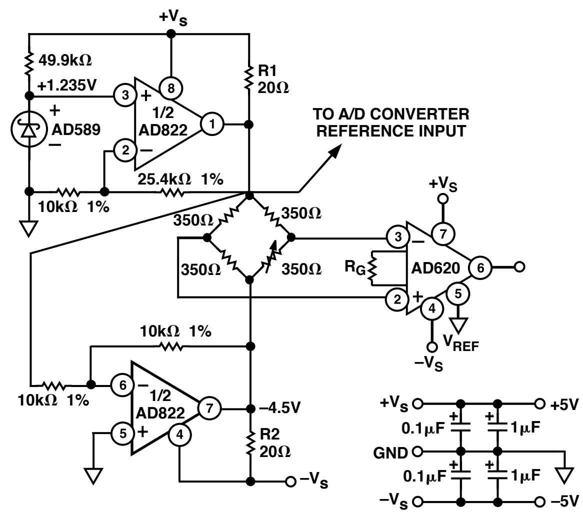
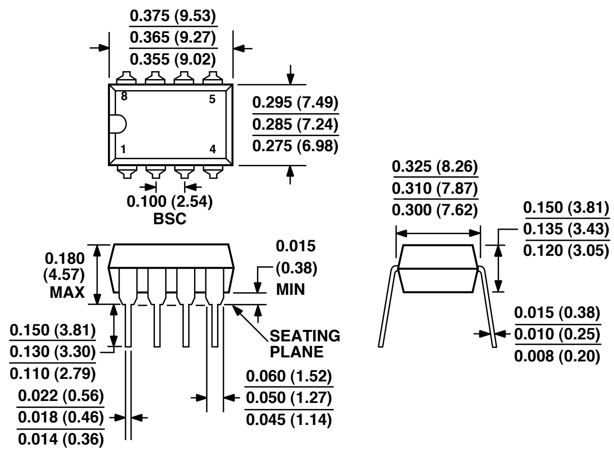


Figure 10. Low Dropout Bipolar Bridge Driver

OUTLINE DIMENSIONS

8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)

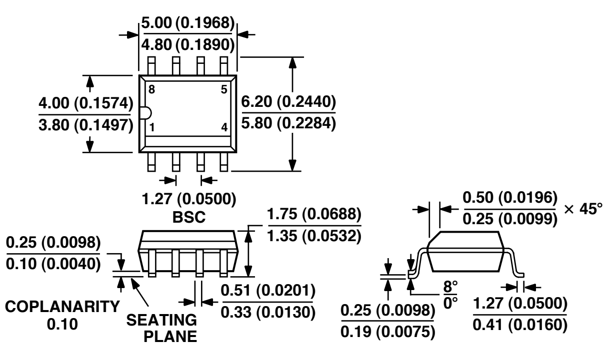
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

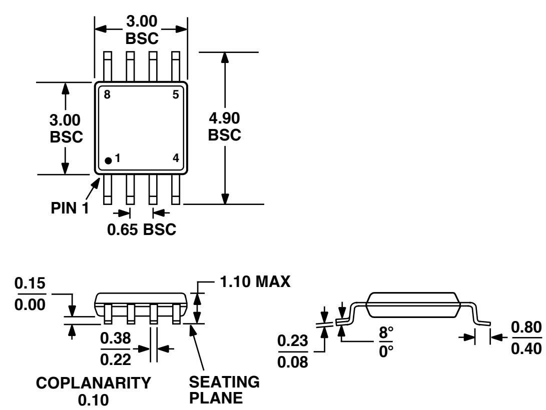
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead microSOIC Package [MSOP]
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

Revision History

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