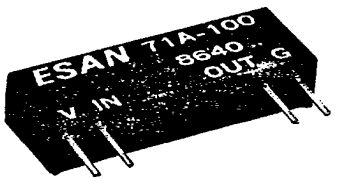
Active Delay Line (TTL Interface)

71A Series

- **Single Output**
- **8 Pin Sip Package**
- **TTL Compatible**



Specifications:

- Delay tolerance : ±5% or 2ns whichever is greater
- Rise time : 4ns max.
- Temp. coefficient : 100 ppm/°C
- Operating Temp. Range : −0°C to 70°C
- Minimum Pulse Width : 40% of total delay
- Supply Voltage : 5VDC ±5%
- Logic 1 Input current : 50 UA max.
- Logic 0 Input current : −2 mA max.
- Logic 1 Output : 2.75V min.
- Logic 0 Output : 0.4V max.
- Logic 1 Fan out : 20/TAP max.
- Logic 0 Fan out : 10/TAP max.
- Power Dissipation : 375 mW max.

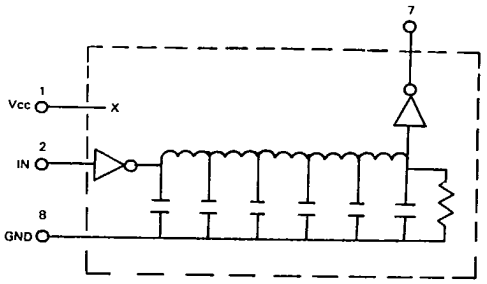
Test Conditions:

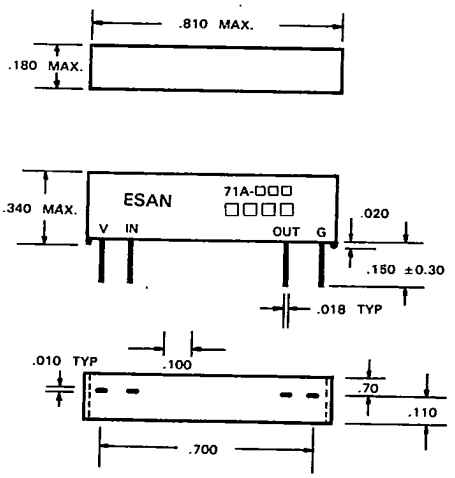
- Input pulse voltage : 3.2V
- Input pulse width : 1.2 * total delay
- Input pulse spacing : 2 * total delay
- Input pulse rise time: : 2 ns
- Rise time : 0.75V to 2.4V
- Time delay measured : @1.5V level
- All measurement : @Vcc = 5.0V, TA = 25°C

Features:

- Schottky TTL interface
- Low power schottky available named "71AL- xxx" series
- Both Leading and Trailing edge available under request named "71B- xxx" series

PART NO.	DELAY TIME (ns)
71A-025	25
71A-050	50
71A-075	75
71A-100	100
71A-125	125
71A-150	150
71A-200	200
71A-250	250
71A-300	300
71A-400	400
71A-500	500





Unit: Inch

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