CYPRESS SEMICONDUCTOR

Reprogrammable 16K x 16 Registered PROM

Features

- 0.8-micron CMOS for optimum speed/power
- High speed
  - 25 ns max set-up
  - 25 ns clock to output
- 16-bit-wide words
- Registered outputs
- Programmable synchronous or asynchronous output enable
- Initialization capability
  - Separate control pin ($\overline{INIT}$)
  - Programmable initialization word
- 40-pin, 600-mil-wide DIP packages
- 44-pin PLCC and 44-pin LCC packages
- 100% reprogrammable in windowed packages
- TTL-compatible I/O
- Capable of withstanding greater than 2001V static discharge

Functional Description

The CY7C272 is a high-performance 16K-word by 16-bit CMOS PROM with output registers. It is available in 40-pin, 600-mil-wide DIP packages and 44-pin PLCC and LCC packages. The 7C272 is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating gate technology and word-wide programming algorithms. The CY7C272 is a plug-in replacement for EPROM devices.

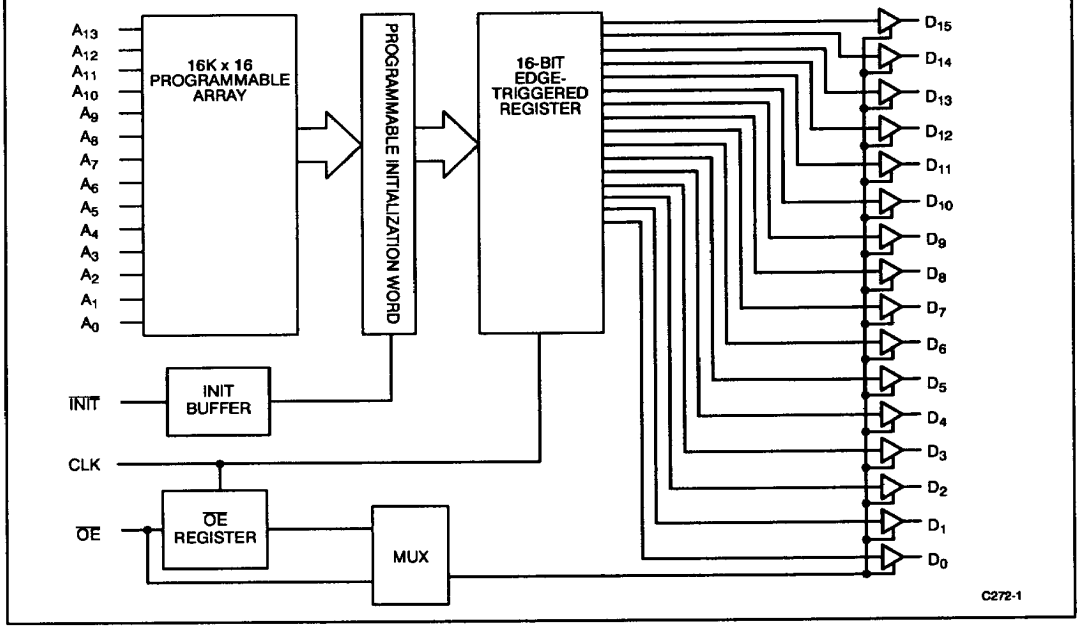
The CY7C272 features a programmable synchronous or asynchronous output enable and a programmable initialization word.

In order to read the CY7C272, an address is placed on the address lines ($A_{13} - A_0$). The data stored at the array location addressed by the address lines is placed in the output registers at the rising edge of CLK. The data will remain on the outputs until the following rising edge of CLK.

If asynchronous output enable is being used, the outputs will enter the active state whenever a LOW is placed on $\overline{OE}$. If a HIGH is placed on $\overline{OE}$, the outputs will be tri-stated. If the synchronous output enable is being used, the outputs will enter the active state following the first rising edge of CLK after a LOW is placed on $\overline{OE}$. The outputs will be three-stated following the first rising edge of CLK after a HIGH is placed on $\overline{OE}$.

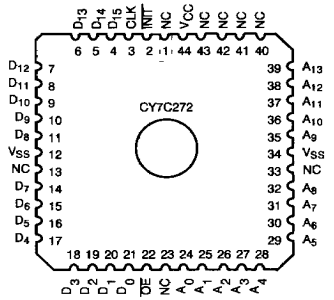
An initialization control input ($\overline{INIT}$) is provided. Applying a LOW to $\overline{INIT}$ causes an immediate load of the programmable initialize word into the output registers and onto the outputs. The output enable must be active when reading the initialization word. The $\overline{INIT}$ LOW disables CLK and must return HIGH to reenable CLK.

Logic Block Diagram



Pin Configurations

LCC/PLCC (Opaque Only)



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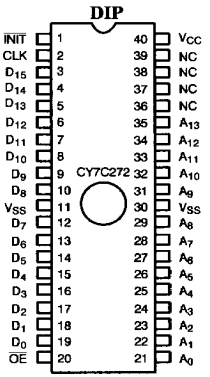
DIP



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Selection Guide

		CY7C272–25	CY7C272–30
Maximum Set-Up Time (ns)		25	30
Maximum Clock to Output (ns)		25	30
Maximum Operating Current (mA)	Commercial	200	200
	Military		250

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	– 40°C to +85°C	5V ±10%
Military[2]	– 55°C to +125°C	5V ±10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature

Electrical Characteristics[3,4]

Parameter	Description	Test Conditions		CY7C272–25 Min.	CY7C272–25 Max.	CY7C272–30 Min.	CY7C272–30 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA (6.0 mA Mil)			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs.		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs.		– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	– 10	+10	μA
V_{CD}	Input Clamp Diode Voltage			Note 3				
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		– 40	+40	– 40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[5]		– 20	– 90	– 20	– 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0.0 mA	Com'l		200		200	mA
			Mil				250	mA

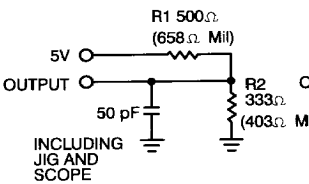
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

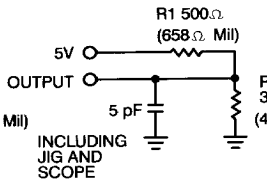
Notes:

3. See Introduction to CMOS PROMs in this Data Book for general information on testing.
4. See the last page of this specification for Group A subgroup testing information.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms



(a)



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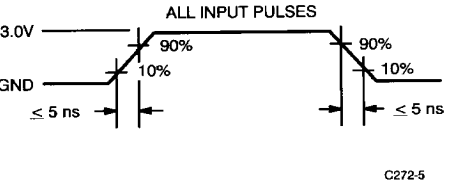
(b) High Z Load



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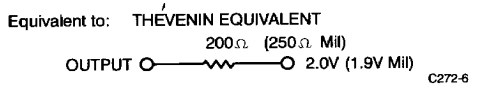

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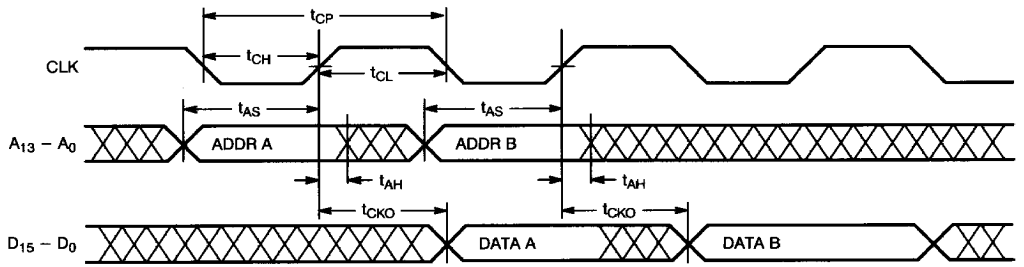
Switching Characteristics Over the Operating Range[3,4]

Parameters	Description	CY7C272–25		CY7C272–30		Units
		Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	25		30		ns
t_{CH}	Clock HIGH Pulse Width	$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		ns
t_{CL}	Clock LOW Pulse Width	$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		ns
t_{AS}	Address Valid to CLK Rise	25		30		ns
t_{AH}	Address Hold from CLK Rise	0		0		ns
t_{CKO}	Clock Rise to Output Data		25		30	ns
t_{OES}	$\overline{OE}$ Set-Up to CLK Rise	20		25		ns
t_{OEH}	$\overline{OE}$ Hold from CLK Rise	10		15		ns
t_{COV}	Clock Rise to Output Valid		25		30	ns
t_{COZ}	Clock Rise to High Z Output		25		30	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		25		30	ns
t_{OEZ}	$\overline{OE}$ HIGH to High Z Output		25		30	ns
t_{IW}	$\overline{INIT}$ Pulse Width	15		18		ns
t_{IDV}	$\overline{INIT}$ LOW to Data Valid		30		35	ns
t_{ICR}	$\overline{INIT}$ Recovery to CLK	15		18		ns

Switching Waveforms

Read Operation Timing Diagram[6]



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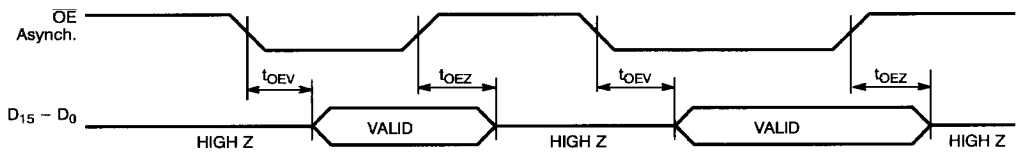
Asynchronous Output Enable



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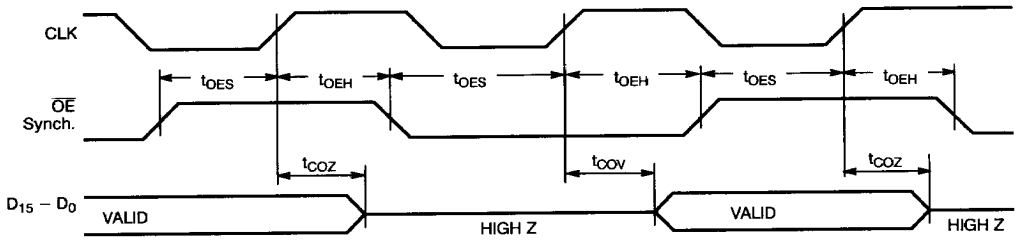
Notes:
6. $\overline{OE}$ assumed active

Switching Waveforms (continued)

Synchronous Output Enable



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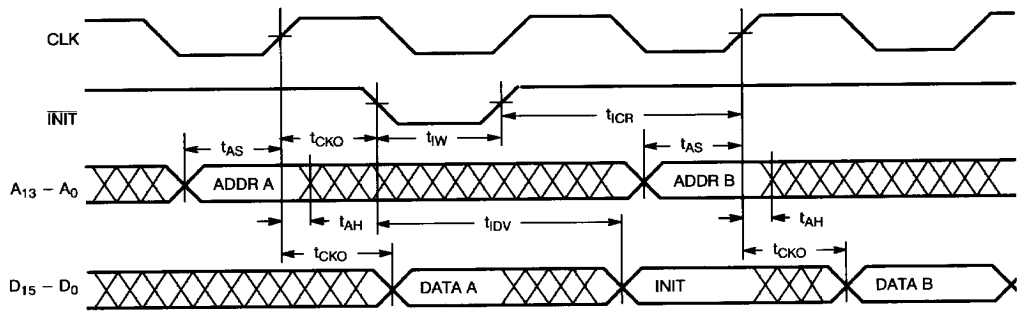
Asynchronous Initialization Timing Diagram[6]



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Architecture Configuration Bits

The CY7C272 has two user-programmable options in addition to the reprogrammable data array. For detailed programming information, contact your local Cypress representative.

The first programmable option determines the operation of the output enable. When this control bit is programmed with a 0, the output enable operates asynchronously. When this control bit is programmed with a 1, the output enable operates synchronously. The initialization word is also user-programmable.

Control Option	Control Word		Function
	Bit	Programmed Level	
OS	D_0	0	$\overline{OE}$ Asynchronous
		1	$\overline{OE}$ Synchronous

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
.	.
3FFF	Data
4000	Control Word
4001	Initialization Word

Control Word (4000H)

D_{15} D_0

XXXXXXXXXXXXXXXOS

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C272 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C272 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Program Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	$D_0 - D_{15}$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	High Z
Program Enable	V_{PP}	V_{ILP}	V_{IHP}	Data
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	Data

Table 2. Signature Mode Table

Signature Mode	A_0	A_9	$D_0 - D_{15}$
Cypress Code	V_{ILP}	V_{PP}	0034 (hex)
Device Code	V_{IHP}	V_{PP}	0016 (hex)

Table 3. Configuration Mode Table[7]

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_2	A_4	$D_0 - D_{15}$
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	X	X	High Z
Program Control Word	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Control Word
Verify Control Word	V_{PP}	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Control Word
Program Init Word	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	Init Word
Verify Init Word	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	Init Word

Notes:
7. X = "don't care" but not to exceed V_{CC} ±5%.

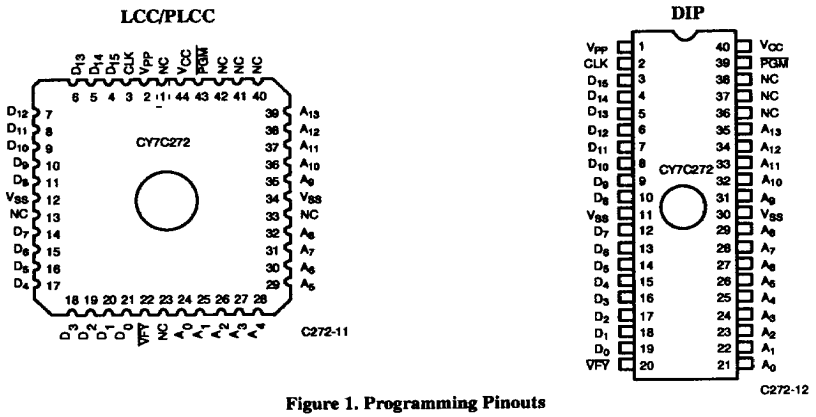

Figure 1. Programming Pinouts

Ordering Information[8]

Speed (ns)		Ordering Code	Package Type	Operating Range
t_{AS}	t_{CKO}			
25	25	CY7C272–25DC	D18	Commercial
		CY7C272–25HC	H67	
		CY7C272–25JC	J67	
		CY7C272–25PC	P17	
		CY7C272–25WC	W18	
30	30	CY7C272–30DC	D18	Commercial
		CY7C272–30HC	H67	
		CY7C272–30JC	J67	
		CY7C272–30PC	P17	
		CY7C272–30WC	W18	
		CY7C272–30DMB	D18	Military
		CY7C272–30HMB	H67	
		CY7C272–30LMB	L67	
		CY7C272–30QMB	Q67	
		CY7C272–30WMB	W18	

Notes:
8. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{CKO}	7, 8, 9, 10, 11
t_{OES}	7, 8, 9, 10, 11
t_{OEH}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{IW}	7, 8, 9, 10, 11
t_{IDV}	7, 8, 9, 10, 11
t_{ICR}	7, 8, 9, 10, 11

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