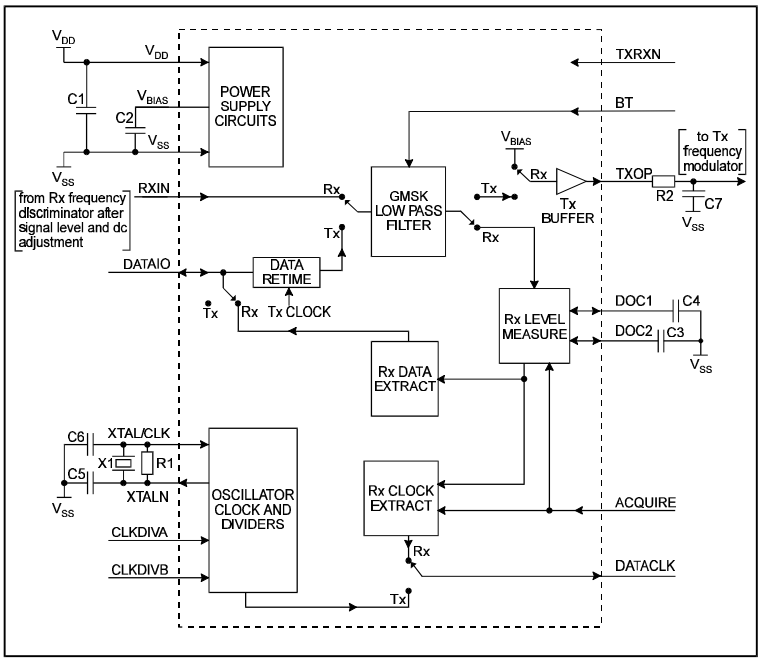
CML Semiconductor Products

Half Duplex GMSK Modem FX579

D/579/4 Sept 1995
Provisional Issue

1.0 Features

- **Half Duplex GMSK Modem for FM Radio Data Links**
- **Acquire Pin to assist with the acquisition of Rx Data signals**
- **Pin-Programmable Rx/Tx Data Rates:**
  4k to 20 kbits/sec at V_{DD} = 3.0V
  4k to 40 kbits/sec at V_{DD} = 5.0V
- **Serial Data Interface with Rx/Tx Data Clock**
- **Low Operating Power:**
  < 2mA at 3.0V, < 4mA at 5.0V
  Non-DSP solution
- **Telemetry, Wireless Alarms, PC, Laptop and Printer Comms, WAN and LAN and General Purpose Data Applications**
- **16-Pin Package with few External Components**
- **Low Cost**



1.1 Brief Description

The FX579 is a single chip, low cost, low current integrated circuit that performs the baseband functions of a half duplex GMSK modem and is intended for use in FM radio data links. This general purpose modem is suitable for data rates in the region of 4 to 40 kbits/sec, at a BT of 0.3 or 0.5.

The Tx and Rx data lines share a common pin and data is synchronised to a Tx/Rx data clock generated by the modem. A single ACQUIRE line is provided to assist with acquisition of Rx data signals.

CONTENTS

1.2 Block Diagram

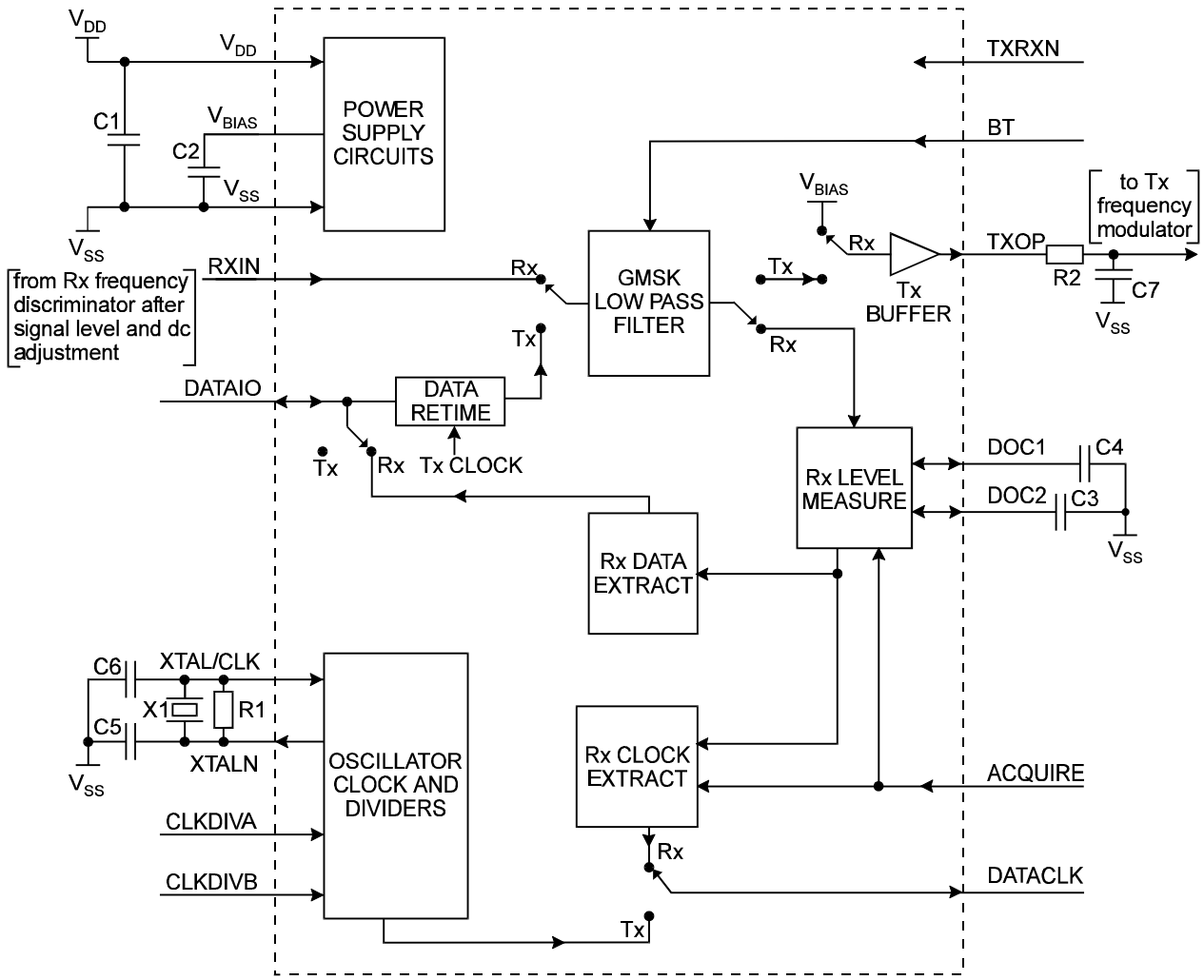


Figure 1 Block Diagram

1.3 Signal List

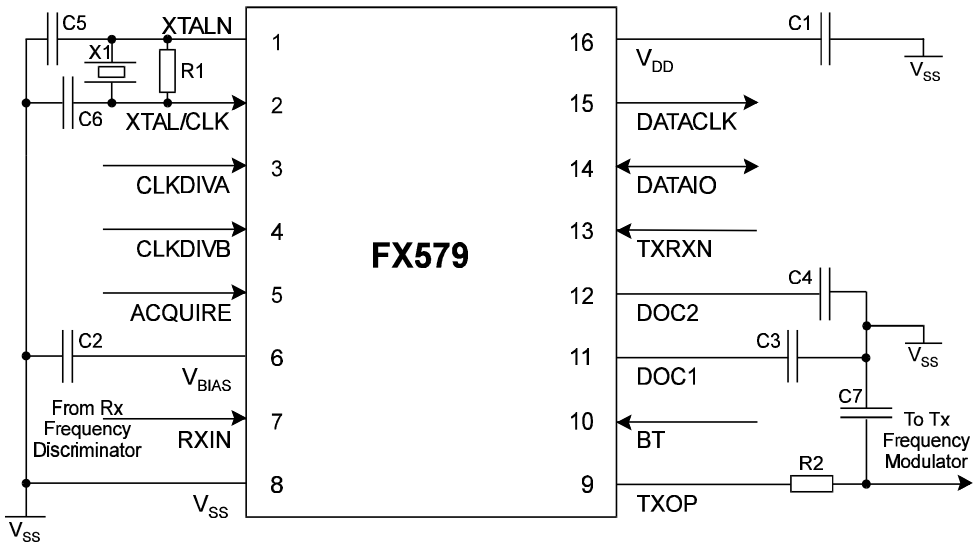
Package D4	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The output of the on-chip oscillator.
2	XTAL/CLK	I/P	The input to the on-chip oscillator for an external Xtal circuit or clock.
3	CLKDIVA	I/P	) Two logic level inputs that control the internal) clock divider and hence the transmit and) receive data rate (See Table 1).
4	CLKDIVB	I/P	
5	ACQUIRE	I/P	A logic "1" applied to this input will set the Rx level measurement and Rx clock extraction circuitry to 'acquire' mode.
6	V_{BIAS}	O/P	The internal circuitry bias line, held at ½ V_{DD}, this pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
7	RXIN	I/P	The Rx signal input from the radio's discriminator via suitable signal and dc level adjustment. In Rx this pin is internally held at ½ V_{DD}.
8	V_{SS}	Power	Negative supply rail. Signal ground.
9	TXOP	O/P	The Tx signal output. This signal should be applied to an external RC before being applied to the radio modulator.
10	BT	I/P	A logic level input to select the modem 'BT' (the ratio of the Tx filter -3dB frequency to the bit rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3.
11	DOC1	O/P	Two pins used by the modem's Rx level measurement circuitry. A capacitor should be connected from each pin to V_{SS}.
12	DOC2	O/P	
13	TXRXN	I/P	A logic level applied to this pin determines whether the modem operates in Tx or Rx mode. A logic "1" sets Tx mode. A logic "0" sets Rx mode.

Package D4	Signal		Description
Pin No.	**Name**	**Type**	
14	DATAIO	BI	A bidirectional pin that is used for inputting Tx data or outputting Rx data.
15	DATACLK	O/P	This pin outputs either the Tx DATACLK in Tx mode or the Rx DATACLK in Rx mode.
16	V_{DD}	Power	Positive supply rail. A single stable power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

Notes:

I/P = Input
O/P = Output
BI = Bidirectional

1.4 External Components



External Components

Component	Value	Tolerance	Component	Value	Tolerance
R1	1MΩ	±10%	C3	Note 2	±20%
R2	Note 1	± 5%	C4	Note 2	±20%
X1	Note 3		C5	Note 3	
C1	100nF	±20%	C6	Note 3	
C2	100nF	±20%	C7	Note 1	±5%

Notes:

1. The RC network formed by R2 and C7 is required between the TXOP pin and the input to the modulator. This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C7, should be positioned to give maximum attenuation of high frequency noise into the modulator.
   The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:
   BT of 0.3 = 0.34/bit rate (bits/sec)
   BT of 0.5 = 0.21/bit rate (bits/sec)
   with suitable values for common bit rates being:

		R2	C7
4000 bits/sec	BT = 0.3	180.0kΩ	470pF
4800 bits/sec	BT = 0.5	91.0kΩ	470pF
8000 bits/sec	BT = 0.3	91.0kΩ	470pF
9600 bits/sec	BT = 0.5	47.0kΩ	470pF
19 200 bits/sec	BT = 0.5	91.0kΩ	120pF
32 000 bits/sec	BT = 0.3	47.0kΩ	220pF
32 000 bits/sec	BT = 0.5	47.0kΩ	150pF
38 400 bits/sec	BT = 0.3	47.0kΩ	180pF
38 400 bits/sec	BT = 0.5	47.0kΩ	120pF

   Note that in all cases the value of R2 should not be less than 47.0kΩ and that the calculated value of C7 includes calculated parasitic capacitances.
2. C3 and C4 should both be 15.0nF for a data rate of 8kbits/sec, and inversely proportional to the data rate for other data rates, e.g. 30.0nF at 4kbits/sec, 3.0nF at 40kbits/sec.
3. The FX579 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 6.5MHz (V_{DD} = 5V) and up to 5.0MHz (V_{DD} = 3V). The value chosen for C5 and C6 should be suitable for the applied V_{DD} and the frequency of X1 and include stray capacitance. As a guide: At 5 Volts, C5 = C6 = 33.0pF at 1.0MHz falling to 18pF at 6.5MHz
   At 3 Volts, C5 = C6 = 33.0pF at 1.0MHz falling to 18pF at 5MHz
   The equivalent series resistance of X1 should be less than 2.0kΩ at 1MHz falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/Clock circuit pins must be minimised.

Figure 2 Recommended External Components (SOIC Package)

1.5 General Description

1.5.1 Overall Function Description

The FX579 is a single chip processor that performs the baseband function of a half duplex modem employing Gaussian minimum shift keying (GMSK) modulation. Data rates of 4kbits/sec to 40kbits/sec and the choice of BT of 0.3 or 0.5 are pin programmable functions to suit radio data channel bandwidth requirements.

Figure 3 shows how the modem is used in a typical radio application. In transmit mode data at the DATAIO pin is retimed with the Tx clock (output at the DATACLK pin) before being level shifted and passed through the GMSK Gaussian filter to the TXOP pin. An external RC network forms part of this filter and is required, in association with any signal and dc level adjustment, for driving the radio's frequency modulator. In receive mode, data from the radio's frequency discriminator, having been adjusted externally for signal and dc levels to provide a nominal input level of 1V pk-pk centred around ½ V_{DD} (V_{DD} = 5V), is then processed to produce data at the DATAIO pin in binary form, together with a regenerated clock at the DATACLK pin.

Acquisition and lock of Rx data signals is made easier and faster by the use of an ACQUIRE input which can be set by the system µController as required.

The FX579 features a low current analogue/digital ASIC process offering significantly lower current consumption than DSP technology. This CMOS microcircuit is available in a 16-pin small outline (SOIC) package.

1.5.2 Description of Blocks and Signal Path

(Reference Block Diagram Figure 1).

Power Supply Circuits

These circuits produce the necessary internal voltage levels. Note that V_{DD} and V_{BIAS} should be decoupled to V_{SS} as shown.

Clock Oscillator and Divider

The transmit and (nominal) receive data rates are determined by division of the frequency present at the XTALN pin, which may be generated by the on-chip Xtal oscillator or come from an external source. Any Xtal/Clock frequency in the range 1.0MHz to 5.0MHz (V_{DD} = 3.0V) or 1.0MHz to 6.5MHz (V_{DD} = 5.0V) may be used depending upon the desired data rate.

A division ratio to facilitate data rate setting is controlled by the logic level inputs on the CLKDIVA and CLKDIVB pins and is shown in Table 1 together with examples of how various 'standard' data rates may be derived from common Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal or Clock Frequency}}{\text{Division Ratio}}$$

CLKDIVA	CLKDIVB	Division ratio = Xtal frequency ÷ Data rate	Xtal Clock Frequency			
			4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)
0	0	128	32 000	38 400	16 000	19 200
0	1	256	16 000	19 200	8000	9600
1	0	512	8000	9600	4000	4800
1	1	1024	4000	4800	-	-

Table 1 Clock and Data Rates (in MHz and bits/sec, respectively)

Note: (1) Device operation is not guaranteed for operation above 40kbits/sec or below 4kbits/sec.
(2) If a suitable Xtal or clock signal is not supplied, device supply current may increase.

Transmit Signal Path

The binary data applied to the DATAIO input is retimed within the chip on each rising edge of the Tx clock and then converted into a 1V pk-pk binary signal centred around V_{BIAS}. This signal is then connected to the input of the low pass Tx filter, and the output connected to the TXOP pin.

The Tx filter has a low pass frequency response, which is approximately Gaussian in shape, as shown in Figure 4. This minimises amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency components, which would otherwise cause interference into adjacent radio channels.

The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation versus frequency response of the transmit filtering provided by this chip has been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit rate.

Note that an external RC network is required between the TXOP pin and the input to the frequency modulator. This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering, and the ground connection to the capacitor should be positioned to give maximum attenuation of high frequency noise into the modulator. The component values should be chosen so that the product of the resistance (in Ohms) and the capacitance (in Farads) is:

0.34 / bit rate for BT of 0.3
0.21 / bit rate for BT of 0.5
(bit rate in bits per second)

Suitable values for common bit rates are given in Table 2

Data Rate	BT	R2	C7
4800 bits/sec	0.5	91.0 kΩ	470pF
8000 bits/sec	0.3	91.0 kΩ	470pF
9600 bits/sec	0.5	47.0 kΩ	470pF
19 200 bits/sec	0.5	91.0 kΩ	120pF
32 000 bits/sec	0.3	47.0 kΩ	220pF
32 000 bits/sec	0.5	47.0 kΩ	150pF
38 400 bits/sec	0.3	47.0 kΩ	180pF
38 400 bits/sec	0.5	47.0 kΩ	120pF

Table 2 Filter Bandwidth Selection

The TXOP signal is centred around V_{BIAS}, going positive for logic "1" level inputs to the DATAIO input and negative for logic "0" inputs. Note that when in receive mode the input of the internal buffer amplifier driving the TXOP pin is connected to V_{BIAS}.

Figure 5 shows typical transmit eye patterns (measured after the external RC network) for BT values of 0.3 and 0.5

Figure 6 shows the transmit output spectrum (measured after the external RC network) again for BT values of 0.3 and 0.5.

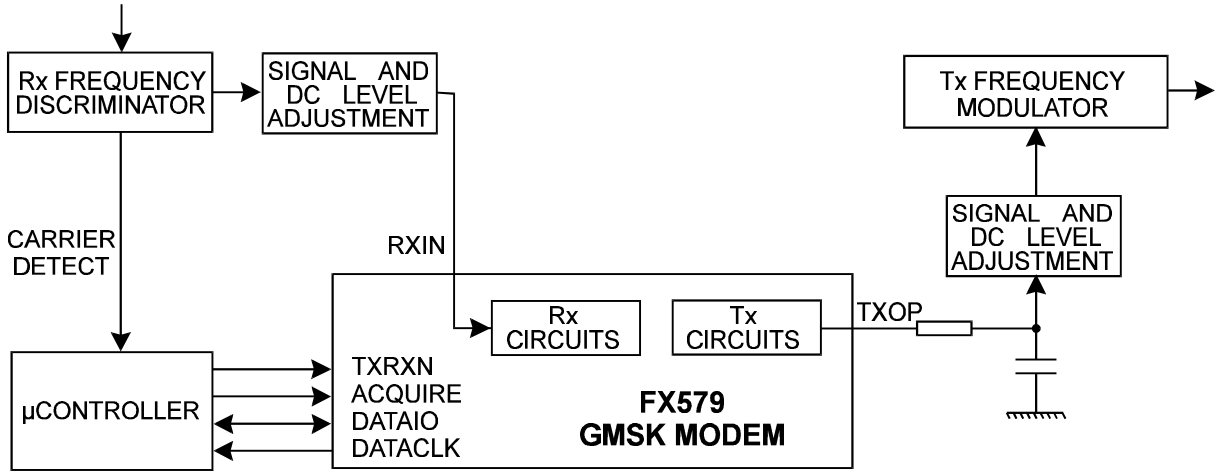


Figure 3 Typical Radio Application

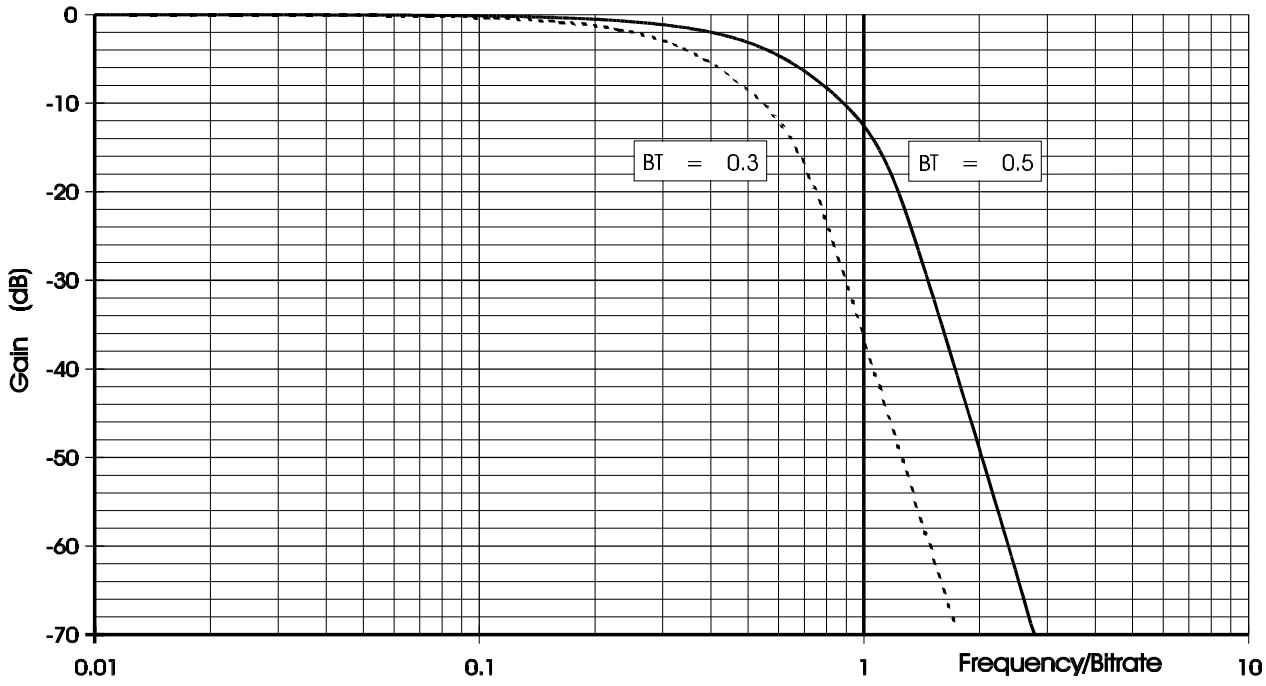


Figure 4 Typical Attenuation v. Frequency Response of Tx Filter (after external RC network)

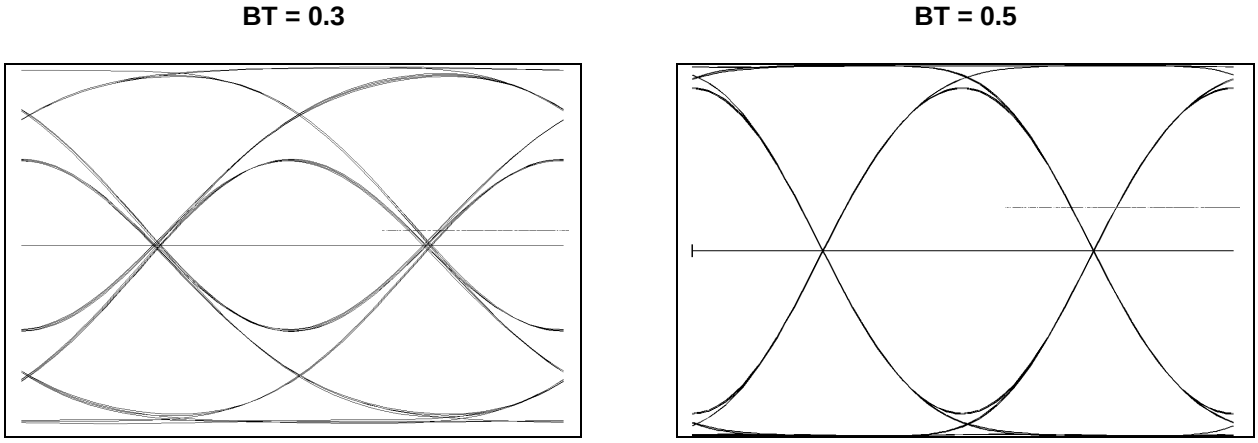


Figure 5 Typical Transmit Eye Patterns (after external RC network)

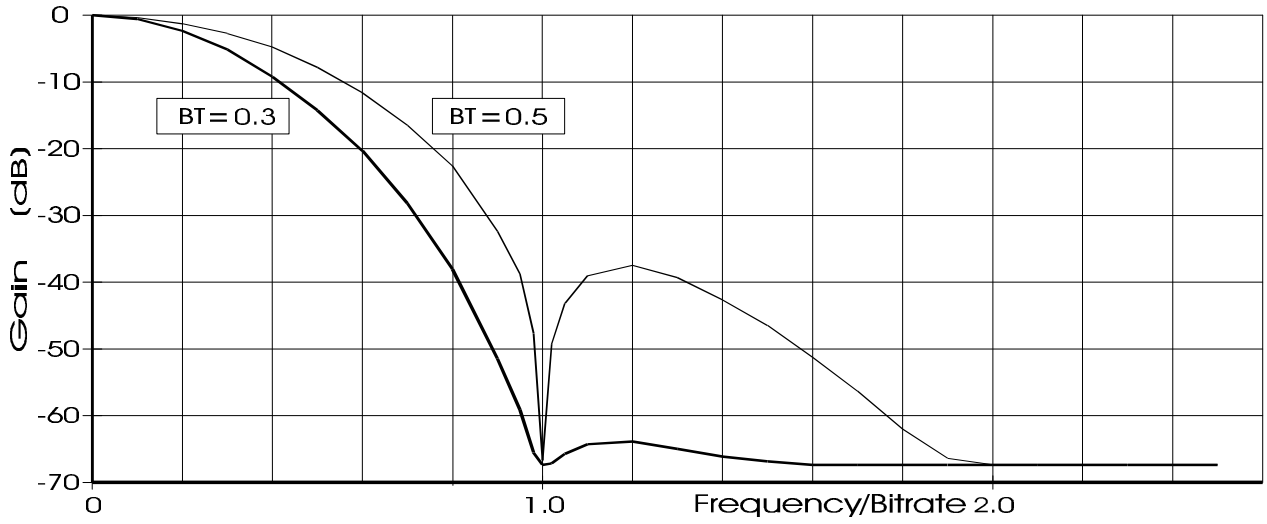


Figure 6 Tx Output Baseband Spectrum (for random data)

Receive Signal Path
The function of the Rx circuitry is to:

a) Accept an incoming signal from the radio's frequency discriminator at a defined level via suitable external signal and dc level adjustment
b) Clean the signal by filtering
c) Provide dc level thresholds for clock and data extraction
d) Provide clock timing information for data extraction and external circuits
e) Provide Rx data as an output in binary form

The output of the radio receiver's frequency discriminator after suitable external signal and level adjustment is applied to the RXIN pin. With V_{DD} = 5V, nominal input level when receiving a continuous "1111000011110000..." data pattern should be 1V pk-pk (level is proportional to V_{DD}) centred around ½ V_{DD}. Positive going signal excursions about V_{BIAS} at RXIN will produce a logic "1" on the DATAIO pin, negative going signal excursions will produce a logic "0".

The signal is then applied to the low pass Rx filter, which has a -3dB corner frequency of 0.56 times the data bit rate, before being applied to the Level Measuring and Clock and Data Extraction blocks.

Level Measuring Circuit
The 'Level Measuring' block consists of two voltage detectors one of which measures the amplitude of the 'positive' peaks of the received signal, while the other measures the 'negative' peaks. These detectors use the external capacitors connected to the DOC1 and DOC2 pins to form voltage hold or integrator circuits.

Results of the two measurements are then processed within the modem to establish the optimum dc level decision thresholds for the Clock and Data Extraction circuits, depending on the received signal amplitude, BT and any dc offset present.

The receive circuits operate in several control modes as defined by the logic level applied to the acquire pin. These are explained later - See 'Acquire Sequence'.

Rx Clock Extraction Block
The 'Rx Clock Extraction' circuit is based on a zero crossing tracking loop which uses a multi resolution digital phase locked loop (PLL). The wide bandwidth mode allows for fast initial phase acquisition. Eight good zero crossings are required for correct operation.

The highest timing resolution is obtained when the PLL is in its narrow bandwidth mode. This mode of operation yields the least amount of phase jitter, which is responsible for the associated bit error rate (BER) performance degradation.

The PLL operating mode is defined by the logic level applied to the ACQUIRE pin - See 'Acquire Sequence'.

Rx Data Extraction Block
The 'Rx Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the received signal, after filtering, in the middle of each bit period and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference depending on the chosen BT. The extracted data is output from the DATAIO pin and should be sampled externally on the rising edge of the received data clock.

Acquire Sequence

Figure 7 shows the typical received output from a radio's frequency discriminator. A data transmission in general begins with a burst of unmodulated carrier followed by preamble of, for example "11001100--" and then frame sync, so as to allow the receive modem to establish timing and level lock as soon as possible, before the message is sent.

In most applications there will also be a dc step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

Figure 7 shows two possible receive operating modes of the FX579. The mode shown in (a) is preferred and should be used when an external carrier detect signal is available, so as to provide the fastest possible acquisition of the received signal. The mode in (b) is suggested for when a carrier detect signal is unavailable. The receive operating modes are determined by the logic state of the ACQUIRE pin as explained in Table 3.

(a) Operation with a carrier detect (Preferred operating mode)

When an external carrier detect signal is available the µController should provide an ACQUIRE pulse as shown. The ACQUIRE input is pulsed to a logic "1" a minimum of 2 bit times after the carrier is detected (to allow for the receive filter delay) and just before preamble is expected (to reduce the probability of false frame sync detection under noisy conditions). The level measurement DOC capacitors are then automatically clamped to the input signal for fast acquisition. The ACQUIRE input should remain at a logic "1" for a minimum of 16 bit times to enable the level measurement circuits to stabilise and the PLL to quickly achieve lock. The ACQUIRE input should then be taken to a logic "0" again, for better signal to noise performance, once the preamble or Frame Sync has been detected by the controlling microprocessor.

(b) Suggested operation without a carrier detect (Non-preferred operating mode)

When a carrier detect signal is not available, it is suggested that the modem be operated in the Lossy Peak Detect/Wide Bandwidth mode (ACQUIRE pin at a logic "1") until the system µController satisfactorily detects preamble and/or frame sync. Then the ACQUIRE pin should be taken to a logic "0" for Peak Averaging/Narrow Bandwidth mode, so as to provide a better signal to noise performance for the rest of the message. The duration of initial unmodulated carrier plus preamble should be a minimum of 100 bit times to allow the voltages on the external DOC capacitors to stabilise. At the end of the message the ACQUIRE pin should be returned to a logic "1".

The FX579 generally can tolerate dc offsets in the received signal of at least ±0.5V with respect to V_{BIAS} (V_{DD} = 5V). The voltages on the DOC1 and DOC2 pins reflect the average peak positive and negative excursions of the (filtered) received signal, and could therefore be used to derive a measure of the data signal amplitude and carrier frequency offset. Note, however, that these pins are driven from very high impedance circuits, so that the dc load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

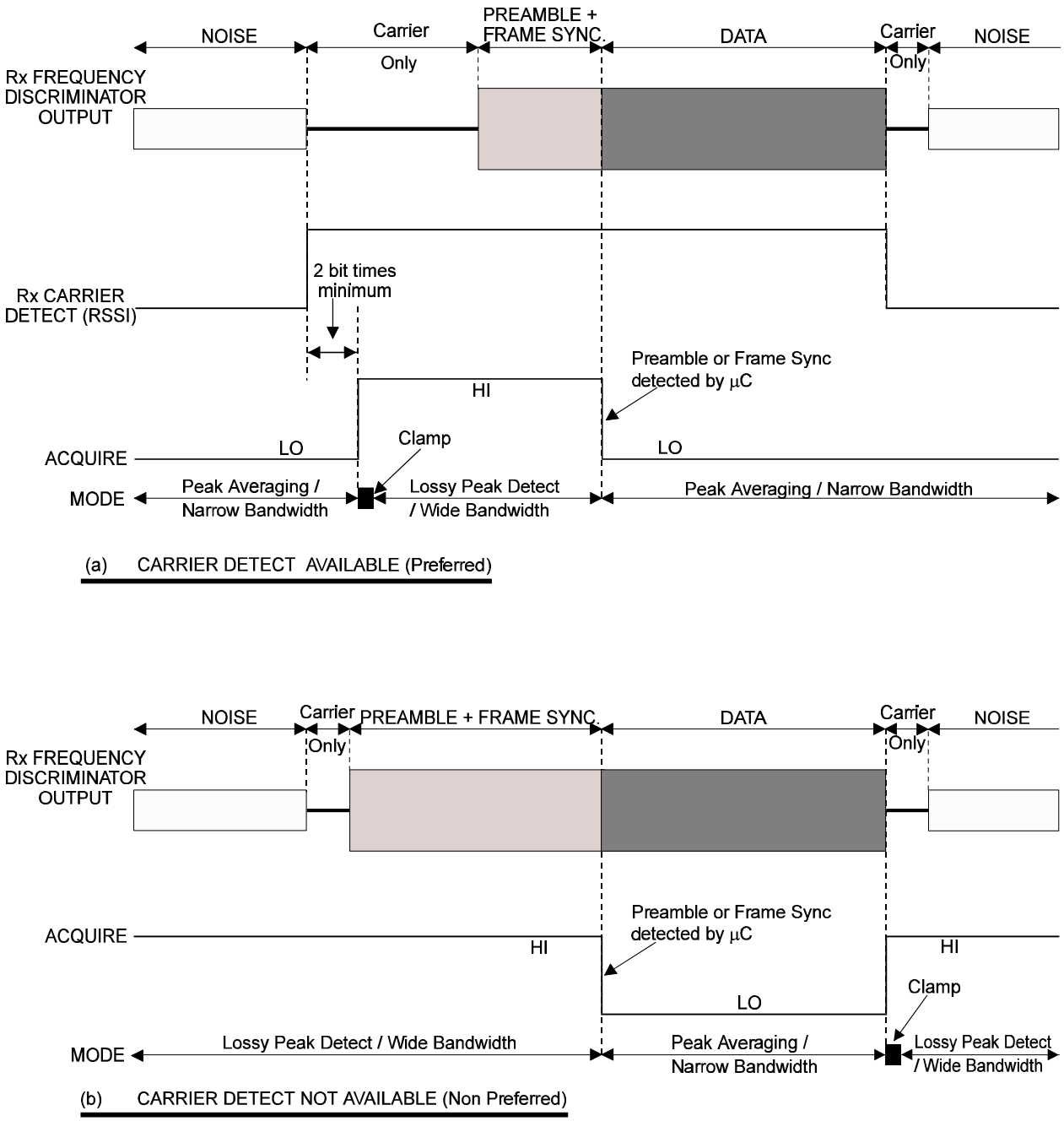


Figure 7 Receive Control Mode Diagram

ACQUIRE Pin	Rx Level Measurement Mode	PLL Mode
"0" to "1"	Clamp	Narrow → Wide Bandwidth
"1"	Lossy Peak Detect	Wide Bandwidth
"0"	Peak Averaging	Narrow Bandwidth

Rx Level Measurement Clamp: Operates for a minimum of two bit times, maximum three bit times, after a "0" to "1" transition of the ACQUIRE input. The external DOC capacitors are rapidly charged towards the input signal level, with the charge time constant being of the order of 0.5 bit time.

Rx Level Measurement Lossy Peak Detect: The detectors rapidly capture the +ve and -ve going signal peaks of the Rx filter output signal, these peaks being stored on the external DOC capacitors. The detectors operate in this mode whenever ACQUIRE is at a logic "1", except for the initial Clamp period.

Rx Level Measurement Peak Averaging: Provides a slower but more accurate measurement of the signal peak amplitudes. This operating mode depends on the PLL circuitry being in lock.

PLL Wide Bandwidth: Sets the PLL bandwidth wide enough to allow a lock to the received signal in 8 zero crossings. This mode will operate as long as ACQUIRE is at logic "1".

PLL Narrow Bandwidth: The correction applied to the extracted clock is limited to a maximum of ± 1/16th bit period for every 4 zero crossings received. The PLL operates in this mode whenever the ACQUIRE input is set to logic "0".

Table 3 Receive Operating Modes

Rx Data Formats

The receive section of the FX579 works best with data which has a reasonably 'random' structure, i.e. the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences (> 100 bits) of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of patterns without "11" and "00" should be avoided.

For this reason, it is recommended that data is scrambled in some manner before transmission, for example by 'exclusive-ORing' with the output of a binary pseudorandom pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of "1"s and "0"s i.e. "110011001100...." A "10101010...." preamble sequence will yield poor peak levels for the receive circuits, although performance is better with BT = 0.5 than with BT = 0.3.

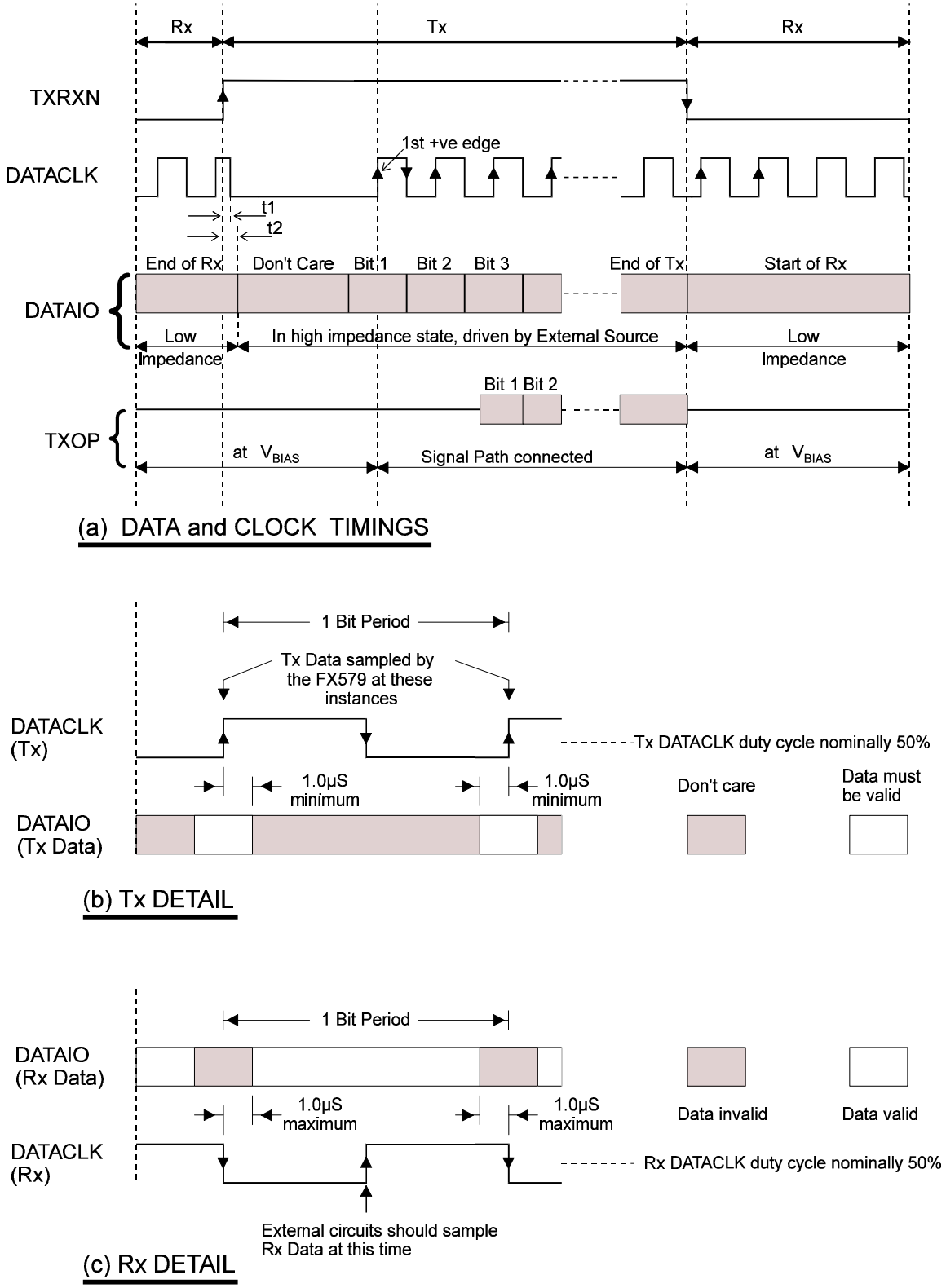


Figure 8 Tx/Rx Data and Clock Timings

Tx/Rx Switching
(Refer to Figure 8)

Rx to Tx Transition - following a "0" to "1" transition on the TXRXN input:

a) If DATACLK is at a logic "1" it will go to a logic "0" (t1 max = 1µs), or if at logic "0" will stay low. It will then remain at "0" for a minimum of 2 bit times, maximum of 3 bit times, before the first +ve transmit clock edge occurs.

b) The DATAIO line will go to a high impedance state ready for Tx data to be applied (t2 max = 1µs). Data on the DATAIO line should be set up and ready for when the first +ve transmit clock edge occurs. This edge will clock the first bit of data into the transmit filter. Succeeding -ve clock edges may be used by the µController to ensure that data is always set up when +ve edges occur.

c) TXOP is opened to the transmit path upon occurrence of the first +ve clock edge. Due to the delay of the filter, the centre of Bit 1 will appear at the pin a maximum of 2 bit times (BT = 0.5) or 2.5 bit times (BT = 0.3) later.

d) At the end of a message the transmit output will remain in the state of the last bit sent.

e) If a long period of unmodulated carrier is required before a message (approximately 10ms as on MOBITEX), then the radio's transmitter should be keyed up with the FX579 modem still in Rx mode.

Tx to Rx Transition - following a "1" to "0" transition on the TXRXN input:

a) DATACLK continues at the nominal bit rate in a free-running mode until locked to a receive signal, e.g. after a satisfactory ACQUIRE sequence.

b) The buffer driving the TXOP pin is immediately connected to V_{BIAS}.

c) The DATAIO line immediately goes low impedance and starts sending Rx data.

d) There is a 3-bit delay in the receive path before RXIN input data can appear at the DATAIO pin.

1.6 Application Notes

Radio Channel Requirements
To achieve legal adjacent channel performance at high bit rates, a radio with an accurate carrier frequency and an accurate modulation index is required.

For optimum channel utilization, (eg. low BER and high data rates) attention must be made to the phase and frequency response of both the IF and baseband circuitry, and to the accuracy of the Tx/Rx carrier frequencies.

Bit Rate, BT and Bandwidth
The maximum data rate that can be transmitted over a radio channel depends on the following:

Channel spacing
Allowable adjacent channel interference
Tx filter bandwidth
Peak carrier deviation (Modulation Index)
Tx and Rx carrier frequency accuracies
Modulator and demodulator linearity
Receive IF filter frequency and phase characteristics
Use of error correction techniques
Acceptable error-rate

As an example, for MOBITEX operation, a raw data rate of 8kbits/sec at 12.5kHz channel spacing may be achievable - depending on local regulatory requirements, using a ± 2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between Tx and Rx carrier frequencies.

Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data rate to 4800bits/sec would allow the BT to be increased to 0.5, thus improving the error rate performance.

For CDPD operation, a 19 200 bits/sec raw data rate at 30kHz channel spacing may be utilised with a ± 8kHz maximum deviation, a BT of 0.5, and no more than 3kHz discrepancy between Tx and Rx carrier frequencies.

These examples should be used for guidance purposes only. Regulatory compliance of a design should be verified.

FM Modulator, Demodulator and IF
For optimum performance, the 'eye' pattern of the received signal (when receiving random data) applied to the FX579 should be as close as possible to the transmit 'eye' pattern examples shown in Figure 5.

Of particular importance are general symmetry, cleanliness of the zero crossings, lack of overshoot and, for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to:

a) Linearity and frequency/phase response of the Tx frequency modulator.
(Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. Hence two point modulation is necessary for synthesised radios.)

b) Bandwidth and phase response of the Rx IF filters.

c) Accuracy of the Tx and Rx carrier frequencies.
(Any difference will shift the received signal towards one of the skirts of the IF filter response.)

AC Coupling of Tx and Rx Signals
Ideally, the transmit path to the modulator should be dc coupled. Similarly, the Rx demodulated signal after external adjustment should be dc coupled to the FX579 RXIN pin, providing a signal symmetrically centred about V_{BIAS}. Figure 9 shows the bit error rate (BER) performance under these conditions for BT values of 0.3 and 0.5 in peak averaging mode. However, practical applications may require ac coupling from the FX579's transmit output to the frequency modulator and between the receiver's frequency discriminator and the FX579's receive input. This creates two problems:

a) AC coupling of the signal will degrade the FX579's bit error rate (BER) performance, as shown in Figure 10 for a data rate of 8kbits/sec, with V_{DD} = 5V and BT = 0.3.

b) AC coupling at the receive input will transform a step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the FX579's level measuring circuits. Sufficient time should therefore be allowed for the signal into the FX579 to settle before the ACQUIRE line is activated.

It is recommended that a data message does not contain long sequences of consecutive ones or zeroes and that the Tx and Rx path frequency responses have cut off frequencies of ≤5Hz and ≤20Hz respectively, for a data rate of 8kbits/sec and BT = 0.3.

Two-Point Modulation
When designing the FX579 into a radio that uses a frequency synthesiser, a two point modulation technique is recommended. This is to prevent the radio's PLL circuitry from counteracting the modulation process, and so provide a clean flat modulation response down to dc.

The transmit output (after the external RC) should be suitably buffered before being applied to the radio's synthesizer. The drive should be applied to both the Voltage Controlled Oscillator and Reference Oscillator Modulation inputs with suitable ac/dc levels and with correct phase to achieve good cancellation of the loop's feedback and so provide a flat modulation response.

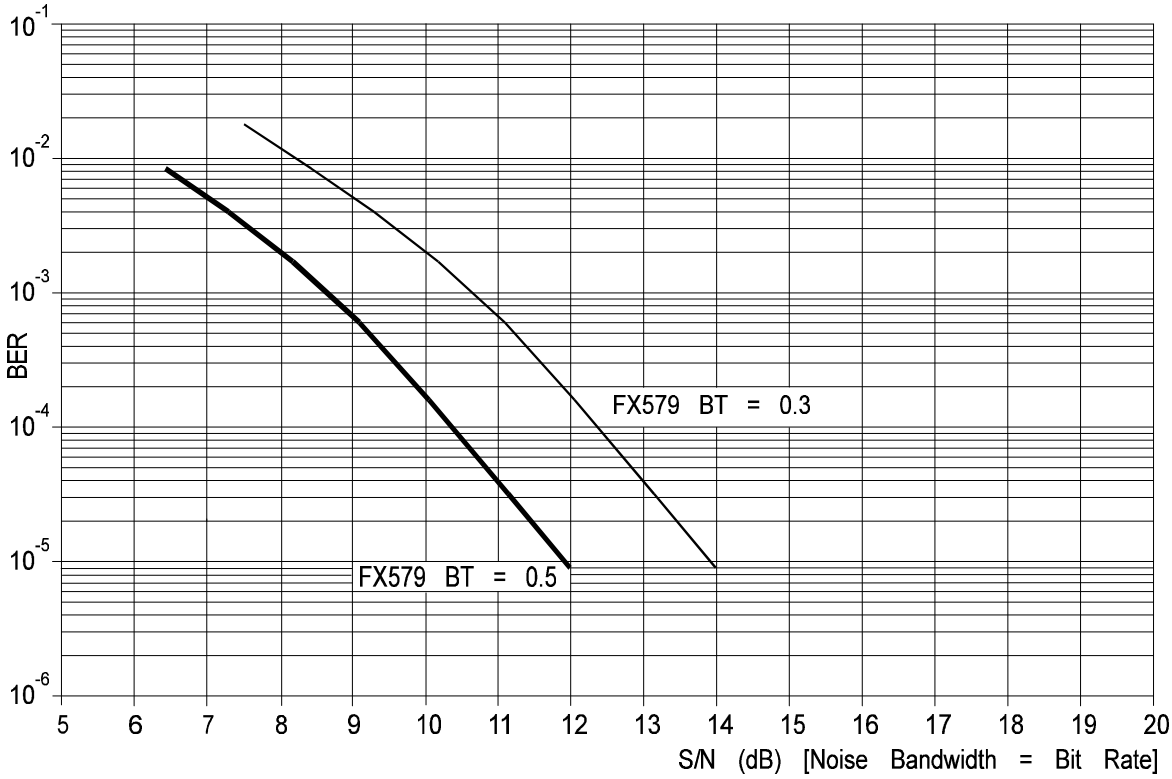


Figure 9 Typical Bit Error Rate Performance

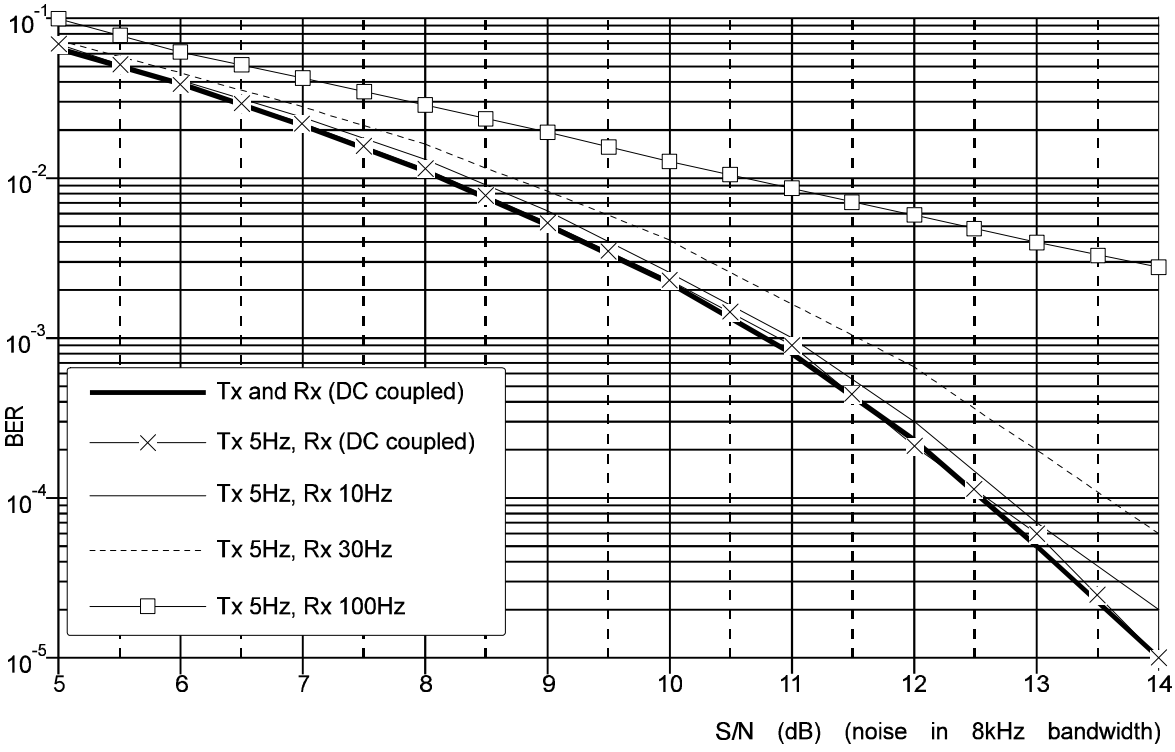


Figure 10 Effect of AC Coupling on Typical Bit Error Rate (8000 bits/sec, BT = 0.3)

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply voltage (V_{DD})	-0.3	7.0	V
Voltage on any pin (ref. V_{SS} = 0V)	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C
D4 Package (Plastic)			
Total allowable power dissipation at Tamb=25°C		800	mW
..... Derating		13	mW/°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Condition	Min.	Max.	Units
Operating Temperature		-40	+85	°C
Supply Voltage (V_{DD})		3.0	5.5	V
Xtal/Clock Frequency	(V_{DD} < 4.5V)	1.0	5.0	MHz
Xtal/Clock Frequency	($V_{DD} \geq$ 4.5V)	1.0	6.5	MHz
Data Rate	(V_{DD} < 4.5V)	4000	20 000	bits/sec
Data Rate	($V_{DD} \geq$ 4.5V)	4000	40 000	bits/sec

Operating Characteristics
All device characteristics are measured under the following conditions unless otherwise specified:

Tamb = 25°C, V_{DD} = 5.0V, Xtal frequency = 4.096MHz
Data rate = 8000 bits/sec, Noise bandwidth = bit rate

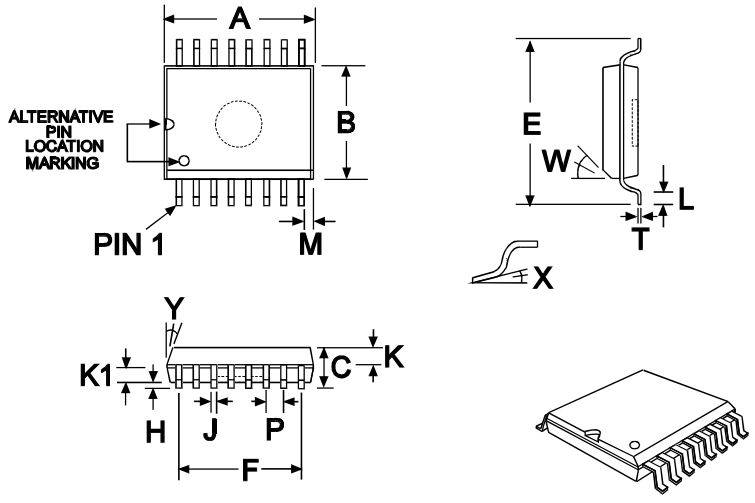
Characteristic	Note	Min.	Typ.	Max.	Units
Static Values					
Supply Current					
(for V_{DD} = 3.0V)	1	-	-	2	mA
(for V_{DD} = 5.0V)	1	-	-	4	mA
Logic "1" input level		3.5	-	-	V
Logic "0" input level		-	-	1.5	V
Logic input current	2	-5.0	-	5.0	µA
Logic "1" Output Level at I_{OH} = -120µA		4.6	-	-	V
Logic "0" Output Level at I_{OL} = 120µA		-	-	0.4	V

Characteristic	Note	Min.	Typ.	Max.	Units
Transmit Parameters					
TXOP output impedance	3	-	100	-	Ω
TXOP output level	4, 6, 9	0.8	1.0	1.2	Vpk-pk
Tx output offset (wrt V_{BIAS})	-	-100	-	+100	mV
Tx data delay (BT = 0.3)	5	-	2.0	2.5	bit periods
Tx data delay (BT = 0.5)	5	-	1.5	2.0	bit periods
Receive Parameters					
RXIN input impedance			3	-	MΩ
RXIN input level	7, 9	0.7	1.0	1.3	Vpk-pk
Rx dc offset from ½ V_{DD}	9	-	±0.5	-	V
Rx time delay	8	-	-	3	bit periods
On-Chip Xtal Oscillator					
Input impedance	10	10		-	MΩ
Output impedance	10	-	50	-	kΩ
Voltage gain	10	-	25	-	dB
"High" clock pulse width	11	60	-	-	ns
"Low" clock pulse width	11	60	-	-	ns

Notes:

1. Not including any current drawn from the modem pins by external circuitry
2. For V_{IN} in the range V_{SS} to V_{DD}
3. Measured by ac coupling an external 1kHz source via suitable resistance to the TXOP pin. The value specified is the average of values measured in the all "1"s and all "0"s states
4. Data pattern of "1111000011110000..."
5. Measured between the rising edge of the Tx DATACLK and the centre of the corresponding bit at the output of the external RC network connected to TXOP
6. Measured at the output of the external RC network
7. For optimum performance, measured at RXIN for a "1111000011110000..." pattern
8. Measured between the centre of bit at RXIN and corresponding rising edge of the Rx data clock
9. Levels are proportional to applied V_{DD}
10. Small signal measurement at 100Hz with no load on XTALN output
11. Timing for an external clock input to the XTAL/CLK pin

1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.366 (9.29)	
H	0.004 (0.10)		0.012 (0.30)
J	0.013 (0.33)		0.019 (0.48)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 11 SOIC Mechanical Outline: *Order as part no. FX579D4*

CONSUMER MICROCIRCUITS LIMITED

1 WHEATON ROAD
WITHAM - ESSEX CM8 3TD - ENGLAND

Telephone: +44 1376 513833
Telefax: +44 1376 518247