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i.MX Applications Processors with Hantro's Multimedia Framework

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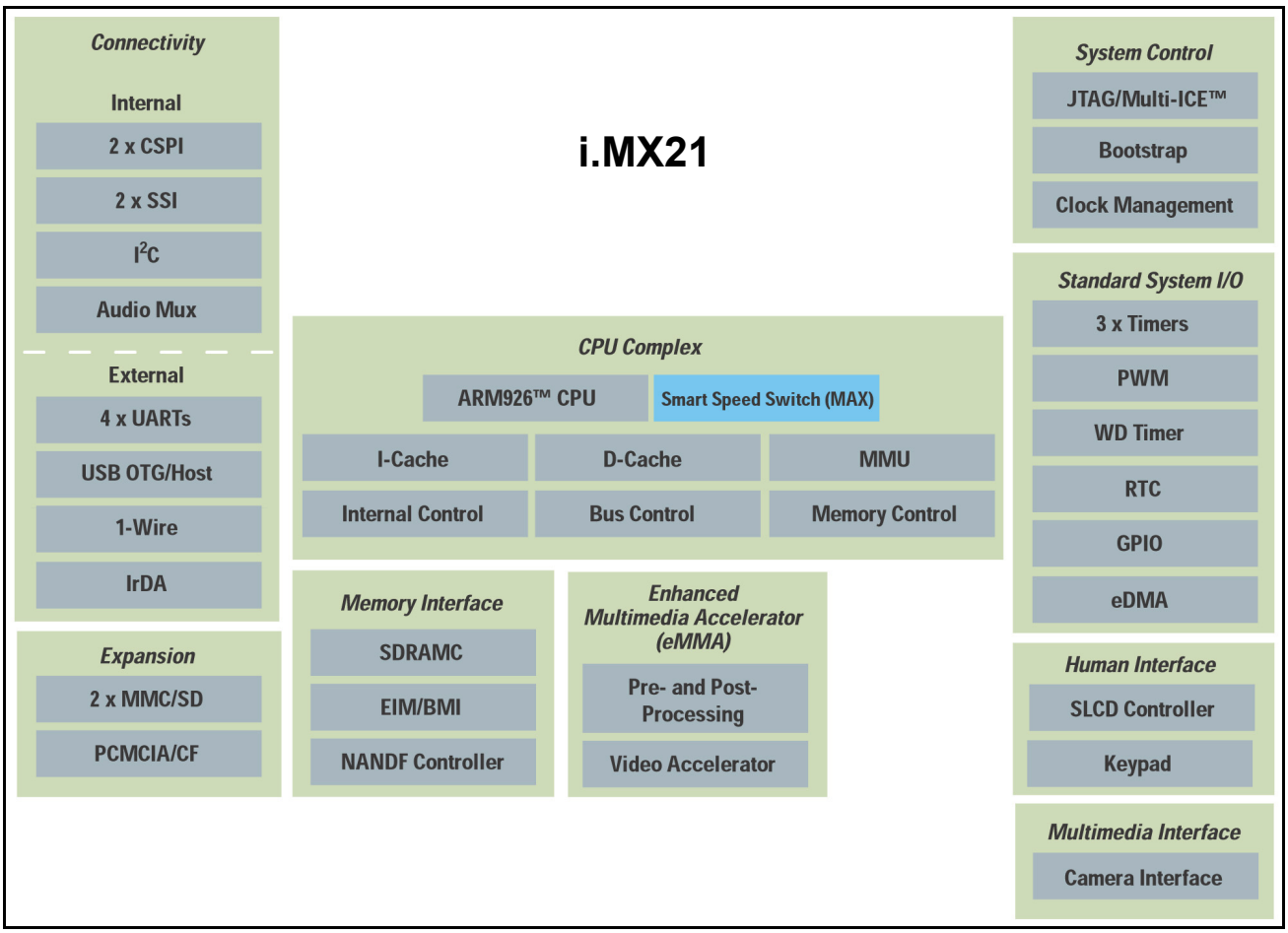
Executive Briefing

Although multimedia is on the tip of everybody's tongue when we talk about the advanced capabilities of new wireless handheld communications devices, the technologies that can really turn multimedia services into useful tools and eye-popping entertainment are just beginning to reach the marketplace.

The i.MX1 is the latest of the advanced class of ARM9™ core-based applications processors that are designed to specifically address requirements of turning full-blown, real-time multimedia into a pocket-sized reality. The i.MX1, with an ARM920T™ core processor, is designed to provide performance with stamina — a powerful, cost-effective and low-power applications processor for smart phones, wireless enabled PDA's, and other mobile wireless devices.

i.MX1's integrated multimedia functions include a color LCD controller, which is designed to support up to VGA (640 pixels x480 lines) resolution, and video port with built-in image pre-processing. In addition to the ARM920T core, Freescale Semiconductor has also added a fixed-point multiplier and DCT (discrete cosine transform) hardware accelerator. The combination of the ARM920T core processor and Freescale technology enables the i.MX1 to readily meet the performance requirements needed to implement today's multimedia applications.

Freescale, however, has gone a step further to extend the multimedia capabilities of the i.MX family of processors. The company has teamed with Hantro and licensed their advanced video codec. The Hantro codec may be implemented as software, hardware, or as a combination of software and hardware. The Hantro software codec is included in the i.MX1 delivery package.



i.MX Family and Hantro Video Technology

Having already ported the Hantro software video codec to the i.MX1 processor, we have now added Hantro video codec hardware, along with the software, to our recently announced next generation i.MX21 applications processor. Designed to deliver real-time MPEG4 and H.263 video compression and decompression, the codecs are standards-based and scalable from low image resolutions and frame rates up to CIF (352x288) at 30 fps (frames per second).

Further more, to facilitate application development, multimedia middleware is available from Hantro to enable functions such as: video record, playback (in a camcorder, for instance) and content sharing through standard compression mechanisms and file formats. The high compression ratios of the video codec helps ensure compact video file sizes, designed to deliver a cost-effective use for the end user when sharing content over a wireless network.

The ARM920T processor in the i.MX1 has plenty of performance overhead to perform sophisticated multimedia functions using Hantro's software codec. For instance, running video conference—with viewfinder, MPEG-4 decode, image deblock, image CSC (color space conversion), and MPEG-4 encode-on QCIF (Quarter CIF-176x144), 15 fps at 64Kbits/sec—uses only about 150 MHz (speeds are approximate) with a 16-bit external memory bus. A 32-bit external memory bus helps reduce the speed and performance requirements even further, to about 130 MHz.

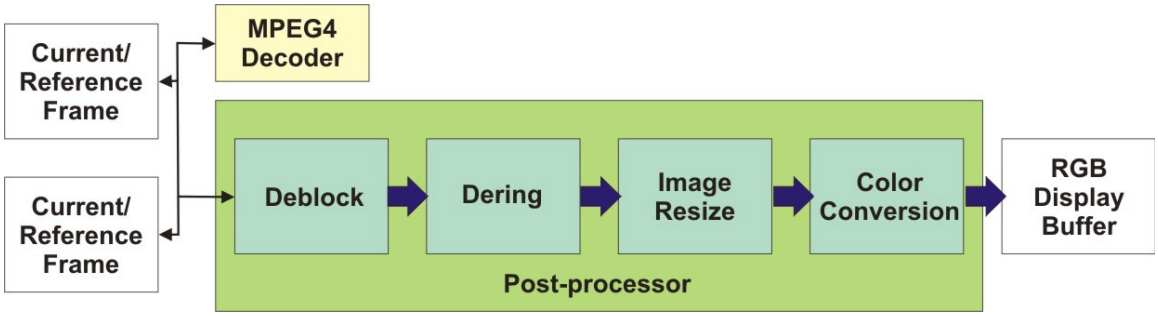
In another example, one-way video streaming of QCIF at 30 fps, using MPEG-4 decode, image deblock, and image CSC, requires just over 100 MHz with a 16-bit memory bus and only about 90 MHz with a 32-bit memory bus.

Both the Hantro codec and the i.MX1 architecture are optimized to provide high performance at low power levels. So, even though software solutions are often viewed as resource hogs, in this particular case the flexibility of a software codec doesn't stretch the processor to the limits of its performance capabilities.

i.MX21 and the Hantro Hardware Implementation

The next generation i.MX processor, the i.MX21, includes the ARM926EJ-S™ core processor operating at speeds starting at 266 MHz, and is designed to support both 16-bit and 32-bit external memory buses. The i.MX21 also includes an LCD controller supporting resolutions up to SVGA resolutions, eMMA (enhanced multimedia accelerator), and a video port.

The i.MX21's eMMA includes the Hantro MPEG-4 hardware and Freescale technology for pre-processing and post-processing hardware. Utilizing the i.MX21 eMMA for a videophone use case scenario (see below), less than 20 MHz of processor loading may be required to support these functions thereby helping to reduce the overall use case loading which is described later.



There are distinct advantages offered by the hardware eMMA. All computer intensive encoding and decoding calculations are executed in hardware, with software only handling the control functions. This means that the i.MX21 is designed to handle the simultaneous encode and decode of CIF resolution video at 30 fps. This kind of performance is particularly critical to meet the demanding requirements of real-time 30 fps wireless video conferencing. The i.MX21 is designed to meet these requirements and does it with resources to spare—resources that may be used to perform additional activities.

Also, by complementing Hantro's video codec with Freescale's pre-processing and post-processing hardware technology, the i.MX21 is a unique solution with enhanced multimedia performance. The pre-processing hardware technology comprises image resizing and CSC between the image sensor and the encoding process. The post-processing hardware technology comprises everything between decoding and display. The Freescale technology includes algorithms for deblocking, deringing, and resizing, which contribute to creating a sharper, clearer image, regardless of format

In addition, there is an inherent advantage to implementing the Hantro MPEG-4 and H.263 codec with Freescale technology in hardware since it requires far less power to operate than a software only solution. Simply put, it is designed to take less power to trip a gate than it does to run software. Still, the options are not simply all software or all hardware. The Hantro video codec may be implemented as a combination of hardware and software, depending upon applications processor priorities.

Two Freescale test case analyses, one with a video phone and the other with one-way streaming, demonstrate the flexibility of the i.MX21/Hantro solution, and how a hardware implementation can help reduce the amount of processing power needed for multimedia functions.

A Power Saving Demonstration

In the videophone use case scenario (QCIF, 15 fps), a live, real-time video and audio link is established between a wireless handheld and another device. The applications processor had to support the following applications, running in parallel: MPEG-4 encode; MPEG-4 decode; MPEG-4 post-processing, including deblock, dering, resizing, and color space conversion; image pre-processing and camera view finding; AMR (adaptive multi-rate) voice encode; AMR voice decode; echo cancellation, and operating system overhead, using operating systems such as Symbian OS, Palm OS, WinCE or eLinux. All megahertz numbers are approximate and are based on simulated performance analyses.

To run all these functions using only the ARM926EJ-S core unit would require well in excess of 400 MHz. In this case, MPEG-4 encoding alone would require about 190 MHz. Employing low-level assembly optimized MPEG-4 encode and decode, plus eMMA pre-processing and post-processing hardware acceleration, helps to reduce cycle usage to approximately 250 MHz.

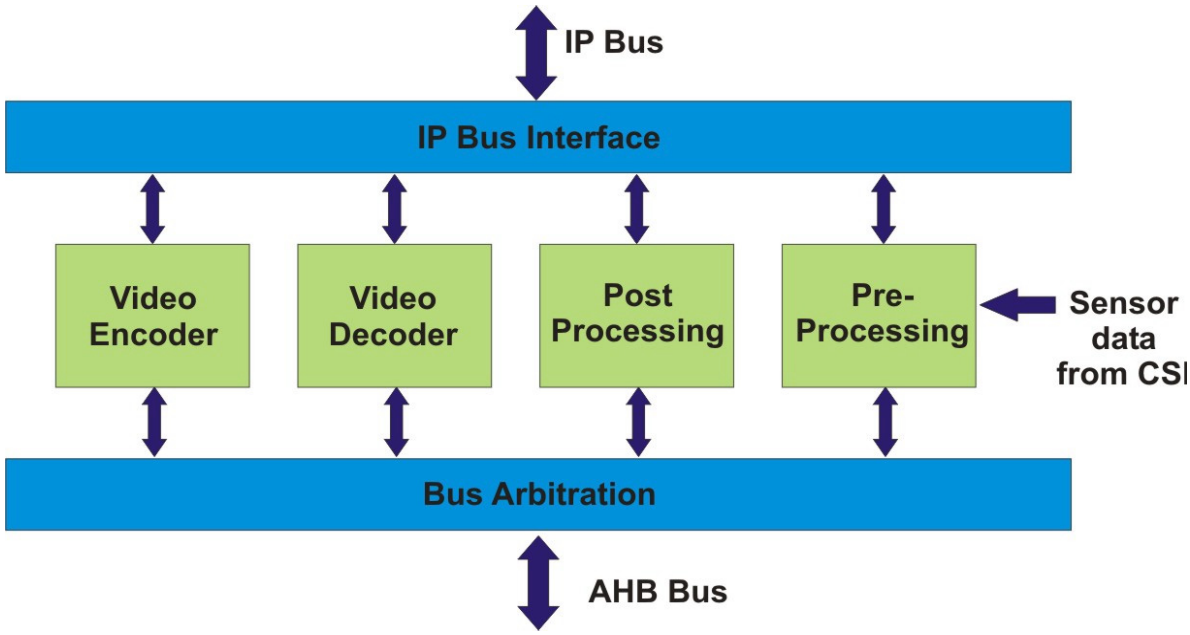
By implementing encode and decode in hardware, as well as the Freescale post-processing technology, performance requirements plummet to about 160 MHz.

The one-way streaming use case scenario involves streaming CIF resolution 30 fps MPEG-4 encoded data from external memory/flash memory (or across a wireless link through an MPEG-4 decoder) to a display. The applications processor is required to support: MPEG-4 Decode; MPEG post-processing, including deblock, dering, scaling, and color space conversion; audio decoder (MP3 or AMR); and OS overhead.

For the ARM926EJ-S alone, using optimized MPEG-4 decode software, meeting these requirements would require about 610 MHz. MPEG-4 decoding alone would take 140 MHz (much more than for the video phone because of the higher resolution and greater frame rate requirements). By implementing the Freescale post-processing technology in hardware, the performance requirement drops to about 210 MHz. Furthermore, employing Hantro's hardware decoder rather than the optimized decode software-only solution gets you down to less than 100 MHz.

The Modular Solution

Each block that makes up the eMMA—video encoder, video decoder, post-processing and pre-processing technology—is an independent component that may be implemented in hardware or software, regardless of how the other blocks are employed.



For instance, the i.MX21 is designed to employ the full Hantro codec and the Freescale pre-processing and post-processing in hardware, but the processor has plenty of megahertz overhead to explore other options, depending on the application requirements. With a combination software and hardware implementation of the Hantro video codec, computation intensive priorities may be performed in hardware while less demanding and frequently changing requirements may be executed in software, thus helping to provide power saving performance and enhanced flexibility exactly where they are needed.

The post-processing hardware acceleration is designed to support either the hardware decoder or a custom software decoder. Even the sub-blocks within the post-processing block—deblock, dering, and resize—are independent components that may be individually bypassed by software configuration if it's not needed for a particular post-processing process use case scenario.

The modular approach employed by both Hantro and Freescale also helps ease the migration from i.MX1 to i.MX21. Since it's made up of independent components, the software codec used in the i.MX1 may be transferred to the i.MX21 and plugged into its new host. What's more, Hantro provides the multimedia middleware that ties all the blocks together for developing multimedia applications. In the end, re-development time and expenses are minimized when migrating from i.MX1 to i.MX21 allowing developers to reach the market quickly with new products.

Conclusion

The combination of Freescale's i.MX processors's high performance technology and Hantro's software or hardware solution is ideal for making the most from available resources. The Hantro software codec can provide a flexible implementation that enables the i.MX1 to meet the needs of today's multimedia enabled wireless and hand held devices.

Now, stepping into the future with the powerful i.MX21, a full hardware implementation is possible, or a software/hardware combination can be used, employing the greatest advantages of each where they are needed the most. The combination of high performance, enhanced flexibility, and significant power savings can be realized in one applications processor.

Delivering real-time multimedia in pocket-sized mobile devices is a huge challenge, particularly since the world's carriers keep enticing the consumers with new and advanced video and audio services. The Freescale family of i.MX processors is continuing to evolve to support the multimedia features of the future. As part of this evolution, Hantro's video codec provides a foundation that enables rapid concept-to-market implementation through the next several generations of the i.MX family of processors.

Revision History

This revision is to provide change from Motorola to Freescale Semiconductor.

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