JUN 12 1992

VITELIC

V53C100B FAMILY HIGH PERFORMANCE, LOW POWER 1M X 1 BIT FAST PAGE MODE CMOS DYNAMIC RAM

PRELIMINARY

HIGH PERFORMANCE V53C100B	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	20 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read-Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V53C100BL	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	200 µA	200 µA	200 µA

Features

- 1M x 1-bit organization
- Low power dissipation for V53C100B-80
  - Operating Current – 70 mA max.
  - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C100B – 1.0 mA max.
  - V53C100BL – 0.2 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- Refresh Interval
  - V53C100B – 512 cycles/8ms
  - V53C100BL – 512 cycles/64ms
- Fast Page Mode operation for a sustained data rate greater than 25 MHz
- Standard packages are 18 pin Plastic DIP and 26/20 pin SOJ
- Low Battery Back-up Current
  - V53C100BL – 300 µA max.
  - 200 µA max. available on request

Description

The Vitelic V53C100B is a high speed 1,048,576 x 1 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS IV technology, the V53C100B offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power.

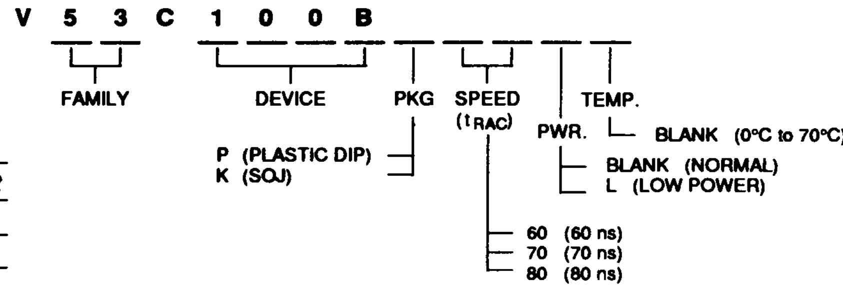
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random or sequential access of up to 1024 bits within a row with cycle times as short as 40 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical timing requirements for fast usable speed. These features make the V53C100B ideally suited for cache based mainframe and mini computers, graphics, digital signal processing and high performance microprocessor systems.

The V53C100BL offers a maximum data retention power of 1.65 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

Device Usage Chart

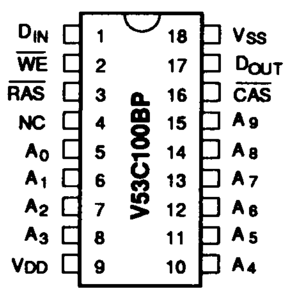
Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	60	70	80	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank

V53C100B Rev. 01 September 1991

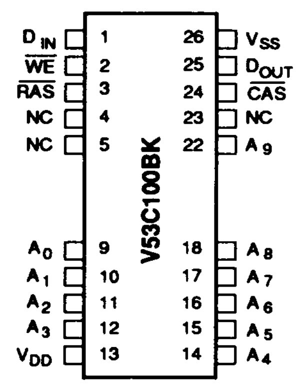


Description	*Pkg.*	*Pin Count*
Plastic DIP	P	18
SOJ	K	26/20

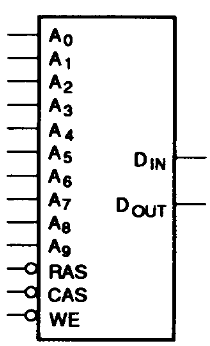
18 Lead Plastic DIP PIN CONFIGURATION Top View



26/20 Lead SOJ Package PIN CONFIGURATION Top View



LOGIC SYMBOL



Pin Names

A_0–A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias ....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} ....–1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ....–1.0 V to +7.0 V
Data Out Current ....50 mA
Power Dissipation ....1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Capacitance**

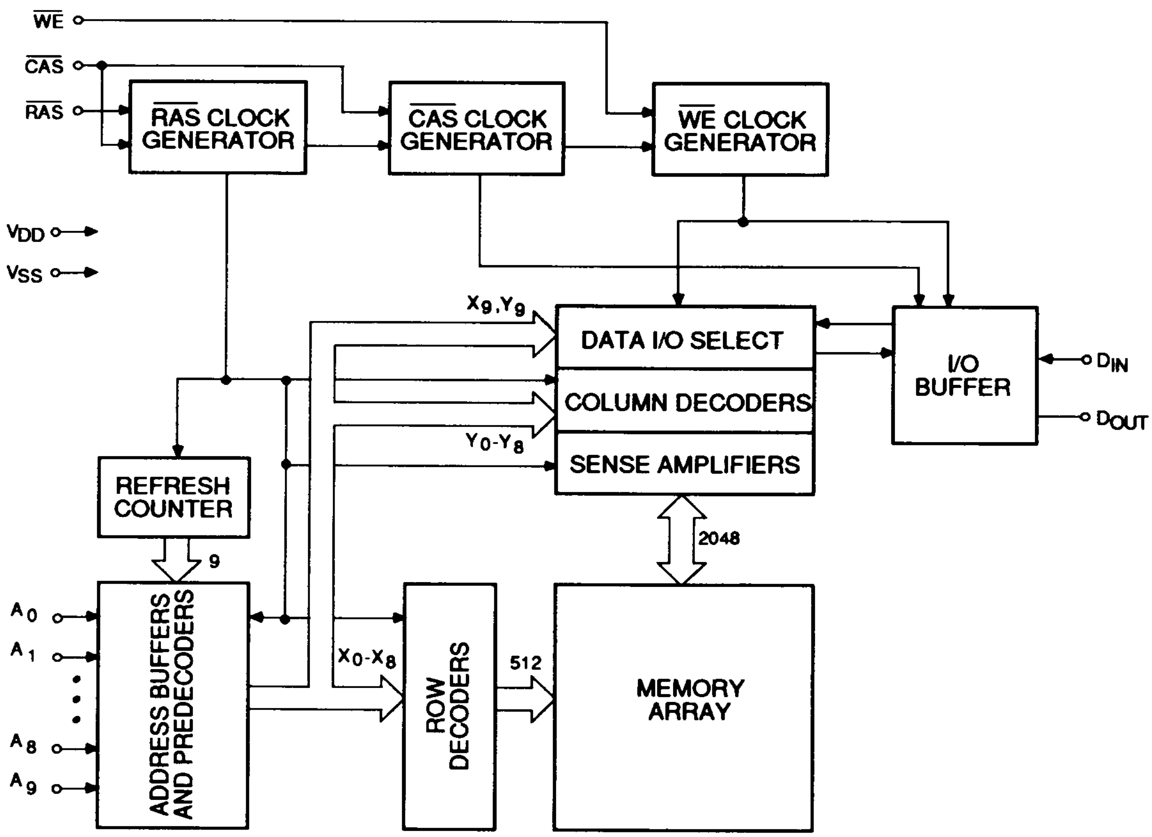
T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	7	pF
C_{OUT}	I/O	—	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram

1M x 1



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C100B Min.	V53C100B Max.	V53C100BL Min.	V53C100BL Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		–10	10	–10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	–10	10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		90		90	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		70		80		80			
		80		70		70			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		90		90	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		80		80			
		80		70		70			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		80		80	mA	Minimum Cycle	1,2
		70		70		70			
		80		60		60			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			3.0		2.0	mA	$\overline{RAS}=V_{IH}$,$\overline{CAS}=V_{IL}$ other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby			1.0		0.2	mA	$\overline{RAS} \ge V_{DD}$ –0.2 V, $\overline{CAS} \ge V_{DD}$ –0.2 V, other inputs ≥ V_{SS}	
I_{DD7}*	Battery Back-up Data Retention Current (V53C100BL only)			N.A.		0.3*	mA	$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle t_{RC}=125µs, t_{RAS}<1µs CMOS Clock Levels	1, 18
V_{IL}	Input Low Voltage (all inputs)		–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)		2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = –5 mA	

*I_{DD7} = 0.2 mA max. available on request.

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40	ns	8,9, 15
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20	ns	8,15
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75K	20	75K	20	75K	ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	10
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	10
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	11

AC Characteristics *(Cont'd.)*

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	15		20		20		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		ns	14
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		15		ns	14
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
33	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	140		155		175		ns	
34	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	80		95		105		ns	
35	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time Read-Modify-Write Cycle	60		70		80		ns	12
36	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	15		20		20		ns	12
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		ns	12
38	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45	ns	15
39	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		45		50		ns	

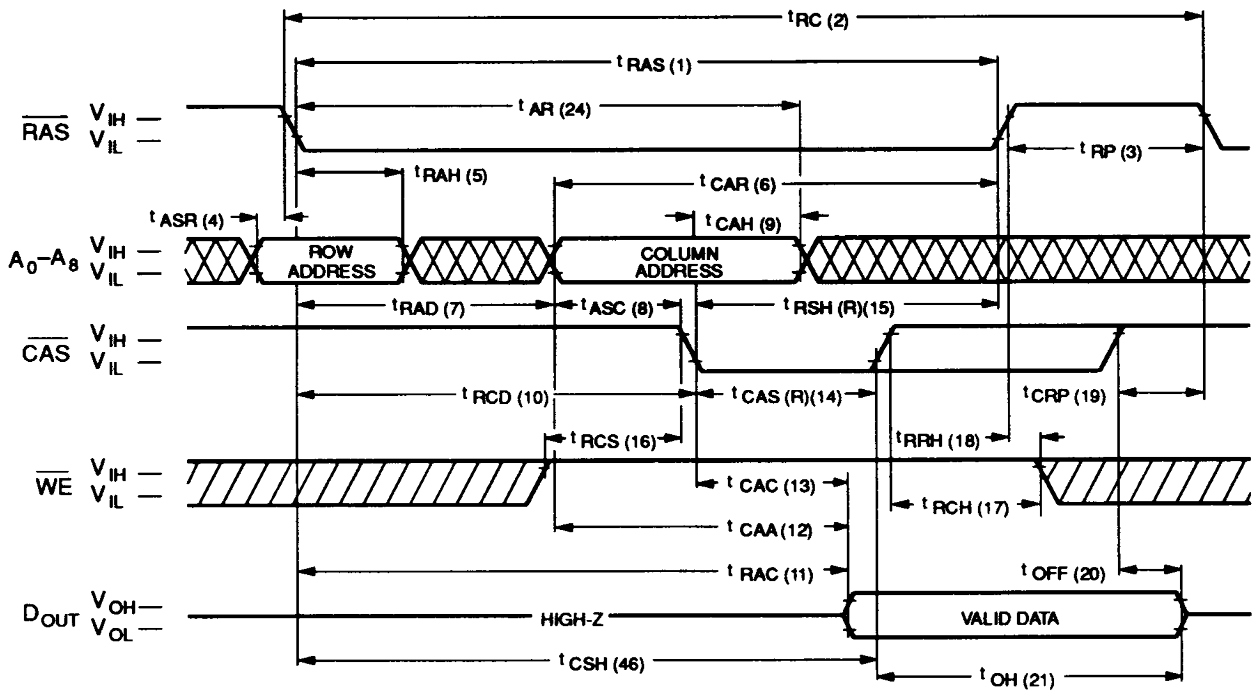
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	60		70		75		ns	
41	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		ns	
42	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
43	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	30		30		30		ns	
46	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
47	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	16
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C100BL only (512 Cycles, t_{RC} = 125 µs)		64		64		64	ms	18

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in First Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \le t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \le t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    t_{RC} = 125 µs (125 µs x 512 = 64 ms)
    t_{RAS} = t_{RAS} (min.) to 1 µs
    Input voltages: $\overline{RAS}$ and $\overline{CAS}$ — $V_{IH} > V_{DD} - 0.2$ V; $V_{IL} < 0.2$ V
    $\overline{WE}$ — $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}

Waveforms of Read Cycle



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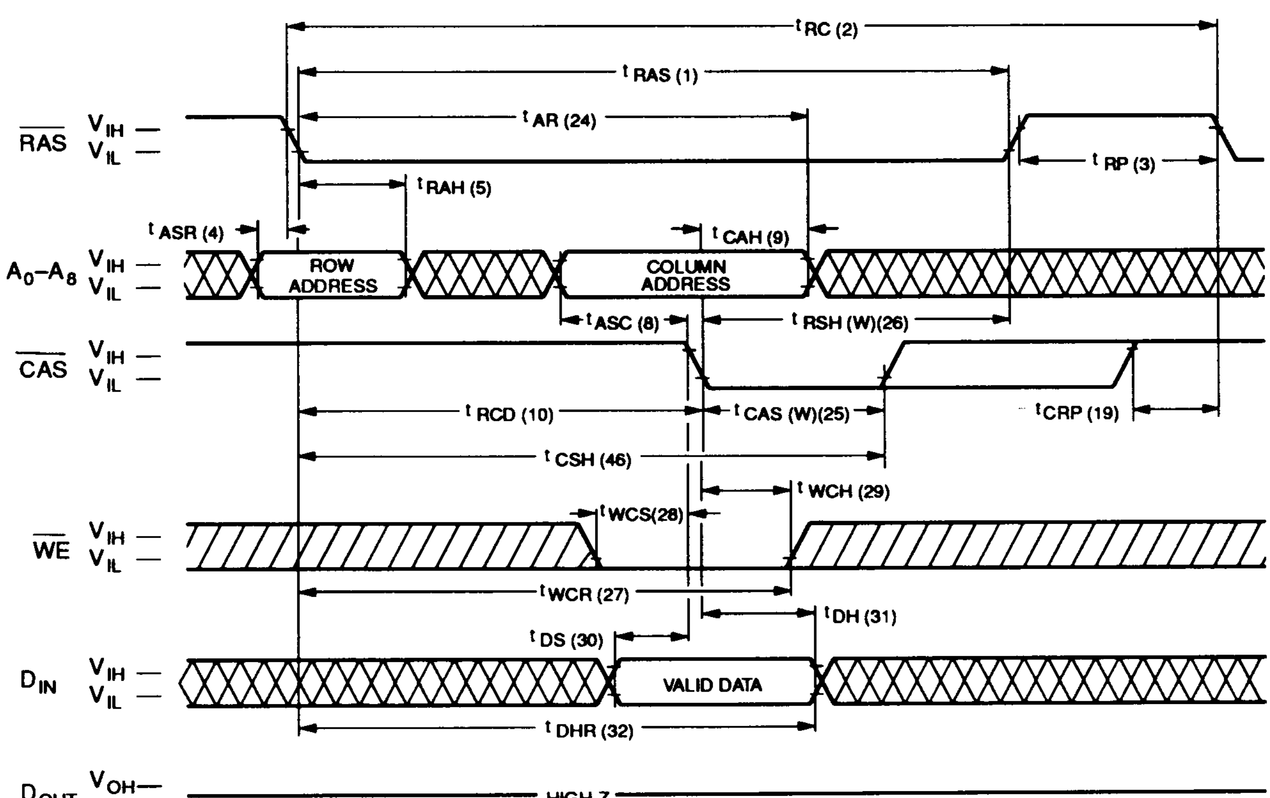
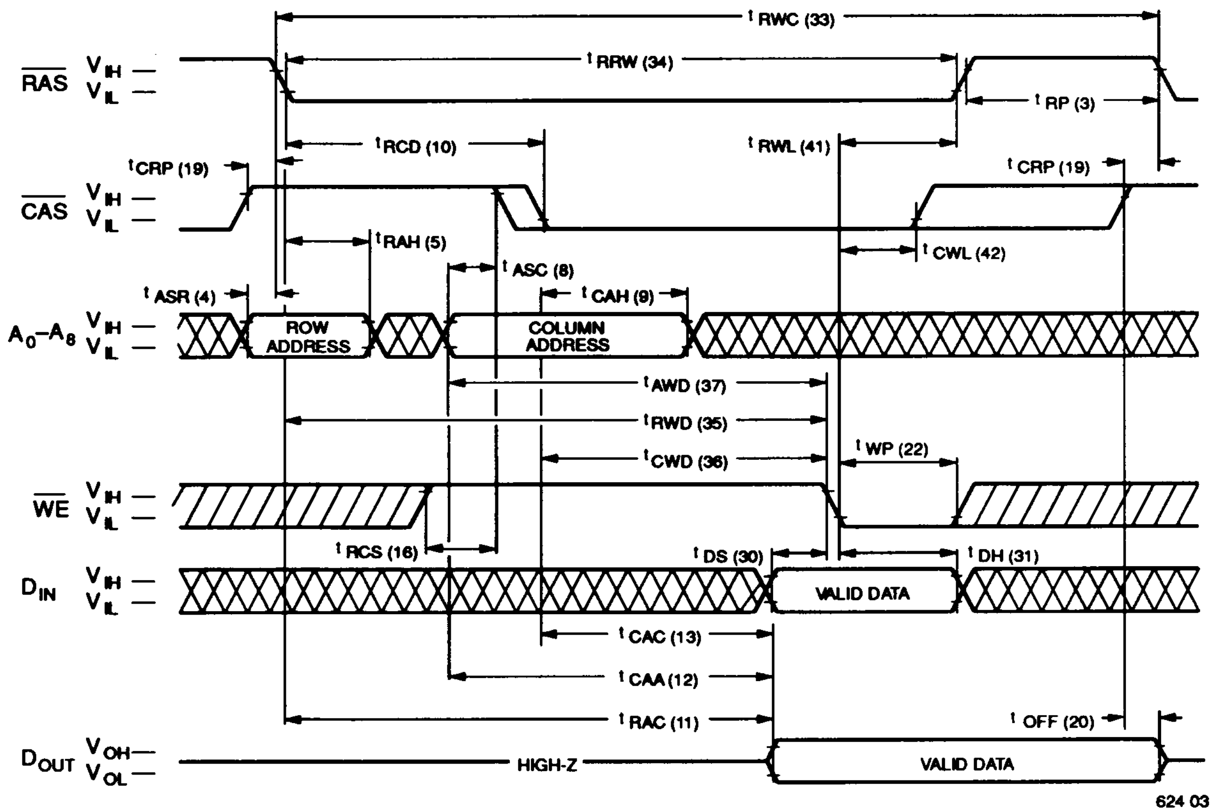
Waveforms of Early Write Cycle

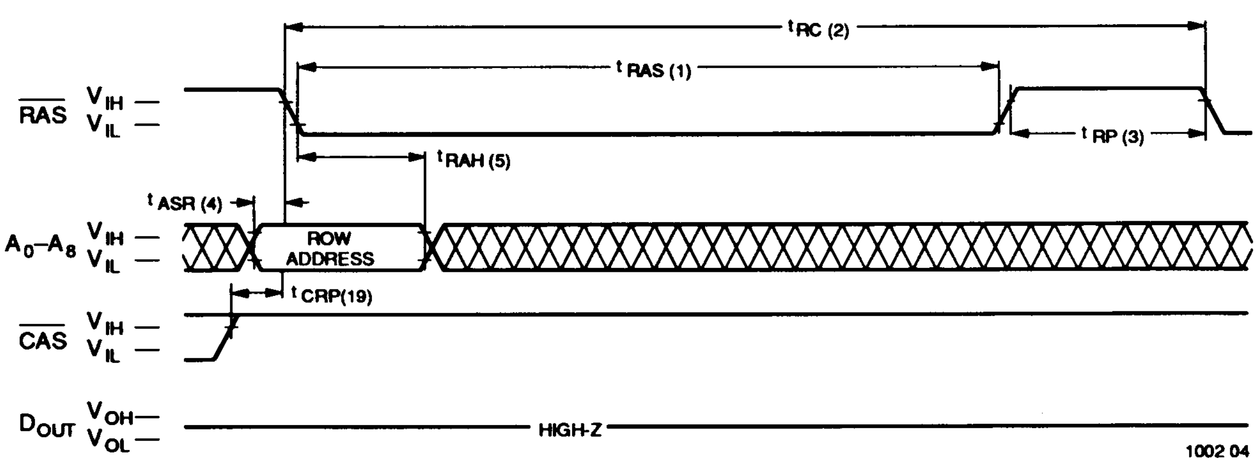


1002 02

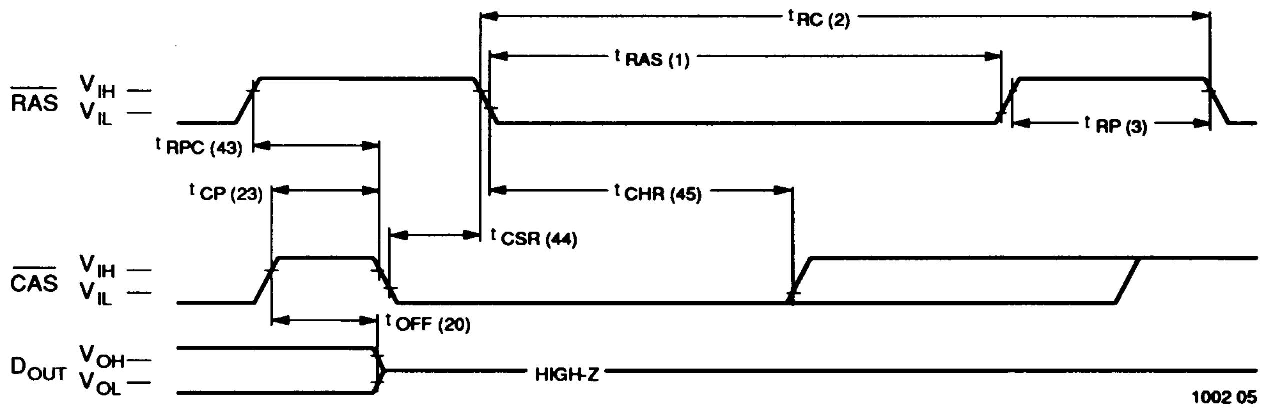
Waveforms of Read-Modify-Write Cycle



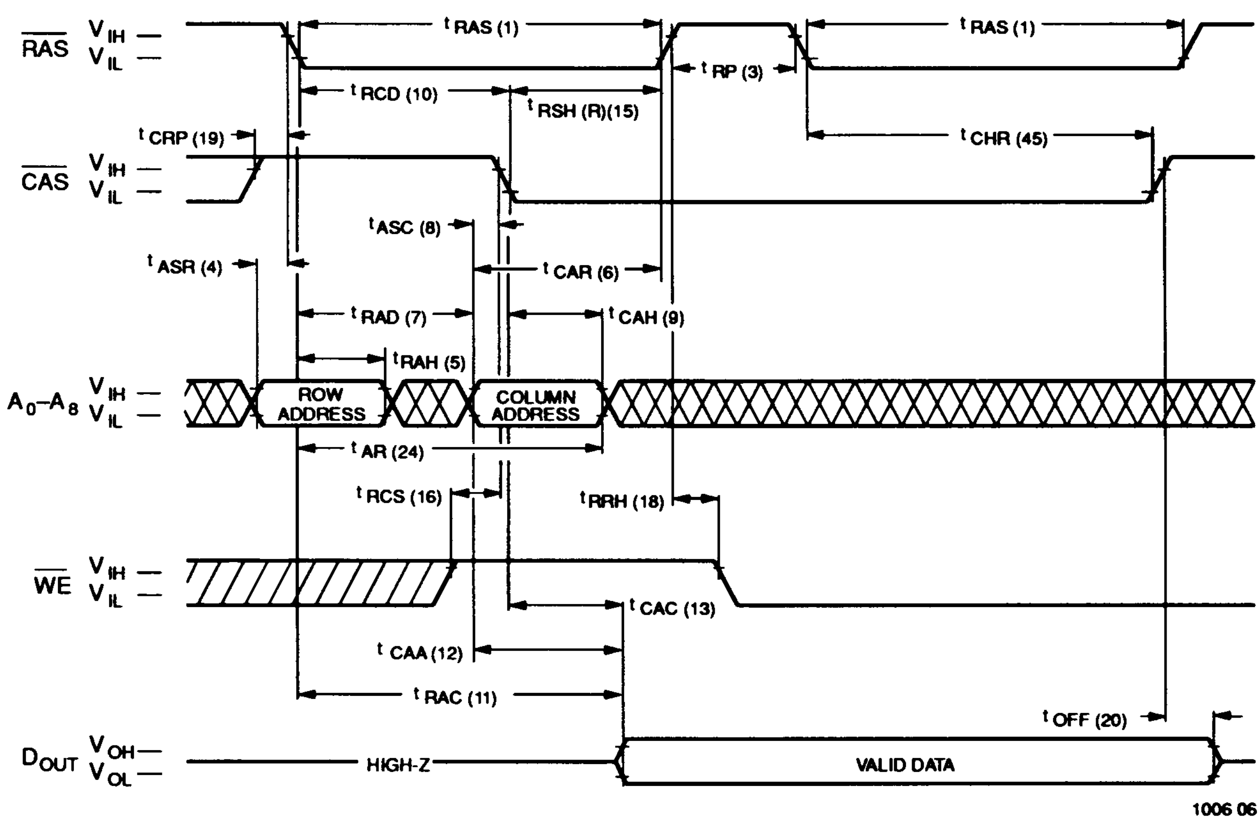
Waveforms of $\overline{RAS}$-Only Refresh Cycle



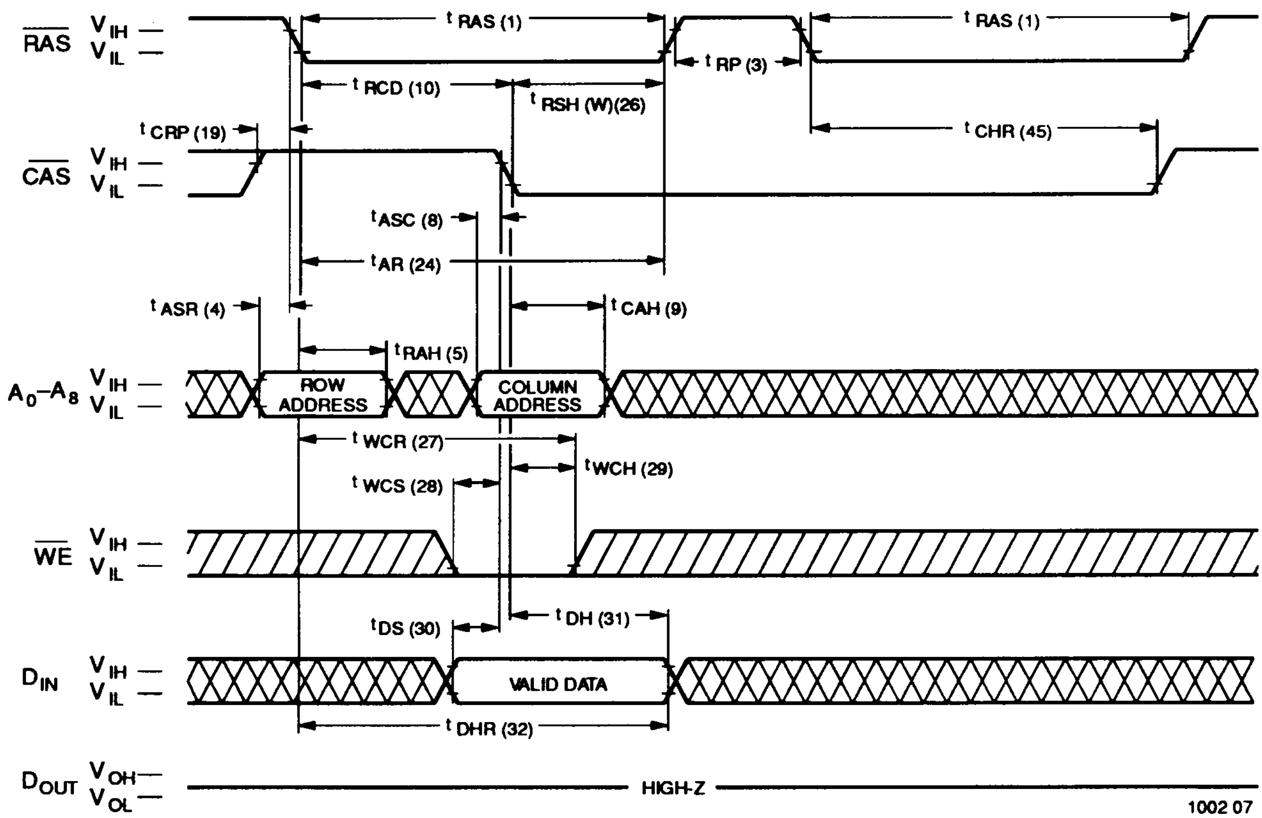
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



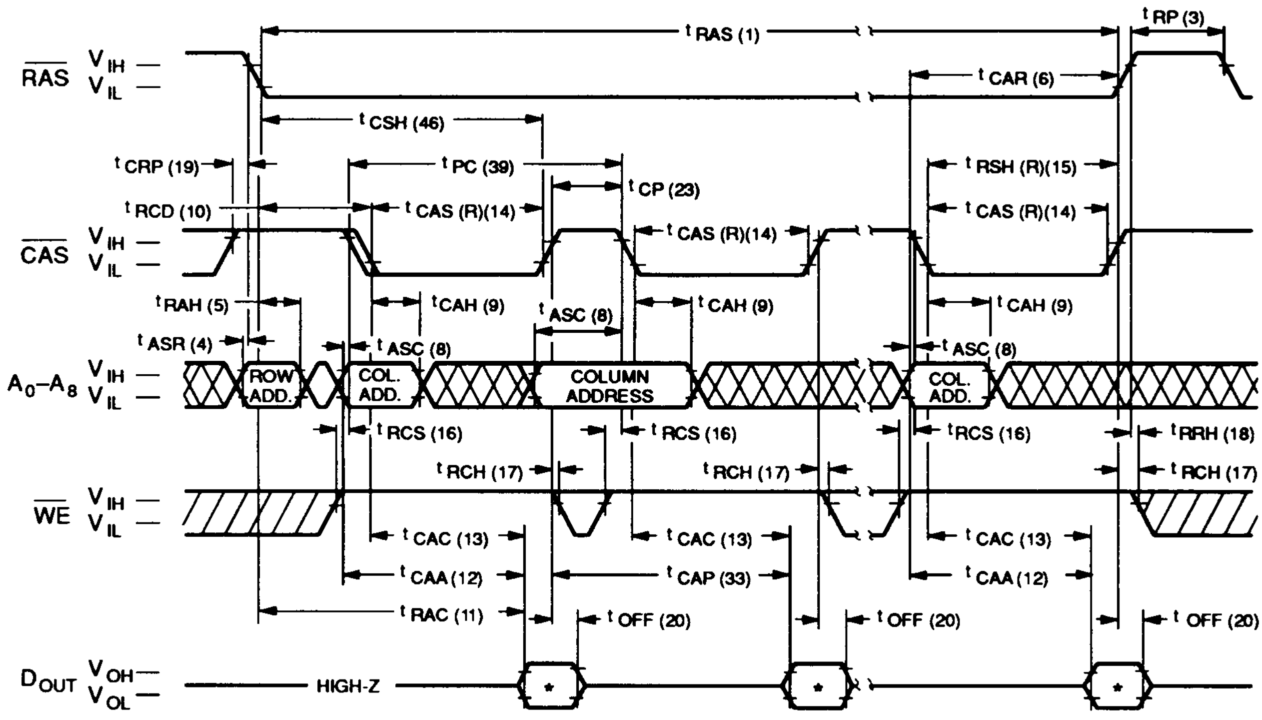
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)

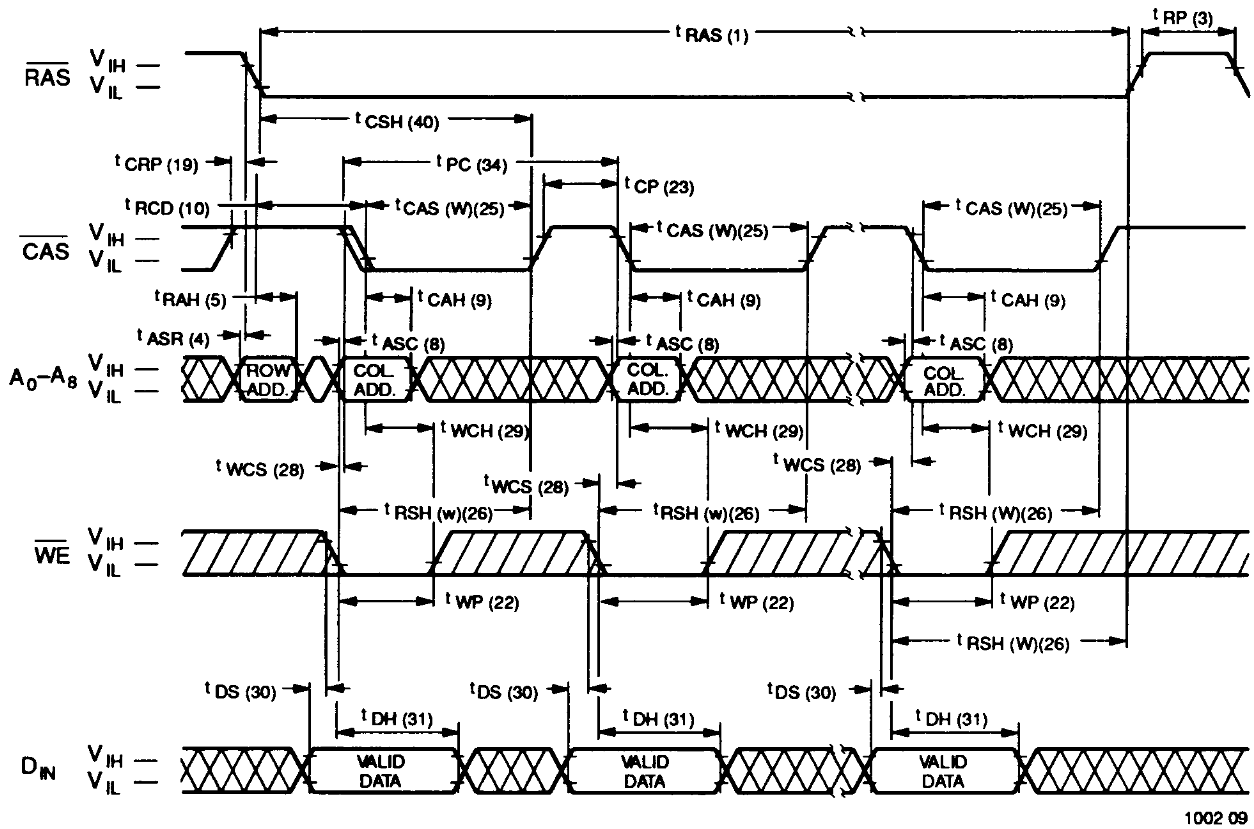


Waveforms of Fast Page Mode Read Cycle

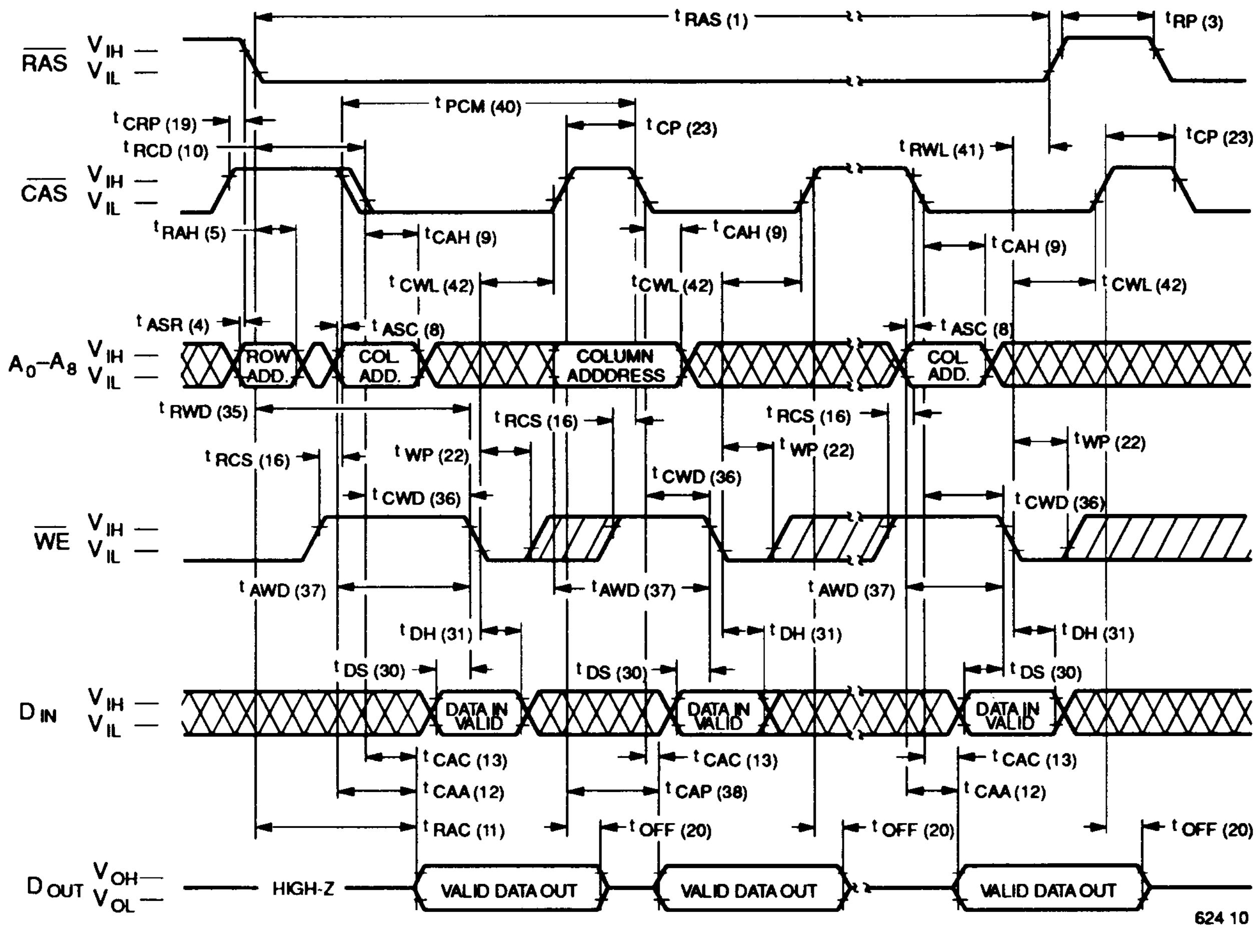


* Valid Data

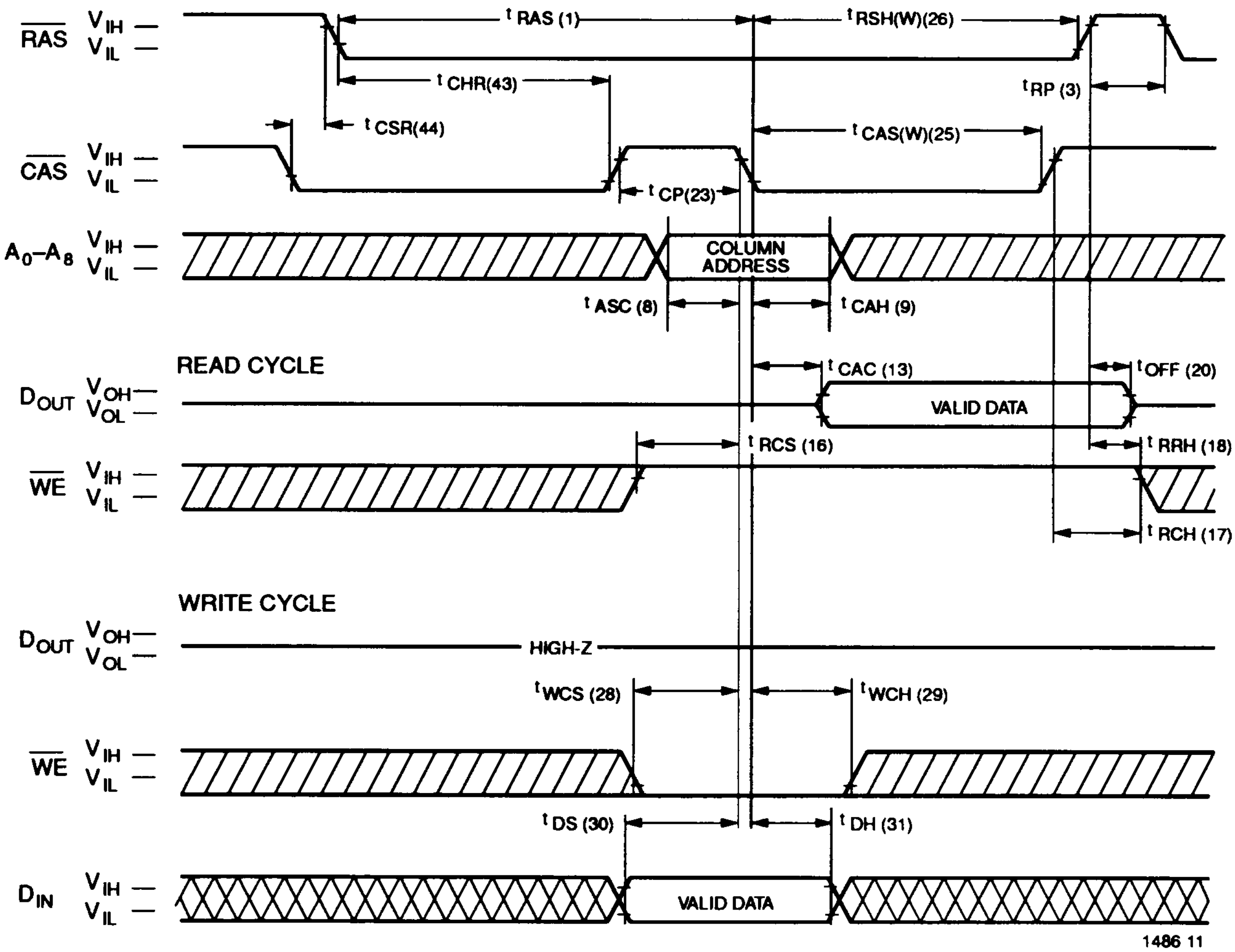
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Modify-Write Cycle



Waveforms of Refresh Counter Test Cycle



Functional Description

The V53C100B is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C100B reads and writes data by multiplexing a 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to Refresh the memory:

1. By selecting all 512 address combinations of A0 through A8 each 8 ms, a refresh of all rows is completed. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C100B will use the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (512 Write cycles) and then verify the written data by applying 512 consecutive Read cycles. In this mode, the V53C100B ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C100B offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C100B power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read, Write, Read-Modify-Write, or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the by the $\overline{CAS}$ rising edge. If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 25 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{1{,}024}{t_{RC} + 1{,}023 \times t_{PC}}$$

Data Output Operation

The V53C100B Data Output pin (D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

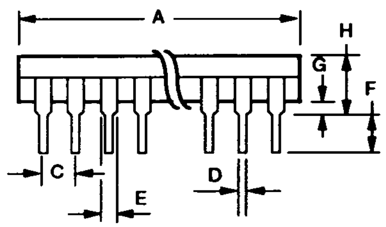
Power On

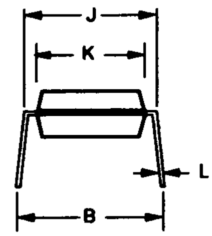
After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval). During power on, the V_{DD} current requirement of the V53C100B is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

Table 1. Vitelic V53C100B Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

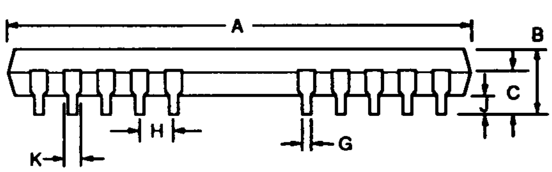
Package Outline

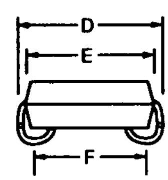




18-pin 300 mil Plastic DIP

Dimension	Inches	Millimeters
A	0.920 Max.	23.368 Max.
B	0.320/0.370	8.128/9.398
C	0.100 Typ.	2.54 Typ.
D	0.018/0.024	0.457/0.610
E	0.048/0.054	1.219/1.372
F	0.110/0.140	2.794/3.556
G	0.005/0.050	0.127/1.270
H	0.180 Max.	4.572 Max.
J	0.300/0.330	7.62/8.382
K	0.280/0.300	7.112/7.620
L	0.008/0.013	0.20/0.33





26/20-pin SOJ

Dimension	Inches	Millimeters
A	0.672/0.684	17.069/17.374
B	0.125/0.135	3.175/3.429
C	0.082/0.093	2.083/2.362
D	0.332/0.342	8.433/8.687
E	0.296/0.304	7.518/7.722
F	0.255/0.275	6.477/6.985
G	0.018 Typ.	0.457 Typ.
H	0.05 Typ.	1.270 Typ.
J	0.026 Min.	0.660 Min.
K	0.028 Typ.	0.711 Typ.

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Printed in U.S.A.

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