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Migrating from LXT325 to LXT336 Quad Receiver

Application Note

January 2001

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1.0	Introduction					
	1.1	Major Differences	.5			
		Pin Comparisons				
	1.3	Applications	.5			
		1.3.1 Migrating to LXT336 Receiver Mode of Operation				
		1.3.2 LXT336 Monitoring Mode of Operation1	1			

Figures

1	LXT325 Receiver Mode Applications	8
	LXT336 Receiver Mode Applications	
	LXT325 Monitor Application	
	LXT336 Monitor Application	

Tables

1	Pinout Cross-Mapping from the LXT325 to the LXT336	6
2	LXT336 Configuration in T1 Receiver Mode of Operation	10
3	LXT336 Configuration in E1 Receiver Mode of Operation	11
4	LXT336 Configuration In T1 Monitoring Mode of Operation	14
5	LXT336 Configuration in E1 Monitoring Mode of Operation	15

Revision History

Revision	Date	Description
-002	03/06/01	Modified Figures 2 & 4. Modified LXT336 QFP pin #18 description Tables 1, 3 & 5.

1.0 Introduction

This Application Note provides information to convert an existing LXT325 based design to the LXT336. The LXT325 was the first Intel Quad Receiver for both T1 and E1 applications. The LXT336 is a new quad T1/E1 receiver with some additional features that are not available on the LXT325.

Due to pin-out and functional differences between the LXT325 and LXT336, migration will require redesigning of the PCB

1.1 Major Differences

- The LXT336 offers both bipolar and unipolar mode, the LXT325 works in bipolar mode only.
- The LXT336 offers selectable AMI/HDB3 decoders, the LXT325 offers AMI decoding only.
- Both devices have a pin called MODE. However, the operation of this pin is different for each device. Refer to the data sheets for details.
- Receiver slicer ratio is selectable on the LXT325 (with MODE pin), on the LXT336 slicer ratio is fixed to 50% for E1 and to 70% for T1 applications.
- LOS criteria are different for the LXT336 and the LXT325. The LXT336 LOS complies with the most recent standards; the LXT325 does not.
- Package size is different for each device. The LXT325 comes in 28 pin DIP, 28pin PLCC and 44 pin QFP packages. The LXT336 is only available in a 64-pin QFP package.

1.2 Pin Comparisons

Table 1 provides a complete pin comparison between the LXT325 and the LXT336 to facilitate migration. It lists the signals available on the LXT325 and the corresponding (equivalent) signals on the LXT336. Due to its increased functionality, the LXT336 has more I/O pins than the LXT325.

1.3 Applications

Table 2 through Table 5 list the LXT336 pin configuration for each of its four major applications:

- T1 Receiver mode
- T1 Monitoring mode
- E1 Receiver mode
- E1 Monitoring mode

The LXT336 meets or exceeds the performance of the LXT325 when used in the recommended configurations. Figure 1 through Figure 4 show how to couple the device to the line and other details the designer should be aware of when converting from the LXT325 to the LXT336.



Note: There are significant differences in line coupling transformer requirements and other external components for both receiver and monitoring applications. Refer to the LXT325 and LXT336 data sheets for details.

		LXT325		LXT336			
Pin Number		Pin Number					
DIP	PLCC	QFP	Pin Name	QFP	Pin Name	Description/Comments	
1	2	8	RPOS1	63	RPOS0/ RDATA0	Receiver 1, Receive Positive Data Output.	
2	3	9	RNEG1	62	RNEG0/BPV0	Receiver 1, Receive Negative Data Output.	
3	4	10	RCLK1	64	RCLK0	Receiver 1, Receive Clock Output.	
4	5	13	RPOS2	60	RPOS1/ RDATA1	Receiver 2, Receive Positive Data Output.	
5	6	14	RNEG2	59	RNEG1/BPV1	Receiver 2, Receive Negative Data Output.	
6	7	15	RCLK2	61	RCLK1	Receiver 2, Receive Clock Output.	
7	8	16	LOS3	27	LOS2	Receiver 3, Loss of Signal Output.	
8	9	19	RPOS3	53	RPOS2/ RDATA2	Receiver 3, Receive Positive Data Output.	
9	10	20	RNEG3	52	RNEG2/BPV2	Receiver 3, Receive Negative Data Output.	
10	11	21	RCLK3	54	RCLK2	Receiver 3, Receive Clock Out- put.	
11	12	24	RPOS4	50	RPOS3/ RDATA3	Receiver 4, Receive Positive Data Output.	
12	13	25	RNEG4	49	RNEG3/BPV3	Receiver 4, Receive Negative Data Output.	
13	14	26	RCLK4	51	RCLK3	Receiver 4, Recovered Clock Output.	
14	15	27, 28	GND	3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46	GND	Ground.	
15	16	30	MCLK	1	MCLK	Master Clock Input.	
16	17	31	MODE	-	-	Mode Selection Input. This pin on LXT325 selects 50% or 70% slicer ratio. On the LXT336 the slicer ratio is set to 50% for E1 and 70% for T1 operation.	
17	18	32	RTIP4	29	RTIP3	Receiver 4, Receive TIP Input.	
18	19	35	RRING4	28	RRING3	Receiver 4, Receive RING Input.	
19	20	36	LOS4	30	LOS3	Receiver 4, Loss of Signal Output	
20	21	37	RTIP3	26	RTIP2	Receiver 3, Receive TIP Input.	
21	22	38	RRING3	25	RRING2	Receiver 3, Receive RING Input.	

Table 1. Pinout Cross-Mapping from the LXT325 to the LXT336



		LXT325				LXT336
Pin Number			Pin Name	Pin Number		Description/Comments
DIP	PLCC	QFP	Pin Name	QFP	Pin Name	Description/Comments
22	23	40	LOS2	24	LOS1	Receiver 2, Loss of Signal Output.
23	24	41	RTIP2	23	RTIP1	Receiver 2, Receive TIP Input.
24	25	42	RRING2	22	RRING1	Receiver 2, Receive RING Input.
25	26	2	LOS1	21	LOS0	Receiver 1, Loss of Signal Output.
26	27	3	RTIP1	20	RTIP0	Receiver 1, Receive TIP Input.
27	28	4	RRING1	19	RRING0	Receiver 1, Receive RING Input.
28	1	5, 6	VCC	11, 15, 34, 38, 41	VCC	Positive (+5V) supply.
-	-	-	-	18	MODE	Mode Select Input. Refer to the LXT336 data sheet for details. Tie this pin to GND for E1 AMI operation, High for E1 - HDB3 operation or connect it to 2.5V for T1 operation.
-	-	-	-	4 7 42 45	UBS0 UBS1 UBS2 UBS3	Receiver 1, 2, 3, and 4 - Unipolar- Bipolar Select Input. These Inputs are available only on the LXT336. Connect to GND.
-	-	-	-	32	CLKE	Clock Edge Select Input. Tie pin to VCC through a 10 k Ω resistor.
-	-	-	-	2 5 44 47	CLKI0 CLKI1 CLKI2 CLKI3	CLOCK Input Receiver1, 2, 3, and 4. Connected to GND when migrating from LXT325 to LXT336.
-	-	1, 7, 11, 12,17, 18, 22, 23, 29, 33, 34, 39, 43, 44	NC-not connected	9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC-not connected	All NC pins must be left open (not connected).

Table 1.	Pinout Cross-Mapping from the LXT325 to the LXT336	(Continued)
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1.3.1 Migrating to LXT336 Receiver Mode of Operation

Figure 1 and Figure 2 show the LXT325 and the LXT336 configured for receiver mode of operation. Note the differences between the LXT325 and the LXT336. The following signals are significant: MODE, CLKI, UBS and CLKE. Table 2 specifies the pin-out to configure the LXT336 for T1 receiver mode. Table 4 specifies the pin-out to configure the LXT336 for E1 receiver mode.



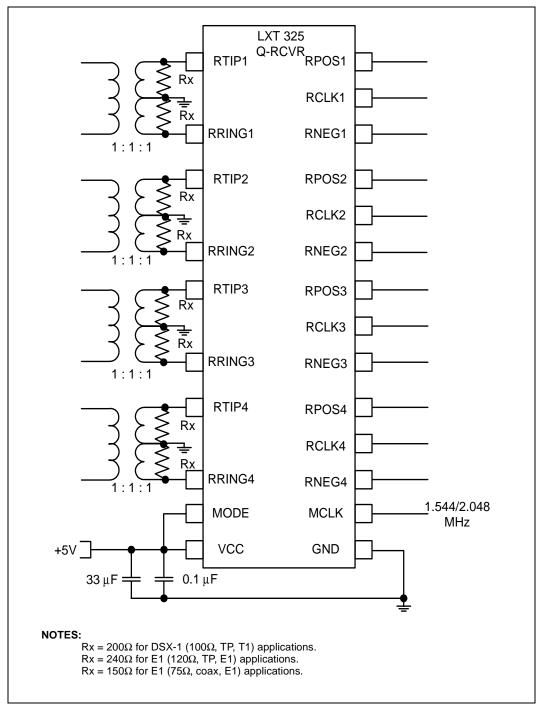


Figure 1. LXT325 Receiver Mode Applications

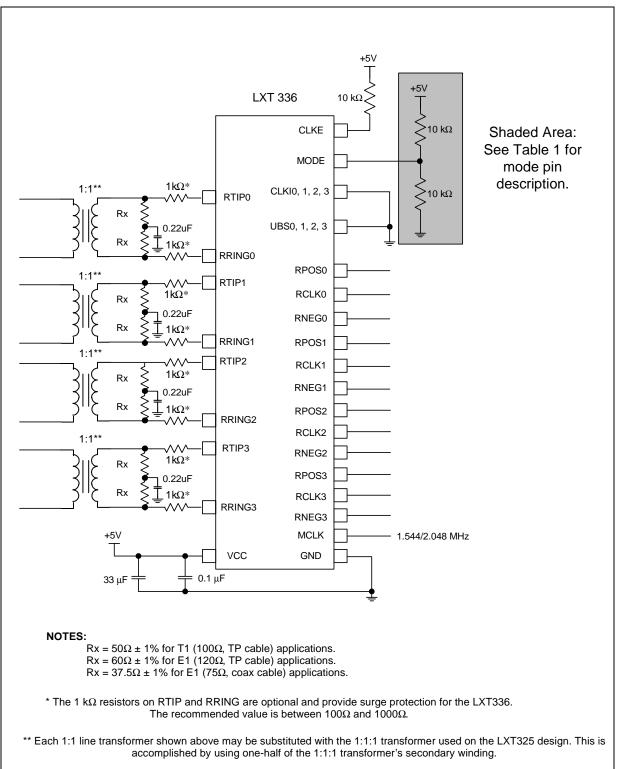


Figure 2. LXT336 Receiver Mode Applications



Pin#SymbolVODescription1MCLKDIMaster Clock. Supply 1.544 MHz clock.2, 5, 44, 47CLKI0, 1, 2, 3DIConnect to ground.3, 6, 81, 0, 14, 17, 31, 35, 39, 43, 44GNDSConnect to ground.4, 7, 42, 45UBS0, 1, 2, 3DIConnect to ground.9, 12, 13, 16, 33, 36, 37, 40, 48, 55NCNot Connected.6, 65, 75, 85NCS45V power supply.11, 15, 34, 38, 41,VCCS45V power supply.18MODEDIMode Select Input. Connect this input to 2.5V signal. See Figure 2.19RRING0AI20RTIP0AI21RRING1AI22RRING2AI23RTIP1AI24RRING2AI25RRING2AI26RTIP2AI27LOS2DO28RRING3AI29RTIP3AI21LOS0DO24LOS1DO25RROS1DO363RPOS0DO264RPOS1DO275LOS2DO286RRING3AI29RTIP3AI20RCINE3DO21LOS0DO22LOS3DO23RCINE3DO24LOS1DO25RRING3DO36RPOS0DO2				
2, 5, 44, 47CLKI0, 1, 2, 3DIConnect to ground.3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46GNDSConnect to power supply Ground.4, 7, 42, 45UBS0, 1, 2, 3DIConnect to ground.9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58NC-Not Connected.111, 15, 34, 38, 41,VCCS $+5V$ power supply.18MODEDIMode Select Input. Connect this input to 2.5V signal. See Figure 2.19RRING0AI 22RRING120RTIP0AI 23RRING221RRING2AI 24RRING226RTIP2AI 25RRING327LOS0DO 24Loss of Signal Port 0.28RRING3AI 2929RTIP3AI21LOS0DO Loss of Signal Port 0.24LOS1DO Loss of Signal Port 0.25RRING3DO Loss of Signal Port 1.26RTIP3AI21LOS0DO Loss of Signal Port 2.30LOS3DO Loss of Signal Port 3.31CLKEDI32CLKEDI33RPOS0DO Receive Positive Data Port 1 (Port 2 per LXT325).60RPOS1DO Receive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DO Receive Positive Data Port 1 (Port 2 per LXT325).50RPOS3DO Receive Positive Data Port 2 (Port 3 per LXT325).51RRIG3DO Receive Positive Data Port	Pin#	Symbol	I/O	Description
3. 6, 8, 10, 14, 17, 31, 35, 39, 43, 46GNDSConnect to power supply Ground.4, 7, 42, 45UBS0, 1, 2, 3DIConnect to ground.9, 12, 13, 16, 33, 6, 57, 58NC-Not Connected.11, 15, 34, 38, 41,VCCS+5V power supply.18MODEDIMode Select Input. Connect this input to 2.5V signal. See Figure 2.19RRINGOAI 22RRING120RTIPOAI 23RTIP123RTIP1AI 41Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2, 3, and 4 per LXT325).26RTIP2AI 4129RTIP3AI21LOS0DO Loss of Signal Port 0.24LOS1DO Loss of Signal Port 1.25RRING2DO Loss of Signal Port 1.26RTIP3AI27LOS2DO Loss of Signal Port 1.28RRING3DO Loss of Signal Port 1.29RTIP3AI21LOS0DO Loss of Signal Port 3.32CLKEDI33Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS1DO Receive Positive Data Port 0 (Port 1 per LXT325).60RPOS1DO Receive Negative Data Port 1 (Port 2 per LXT325).53RNEG2DO Receive Negative Data Port 2 (Port 3 per LXT325).54RNEG3DO Receive Negative Data Port 3 (Port 4 per LXT325).55RNEG3DO Receive Negative Data Port 3 (Port 4 per LXT325)	1	MCLK	DI	Master Clock. Supply 1.544 MHz clock.
31, 35, 39, 43, 46GNDSConnect to power suppry Ground.4, 7, 42, 45UBS0, 1, 2, 3DIConnect to ground.9, 12, 13, 16, 33, 36, 37, 40, 48, 55,NC-Not Connected.111, 15, 34, 38, 41,VCCS+5V power supply.18MODEDIMode Select Input. Connect this input to 2.5V signal. See Figure 2.19RRINGOAI20RTIPOAI21RRING1AI22RRING2AI23RTIP1AI24RRING3AI25RRING3AI26RTIP2AI27LOS0DO28RRING3AI29RTIP3AI21LOS0DO24LOS1DO27LOS2DO28RNEG0DO29RTIP3AI21LOS0DO23LOS3DO24LOS1DO25RNEG0DO26RDE2DO27LOS2DO28RRING339CLKEDI29RD120Coss of Signal Port 3.31RPOS0DO26RNEG027LOS230LOS331ROS132CLKE33RPOS244DO45Receive Negative Data Port 1 (Port 2 per LXT325).52RNEG3 <td>2, 5, 44, 47</td> <td>CLKI0, 1, 2, 3</td> <td>DI</td> <td>Connect to ground.</td>	2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to ground.
9 12 13 16 17 Not Connected. 36, 37, 40, 48, 55, 56, 57, 58 NC - Not Connected. 11, 15, 34, 38, 41, 38, 41, 38, 41, 38, 41, 38, 41, 38, 41, 39, 38, 41, 39, 38, 41, 30, 41, 41, 41, 41, 41, 41, 41, 41, 41, 41		GND	S	Connect to power supply Ground.
36, 37, 40, 48, 55, 56, 57, 58NC-Not Connected.11, 15, 34, 38, 41,VCCS+5V power supply.18MODEDIMode Select Input. Connect this input to 2.5V signal. See Figure 2.19RRING0AI20RTIPOAI21RRING1AI22RRING2AI23RTIP1AI26RTIP2AI27RRING2AI28RRING3AI29RTIP3AI21LOS0DOLoss of Signal Port 0.24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 3.28RRING3DOLoss of Signal Port 3.29RTIP3AIPost Signal Port 3.21LOS0DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.33RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).54RNEG3DOReceive Negative Data Port 2 (Port 3 per LXT325).55RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).56RNEG3DOReceive Negative Data Port 2 (Port 3 per LXT325).57RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).58RNEG3 <t< td=""><td>4, 7, 42, 45</td><td>UBS0, 1, 2, 3</td><td>DI</td><td>Connect to ground.</td></t<>	4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to ground.
38, 41,VCCS+5V power supply.18MODEDIMode Select Input. Connect this input to 2.5V signal. See Figure 2.19RRING0AI20RTIP0AI22RRING1AI23RTIP1AI24RRING2AI26RTIP2AI26RTIP3AI27LOS0DO28RRING3AI29RTIP3AI21LOS0DO24LOS1DOLoS2DOLoss of Signal Port 0.23LOS3DO24LOS1DOLoS2DOLoS2DOLoS3DOLoS4Genero Positive Data Port 0 (Port 1 per LXT325).63RPOS0DORNEG0DOReceive Positive Data Port 1 (Port 2 per LXT325).60RPOS1DORNEG1DOReceive Positive Data Port 1 (Port 2 per LXT325).53RPOS2DO64RCLK0DO8Receive Negative Data Port 2 (Port 3 per LXT325).64RCLK0DO64RCLK1DO8Receive Clock Output Port 1 (Port 2 on LXT325).61RCLK1DO8Receive Clock Output Port 1 (Port 2 on LXT325).64RCLK1DO8Receive Clock Output Port 1 (Port 2 on LXT325).64RCLK1DO8Receive Clock Output Port 1 (Port 2 on LXT325)	36, 37, 40, 48, 55,	NC	-	Not Connected.
19RRING0AI19RTIP0AI20RTIP0AI22RRING1AI23RTIP1AI25RRING2AI26RTIP2AI28RRING3AI29RTIP3AI21LOS0DO24LOS1DO27LOS2DO28CLKEDI29CLKEDI20LOS3DO24LOS1DO25RNEG0DO26ROS3DO27LOS2DO28LOS330LOS331DO29RTIP332CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS060RPOS150RPOS251RNEG152RNEG253RPOS254RNEG355RNEG356RPOS357RNEG358ROS359RNEG350RPOS351RNEG352RNEG353ROS354ROLK155ROLK156ROLK157ROLK158ROLK159ROLS350ROS350ROS350ROS350ROLS350ROLK150 <td></td> <td>VCC</td> <td>S</td> <td>+5V power supply.</td>		VCC	S	+5V power supply.
20RTIP0AI22RRING1AI23RTIP1AI23RTIP1AI25RRING2AI26RTIP2AI28RRING3AI29RTIP3AI21LOS0DOLoss of Signal Port 0.24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Negative Data Port 1 (Port 2 per LXT325).54RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).55RNEG1DOReceive Negative Data Port 2 (Port 3 per LXT325).56RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).55RNEG2DOReceive Negative Data Port 3 (Port 4 per LXT325).56RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	18	MODE	DI	Mode Select Input. Connect this input to 2.5V signal. See Figure 2.
22RRING1AI AI RTIP1Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2, 3, and 4 per LXT325).26RTIP2AI RRING3(Port 1, 2, 3, and 4 per LXT325).26RTIP2AI RRING3AI29RTIP3AI21LOS0DO Loss of Signal Port 0.24LOS1DO LOS2Loss of Signal Port 1.27LOS2DO LOS3Loss of Signal Port 3.30LOS3DO LOS3Loss of Signal Port 3.32CLKEDI Receive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DO Receive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DO Receive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DO Receive Negative Data Port 2 (Port 3 per LXT325).54RNEG2DO Receive Negative Data Port 2 (Port 3 per LXT325).55RNEG2DO Receive Negative Data Port 3 (Port 4 per LXT325).50RPOS3DO Receive Negative Data Port 3 (Port 4 per LXT325).50RPOS3DO Receive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DO Receive Clock Output Port 0 (Port 1 on LXT325).64RCLK0DO Receive Clock Output Port 1 (Port 2 on LXT325).61RCLK1DO62RCLK1DO63RCLK0DO74Receive Clock Output Port 1 (Port 2 on LXT325).64RCLK0DO75Receive Clock Output Port 1 (Port 2 on LXT325).64RCLK1<	19	RRING0	AI	
23RTIP1 RRING2AI AI RRING2Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2, 3, and 4 per LXT325).26RTIP2 RTIP3AI28RRING3 RTIP3AI29RTIP3AI21LOS0DO Loss of Signal Port 0.24LOS1DO LOS2Loss of Signal Port 1.27LOS2DO Loss of Signal Port 2.30LOS3DO Loss of Signal Port 3.32CLKEDI Receive Positive Data Port 0 (Port 1 per LXT325).63RPOS0 RNEG0DO Receive Negative Data Port 0 (Port 1 per LXT325).60RPOS1 RNEG1DO Receive Positive Data Port 1 (Port 2 per LXT325).53RPOS2 RNEG1DO Receive Positive Data Port 2 (Port 3 per LXT325).54RNEG2DO Receive Negative Data Port 2 (Port 3 per LXT325).55RNEG2DO Receive Positive Data Port 3 (Port 4 per LXT325).50RPOS3 RNEG3DO Receive Negative Data Port 3 (Port 4 per LXT325).50RPOS3 RNEG3DO Receive Negative Data Port 3 (Port 4 per LXT325).64RCLK0 RCLK1DO65RCLK0 RCLK1DO66RCLK1DO67RCLK1DO68RCLK1DO69RCLK1DO60RCLK1DO70Receive Clock Output Port 1 (Port 2 on LXT325).71RCLK0DO72RCLK0DO73RCLK0DO74RCLK0	20	RTIP0	AI	
25RRING2AI (Port 1, 2, 3, and 4 per LXT325).26RTIP2AI 2828RRING3AI 2929RTIP3AI20RTIP3AI21LOS0DO LOS1Loss of Signal Port 0.24LOS1DO LOS2Loss of Signal Port 1.27LOS2DO LOS3Loss of Signal Port 3.30LOS3DO LOS3Loss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DO Receive Positive Data Port 0 (Port 1 per LXT325).60RPOS1DO Receive Negative Data Port 1 (Port 2 per LXT325).59RNEG1DO Receive Positive Data Port 2 (Port 3 per LXT325).53RPOS2DO Receive Positive Data Port 2 (Port 3 per LXT325).50RPOS3DO Receive Positive Data Port 3 (Port 4 per LXT325).50RPOS3DO Receive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DO Receive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DO	22	RRING1	AI	
26RTIP2AI26RTIP3AI29RTIP3AI29RTIP3AI21LOS0DOLoss of Signal Port 0.24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Positive Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Clock Output Port 0 (Port 1 on LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	23	RTIP1	AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3
28RRING3 RTIP3AI29RTIP3AI21LOS0DOLoss of Signal Port 0.24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).50RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Clock Output Port 0 (Port 1 on LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	25	RRING2	AI	(Port 1, 2, 3, and 4 per LXT325).
29RTIP3AI21LOS0DOLoss of Signal Port 0.24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	26	RTIP2	AI	
21LOS0DOLoss of Signal Port 0.24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Positive Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).50RNEG2DOReceive Positive Data Port 3 (Port 4 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	28	RRING3	AI	
24LOS1DOLoss of Signal Port 1.27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	29	RTIP3	AI	
27LOS2DOLoss of Signal Port 2.30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).50RNEG2DOReceive Positive Data Port 3 (Port 4 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	21	LOS0	DO	Loss of Signal Port 0.
30LOS3DOLoss of Signal Port 3.32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	24	LOS1	DO	Loss of Signal Port 1.
32CLKEDIClock Edge Select Input. Pull this pin High using a 10k Ω resistor.63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).50RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	27	LOS2	DO	Loss of Signal Port 2.
63RPOS0DOReceive Positive Data Port 0 (Port 1 per LXT325).62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Negative Data Port 3 (Port 4 per LXT325).50RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	30	LOS3	DO	Loss of Signal Port 3.
62RNEG0DOReceive Negative Data Port 0 (Port 1 per LXT325).60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).50RNEG3DOReceive Positive Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
60RPOS1DOReceive Positive Data Port 1 (Port 2 per LXT325).59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).50RNEG3DOReceive Positive Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	63	RPOS0	DO	Receive Positive Data Port 0 (Port 1 per LXT325).
59RNEG1DOReceive Negative Data Port 1 (Port 2 per LXT325).53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	62	RNEG0	DO	Receive Negative Data Port 0 (Port 1 per LXT325).
53RPOS2DOReceive Positive Data Port 2 (Port 3 per LXT325).52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	60	RPOS1	DO	Receive Positive Data Port 1 (Port 2 per LXT325).
52RNEG2DOReceive Negative Data Port 2 (Port 3 per LXT325).50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	59	RNEG1	DO	Receive Negative Data Port 1 (Port 2 per LXT325).
50RPOS3DOReceive Positive Data Port 3 (Port 4 per LXT325).49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	53	RPOS2	DO	Receive Positive Data Port 2 (Port 3 per LXT325).
49RNEG3DOReceive Negative Data Port 3 (Port 4 per LXT325).64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	52	RNEG2	DO	Receive Negative Data Port 2 (Port 3 per LXT325).
64RCLK0DOReceive Clock Output Port 0 (Port 1 on LXT325).61RCLK1DOReceive Clock Output Port 1 (Port 2 on LXT325).	50	RPOS3	DO	Receive Positive Data Port 3 (Port 4 per LXT325).
61 RCLK1 DO Receive Clock Output Port 1 (Port 2 on LXT325).	49	RNEG3	DO	Receive Negative Data Port 3 (Port 4 per LXT325).
	64	RCLK0	DO	Receive Clock Output Port 0 (Port 1 on LXT325).
54 RCLK2 DO Receive Clock Output Port 2 (Port 3 on LXT325).	61	RCLK1	DO	Receive Clock Output Port 1 (Port 2 on LXT325).
	54	RCLK2	DO	Receive Clock Output Port 2 (Port 3 on LXT325).
51 RCLK3 DO Receive Clock Output Port 3 (Port 4 on LXT325).	51	RCLK3	DO	Receive Clock Output Port 3 (Port 4 on LXT325).

Table 2. LXT336 Configuration in T1 Receiver Mode of Operation

Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 2.048 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to Ground.
3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to Ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11, 15, 34, 38, 41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect to Vcc or Gnd. See Figure 2.
19	RRING0	AI	
20	RTIP0	AI	
22	RRING1	AI	
23	RTIP1	AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3
25	RRING2	AI	(Port 1, 2, 3, and 4 per LXT325).
26	RTIP2	AI	
28	RRING3	AI	
29	RTIP3	AI	
21	LOS0	DO	Loss of Signal Port 0.
24	LOS1	DO	Loss of Signal Port 1.
27	LOS2	DO	Loss of Signal Port 2.
30	LOS3	DO	Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63	RPOS0	DO	Receive Positive Data Port 0 (Port 1 per LXT325).
62	RNEG0	DO	Receive Negative Data Port 0 (Port 1 per LXT325).
60	RPOS1	DO	Receive Positive Data Port 1 (Port 2 per LXT325).
59	RNEG1	DO	Receive Negative Data Port 1 (Port 2 per LXT325).
53	RPOS2	DO	Receive Positive Data Port 2 (Port 3 per LXT325).
52	RNEG2	Do	Receive Negative Data Port 2 (Port 3 per LXT325).
50	RPOS3	DO	Receive Positive Data Port 3 (Port 4 per LXT325).
49	RNEG3	DO	Receive Negative Data Port 3 (Port 4 per LXT325).
64	RCLK0	DO	Receive Clock Output Port 0 (Port 1 on LXT325).
61	RCLK1	DO	Receive Clock Output Port 1 (Port 2 on LXT325).
54	RCLK2	DO	Receive Clock Output Port 2 (Port 3 on LXT325).
51	RCLK3	DO	Receive Clock Output Port 3 (Port 4 on LXT325).

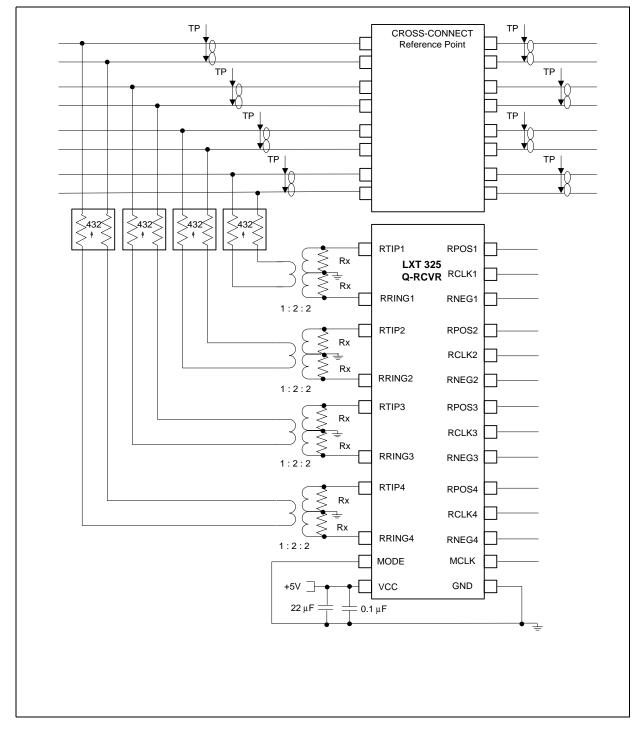
Table 3. LXT336 Configuration in E1 Receiver Mode of Operation

1.3.2 LXT336 Monitoring Mode of Operation

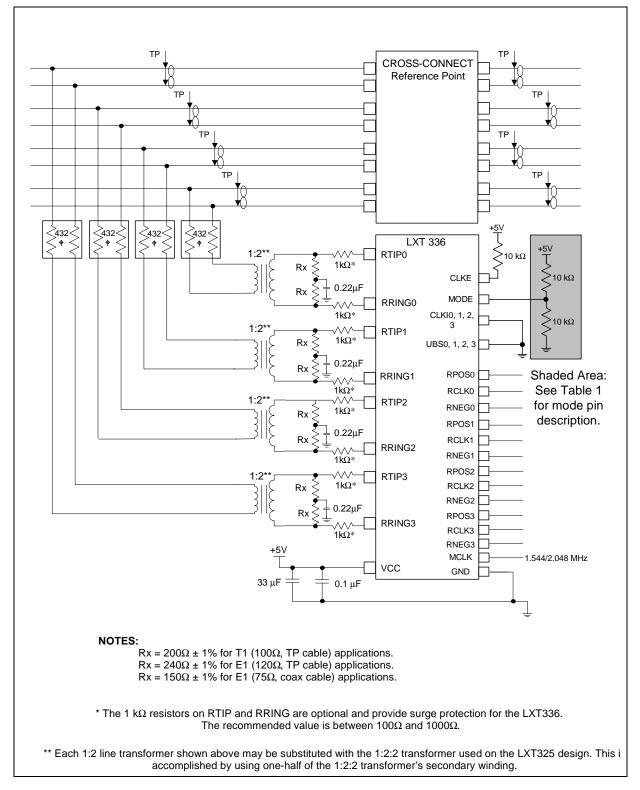
Figure 3 and Figure 4 show the LXT325 and the LXT336 configured for monitor mode of operation. Note the differences between the LXT325 and the LXT336. The following signals are significant: MODE, CLKI, UBS and CLKE. Table 4 specifies the pin-out to configure the LXT336 for T1 monitor mode. Table 5 specifies the pin-out to configure the LXT336 for E1 monitor mode.



Figure 3. LXT325 Monitor Application









Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 1.544 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to Ground.
3, 6, 8, 10, 14, 17,31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to Ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11,15,34, 38,41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect this input to 2.5V. See Figure 4.
19	RRING0	AI	
20	RTIP0	AI	
22	RRING1	AI	
23	RTIP1	AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3
25	RRING2	AI	(Port 1, 2, 3, and 4 per LXT325).
26	RTIP2	AI	
28	RRING3	AI	
29	RTIP3	AI	
21	LOS0	DO	Loss of Signal Port 0.
24	LOS1	DO	Loss of Signal Port 1.
27	LOS2	DO	Loss of Signal Port 2.
30	LOS3	DO	Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63	RPOS0	DO	Receive Positive Data Port 0 (Port 1 per LXT325).
62	RNEG0	DO	Receive Negative Data Port 0 (Port 1 per LXT325).
60	RPOS1	DO	Receive Positive Data Port 1 (Port 2 per LXT325).
59	RNEG1	DO	Receive Negative Data Port 1 (Port 2 per LXT325).
53	RPOS2	DO	Receive Positive Data Port 2 (Port 3 per LXT325).
52	RNEG2	DO	Receive Negative Data Port 2 (Port 3 per LXT325).
50	RPOS3	DO	Receive Positive Data Port 3 (Port 4 per LXT325).
49	RNEG3	DO	Receive Negative Data Port 3 (Port 4 per LXT325).
64	RCLK0	DO	Receive Clock Output Port 0 (Port 1 on LXT325).
61	RCLK1	DO	Receive Clock Output Port 1 (Port 2 on LXT325).
54	RCLK2	DO	Receive Clock Output Port 2 (Port 3 on LXT325).
51	RCLK3	DO	Receive Clock Output Port 3 (Port 4 on LXT325).

 Table 4.
 LXT336 Configuration In T1 Monitoring Mode of Operation

Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 2.048 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to Ground.
3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to Ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11, 15, 34, 38, 41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect this input to Vcc or Gnd. See Figure 4.
19	RRING0	AI	
20	RTIP0	AI	
22	RRING1	AI	
23	RTIP1	AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3
25	RRING2	AI	(Port 1, 2,3, and 4 per LXT325).
26	RTIP2	AI	
28	RRING3	AI	
29	RTIP3	AI	
21	LOS0	DO	Loss of Signal Port 0.
24	LOS1	DO	Loss of Signal Port 1.
27	LOS2	DO	Loss of Signal Port 2.
30	LOS3	DO	Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63	RPOS0	DO	Receive Positive Data Port 0 (Port 1 per LXT325).
62	RNEG0	DO	Receive Negative Data Port 0 (Port 1 per LXT325).
60	RPOS1	DO	Receive Positive Data Port 1 (Port 2 per LXT325).
59	RNEG1	DO	Receive Negative Data Port 1 (Port 2 per LXT325).
53	RPOS2	DO	Receive Positive Data Port 2 (Port 3 per LXT325).
52	RNEG2	DO	Receive Negative Data Port 2 (Port 3 per LXT325).
50	RPOS3	DO	Receive Positive Data Port 3 (Port 4 per LXT325).
49	RNEG3	DO	Receive Negative Data Port 3 (Port 4 per LXT325).
64	RCLK0	DO	Receive Clock Output Port 0 (Port 1 on LXT325).
61	RCLK1	DO	Receive Clock Output Port 1 (Port 2 on LXT325).
54	RCLK2	DO	Receive Clock Output Port 2 (Port 3 on LXT325).
51	RCLK3	DO	Receive Clock Output Port 3 (Port 4 on LXT325).

Table 5.	LXT336 Configuration	n in E1	Monitoring Mode of Operation	

