

BCD-TO-DECIMAL DECODER

GENERAL DESCRIPTION

The MMC 4028 is a BCD-to-decimal or binary-to-decimal decoder. This device is a monolithic IC fabricated in standard Al-gate CMOS technology. MMC 4028 is available in 16-lead dual in line ceramic and plastic package. The MMC 4028 consists of buffering on all four inputs decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of ten decimal decoded outputs. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

FEATURES

- High decoded output drive capability
- Medium speed operation
- „Positive logic“ inputs and outputs (decoded outputs go high on selection)

ABSOLUTE MAXIMUM RATINGS

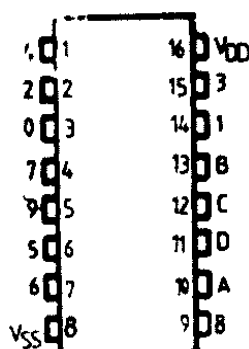
V_{DD}^*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	$V_{DD}+0.5$	V
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for $T_A =$ full package-temperature range		100	mW
T_A	Operating temperature :			
	G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature :			
	G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT	
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
						min.	max.	min.	typ.	max.	min.		max.
I _L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150
			0/10			10		10		0.04	10		300
			0/15			15		20		0.04	20		600
			0/20			20		100		0.08	100		3000
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V _{OH}	Output high voltage												
		0/ 5		< 1	5	4.95		4.95			4.95		
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V _{OL}	Output low voltage												
		5 /0		< 1	5		0.05			0.05		0.05	
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V _{IH}	Input high voltage												
			0.5/4.5	< 1	5	3.5		3.5			3.5		
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V _{IL}	Input low voltage												
			4.5/0.5	< 1	5		1.5			1.5		1.5	
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I _{OH}	Output drive current												
		G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15	
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36	
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9	
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4	
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1	
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36	
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9	
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4	
I _{OL}	Output sink current												
		G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36	
			0/10	0.5		10	1.6		1.3	2.6		0.9	
			0/15	1.5		15	4.2		3.4	6.8		2.4	
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36	
			0/10	0.5		10	1.3		1.1	2.6		0.9	
			0/15	1.5		15	3.6		3.0	6.8		2.4	
I _{IH} I _{IL}	Input leakage current												
		G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1
C _I	Input capacitance			Any input						5	7.5		pF

* T_{LOW} = -55°C for G, H devices, -40°C for E, F devices* T_{HIGH} = +125°C for G, H devices, +85°C for E, F devices

The Noise Margin for both "1" and "0" level is:

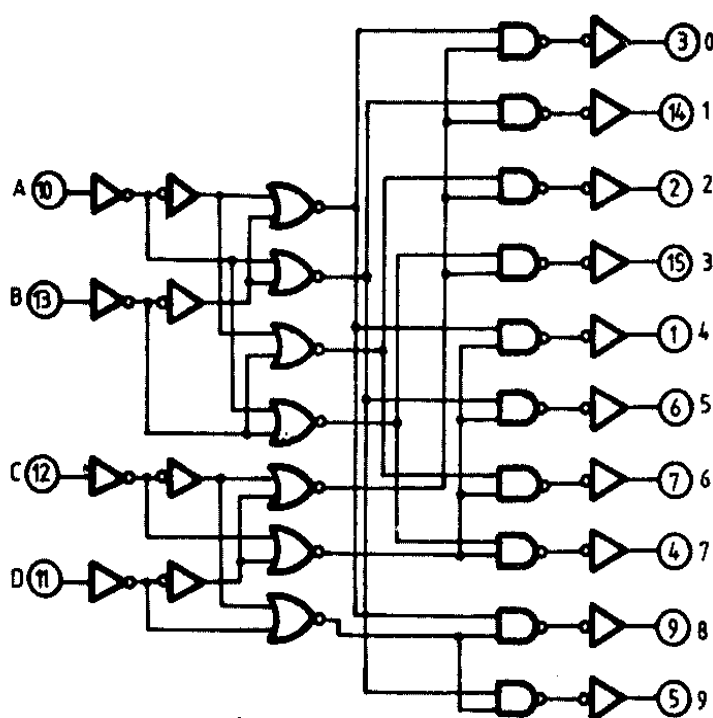
1 V min with V_{DD} = 5 V2 V min with V_{DD} = 10 V2.5 V min with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}$, typical temperature coefficient for all V_{DD} values is $0.3\% / ^\circ\text{C}$ all input rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UM
		min.	typ.	max.	
t_{PHL} t_{PLH} Propagation delay time (clock to out)	5		175	350	ns
	10		80	160	
	15		60	120	
t_{THL} t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

LOGIC DIAGRAM



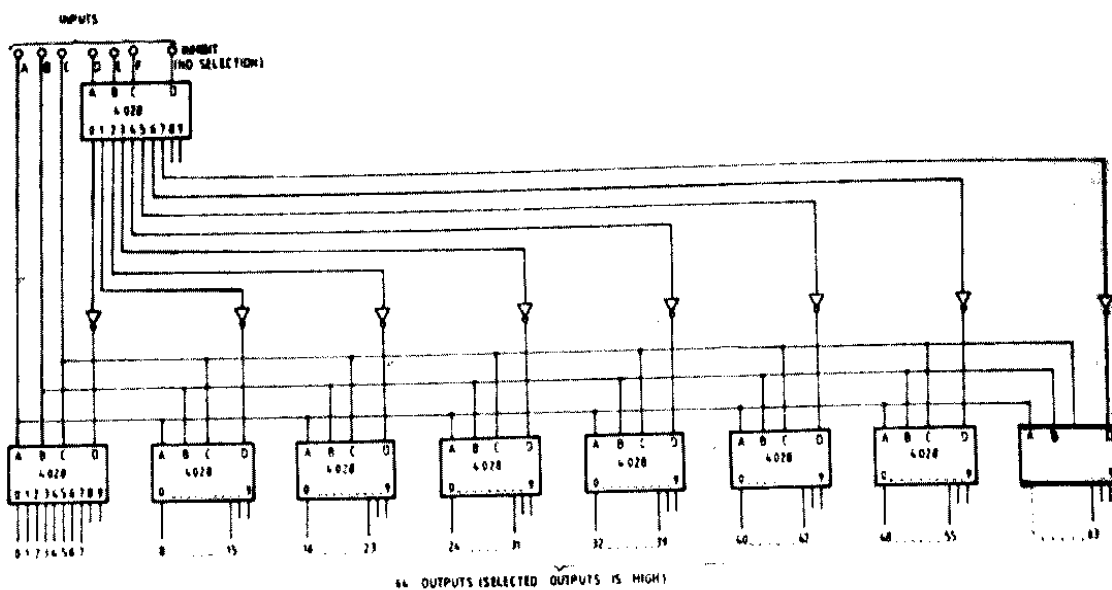
TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0	0	1	0	0	0
0	1	1	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

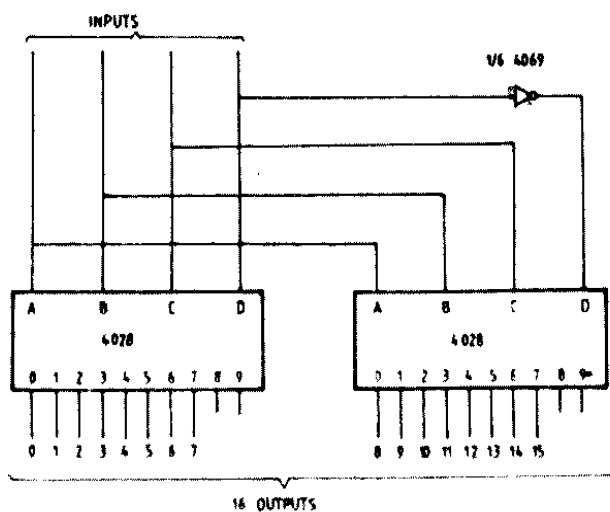
WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

TYPICAL APPLICATIONS

6 — bit binary to 1 of 64 address decoder



Code conversion circuit



Neon readout (Nixie Tube) display application

