ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0C to +70C
Storage Temperature	-65 deg C to +150 deg C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(DC Specification Cont.)

DC CHARACTERISTICS: TA = 0 Deg C to 70 Deg C, VDD = 5V +/- 5%, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output HIGH Voltage	2.4		V	IOH = 400 uA
VOL	Output LOW Voltage		0.4	V	IOL = 24 mA, Note 1,2
VOL	Output LOW Voltage		0.4	V	IOL = 12 mA, Note 1
VOL	Output LOW Voltage		0.4	V	IOL = 10mA, Note 1
VOL	Output LOW Voltage		0.4	V	IOL = 8 mA, Note 1
VOL	Output LOW Voltage		0.4	V	IOL = 4 mA, Note 1
VOL	Output LOW Voltage		0.4	V	IOL = 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VCC + 0.5	V	TTL
VIL	Input LOW Voltage	-0.5	0.8	V	TTL
VIS	Schmitt Input Current	2.4	VCC + 0.5	V	Schmitt, Note 3
VIC	CMOS Input HIGH	3.8	VCC + 0.5	V	CMOS, Note 3
ILI	Input Leakage Current	-10	10	uA	
OLI	Output Leakage Current	-10	10	uA	
ICC	Operating Supply Current		TBD	mA	Input = VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		8	pF	

Notes:

1) Output Current (IOL) Capabilities:

24 mA: SD[0:15]

12 mA:

10mA:

8mA: -CAS, -RAS

4mA: -ROMENL, RA[14-12], CSEL[0-2], HSYNC, VSYNC, -BLANK, P[0-7], PCLK, -DACR, -DACW, MA[0-9], MB[0-9], MD[0-15], -RAS, -WE01, -WE23, -RDSW

2mA: BD[0-7]

2) Open Drain (open-collector) outputs:

24mA: RDY, -NMI, -CINT, -M16, -IO16

3) Input Structures:

Schmitt triggered:

CMOS:

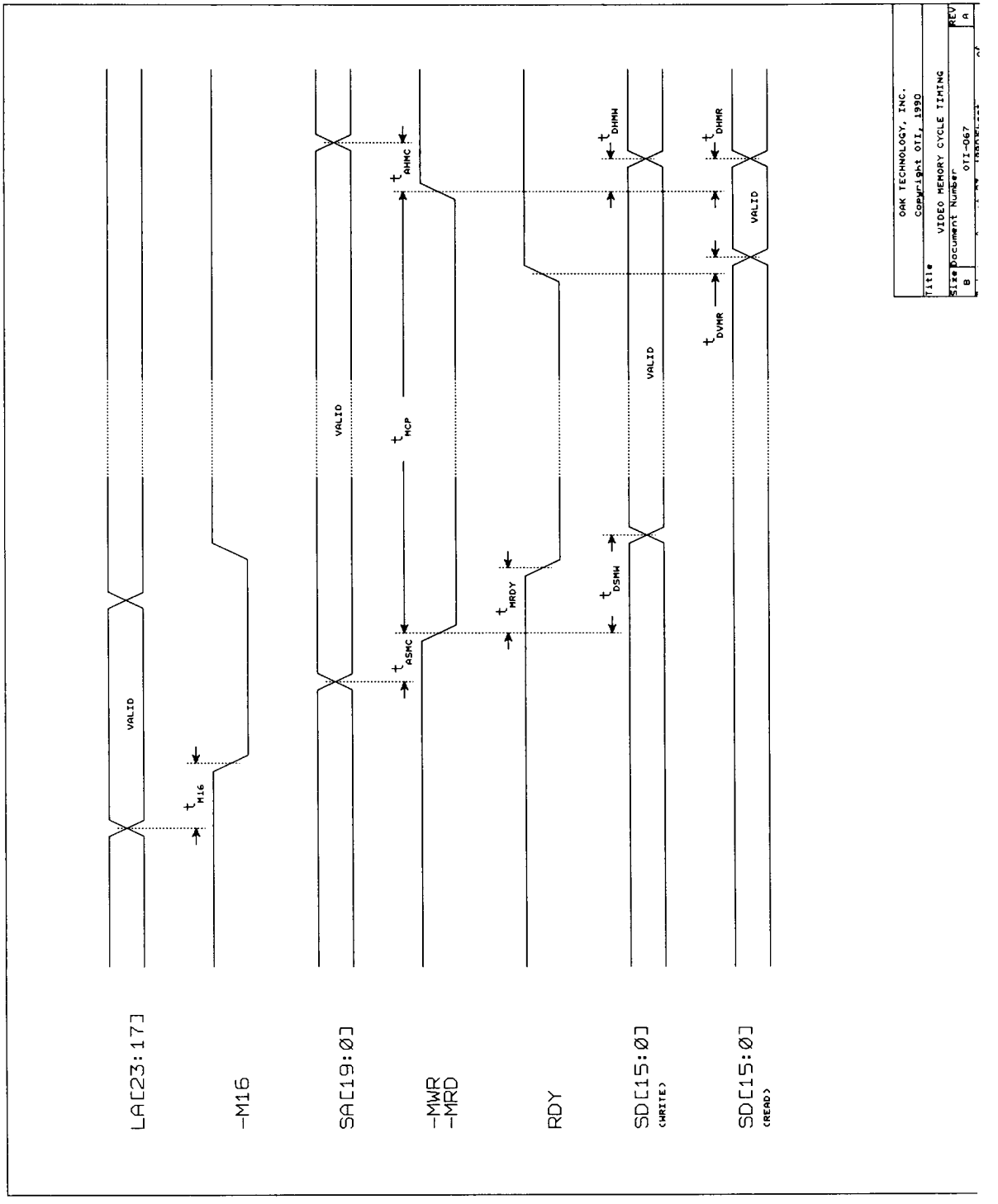
TTL: All others

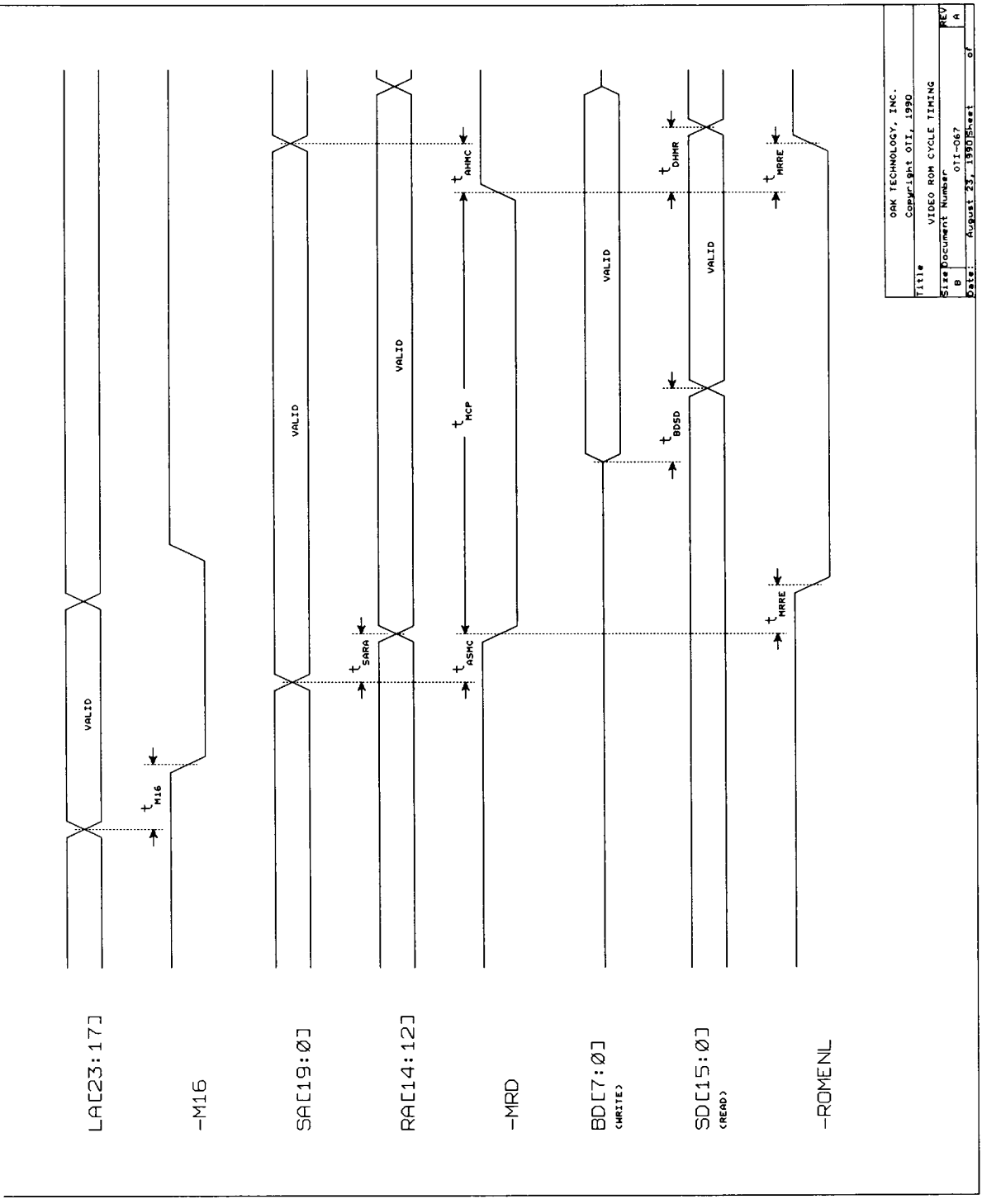
Inputs with pullups: MD[8-15]

SYSTEM BUS INTERFACE TIMING

A. VIDEO MEMORY / VIDEO ROM

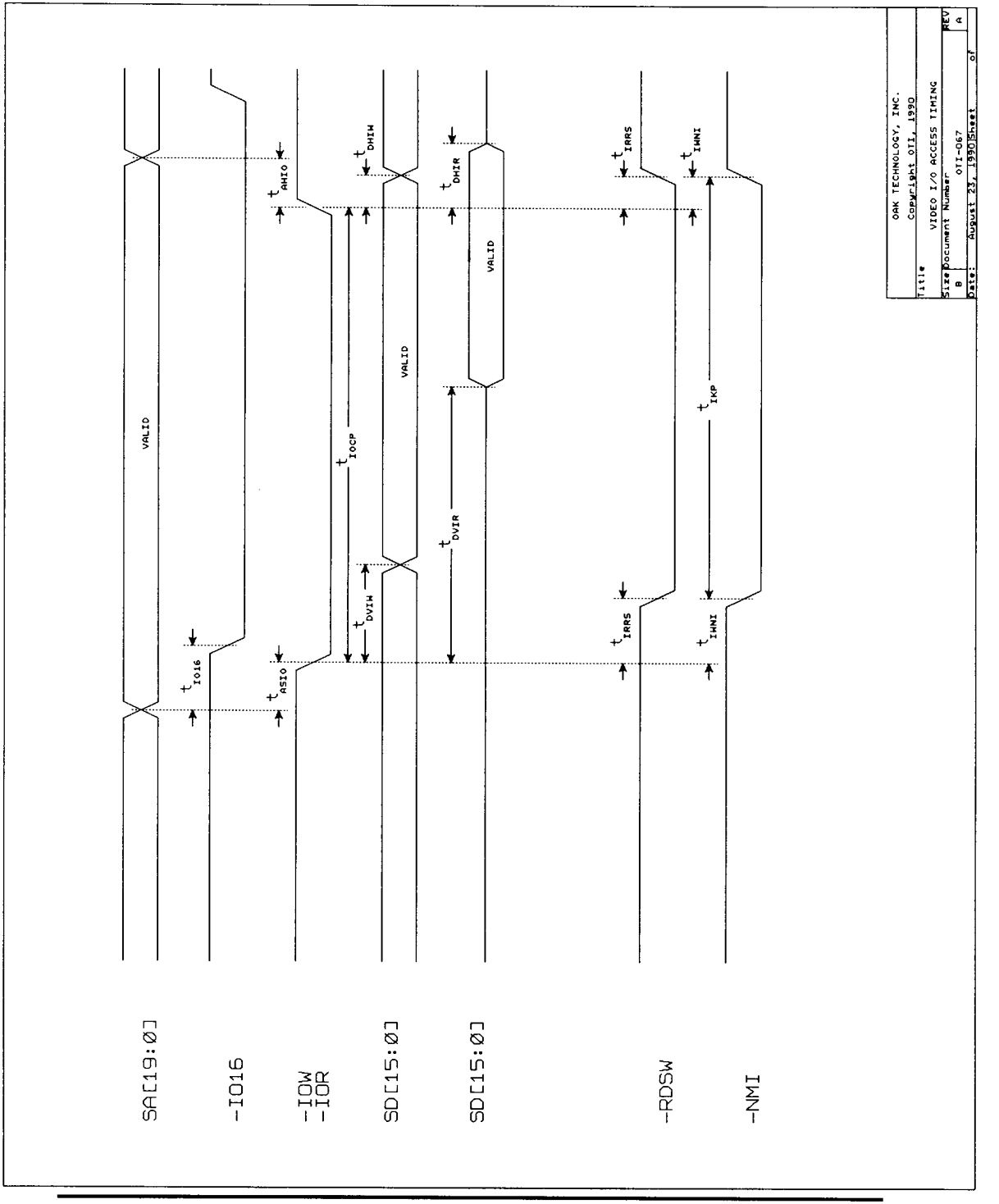
Symbol	Description	Min (ns)	Max (ns)	Note
t_{M16}	-M16 active from valid LA[23:17]		40	
t_{ASMC}	SA[19:0] setup to memory command active	25		
t_{AHMC}	SA[19:0] hold from memory command inactive	20		
t_{MCP}	Memory command pulse width	165		
t_{MRDY}	RDY inactive from memory command active		30	
t_{DSMW}	Write data setup to -MWR active	-45		
t_{DHMW}	Write data hold from -MWR inactive	15		
t_{DVMR}	Read data valid from RDY active		5	
t_{DHMR}	Read data hold from -MRD inactive	0		
t_{SARA}	RA[14:12] delay from SA[14:12]		20	
t_{BDSD}	BD[7:0] valid to SD[15:0] valid		35	
t_{MRRE}	-ROMENL delay from -MRD		25	

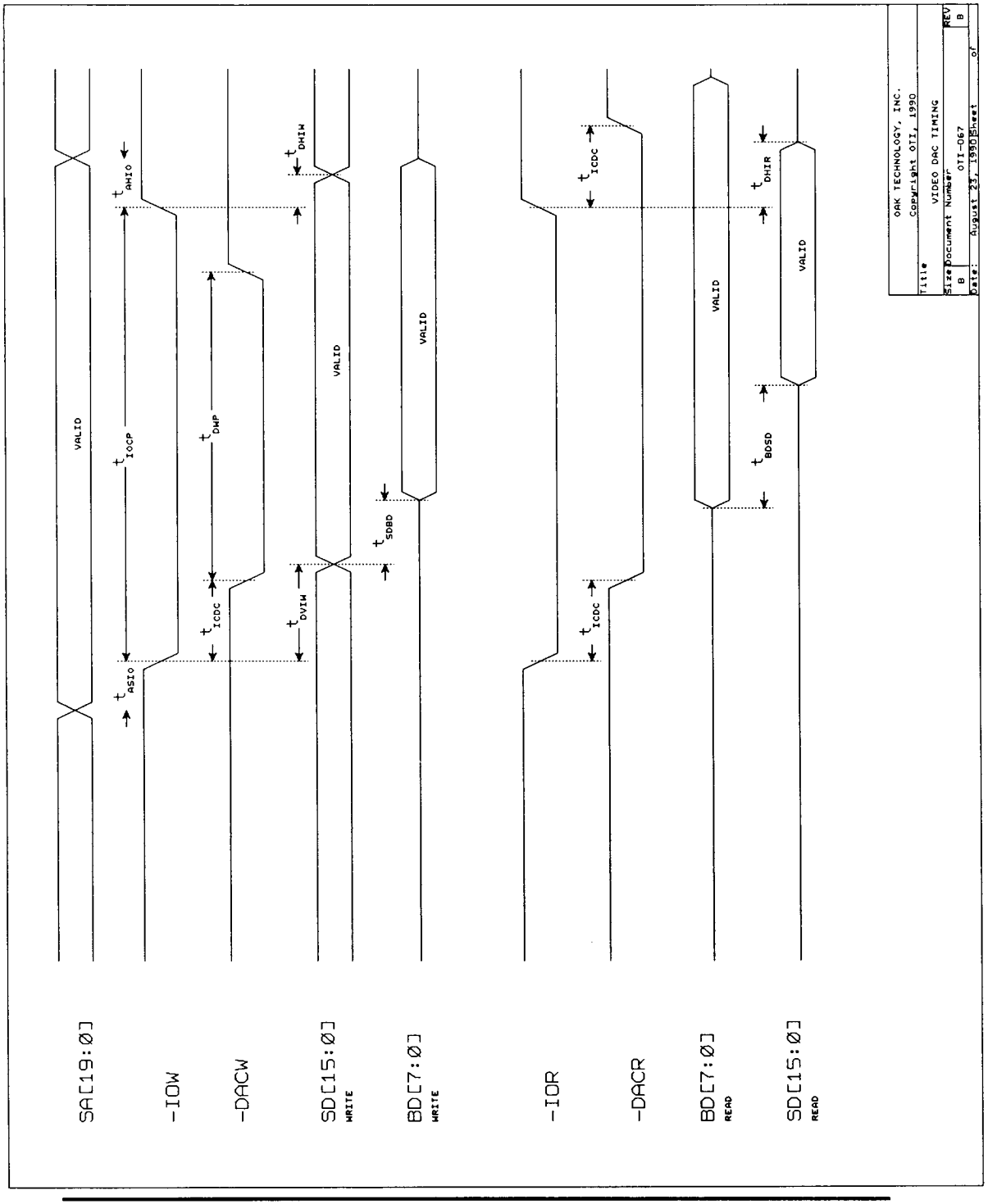




B. VIDEO I/O ACCESS / VIDEO DAC

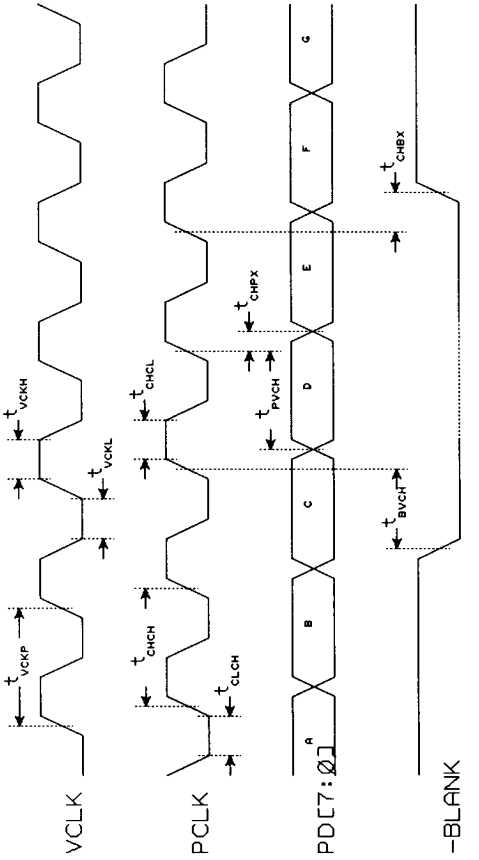
Symbol	Description	Min (ns)	Max (ns)	Note
t_{IO16}	-IO16 active from valid SA[15:0]		60	
t_{ASIO}	SA[15:0] setup to I/O command active	35		
t_{AHIO}	SA[15:0] hold from I/O command inactive	20		
t_{IOCP}	I/O command pulse width	115		
t_{DVIW}	Write data valid from -IOW active	-55		
t_{DHIW}	Write data hold from -IOW inactive	15		
t_{DVIR}	Read data valid from -IOR active		70	
t_{DHIR}	Read data hold from -IOR inactive	0		
t_{IRRS}	-RDSW delay from -IOR		25	
t_{IWNI}	-NMI active from -IOW active		25	
t_{IKP}	-NMI pulse width	t_{IOCP}		
t_{ICDC}	DAC command delay from I/O command		25	
t_{DWP}	-DACW pulse width	70		
t_{SDBD}	SD[7:0] valid to BD[7:0] valid		50	
t_{BDSD}	BD[7:0] valid to SD[15:0] valid		35	





C. VIDEO / PIXEL

Symbol	Description	Min (ns)	Max (ns)	Note
t_{VCKP}	Video input clock period	15		
t_{VCKH}	VCLK width high	6		
t_{VCKL}	VCLK width low	6		
t_{CHCH}	Pixel clock period	15		
t_{CHCL}	PCLK width high	t_{VCKH}-1		
t_{CLCH}	PCLK width low	t_{VCKL}-1		
t_{PVCH}	Pixel word setup time	4		
t_{CHPX}	Pixel word hold time	4		
t_{BVCH}	-BLANK setup time	4		
t_{CHBX}	-BLANK hold time	4		



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D. VIDEO RAM (DRAM) INTERFACE TIMING

Symbol	Description	Min (ns)	Max (ns)	Note
t_{MCKP}	Memory clock period	20		
t_{MCKR}	Memory clock rise/fall		2.5	
t_{RP}	-RAS precharge	$3t_{MCKP}$		
t_{RAS}	-RAS pulse width	$4t_{MCKP}$		
t_{CSH}	-CAS hold time	$4t_{MCKP}$		
t_{RAL}	Column addr. to -RAS lead time	$2t_{MCKP}$		
t_{ASR}	Row address setup	$1t_{MCKP}$		
t_{RAH}	Row address hold	$1t_{MCKP}$		
t_{RSH}	-RAS hold time	$1t_{MCKP}$		
t_{ASC}	Column addr. setup	$1t_{MCKP}$		
t_{CAH}	Column addr. hold	$1t_{MCKP}$		
t_{CP}	-CAS precharge	$1t_{MCKP}$-2		
t_{CAS}	-CAS pulse width	$1t_{MCKP}$+2		
t_{CAC}	Access time from -CAS		$1t_{MCKP}$	
t_{AA}	Access time from Column Address		$2t_{MCKP}$	
t_{CPA}	Access time from -CAS precharge		$2t_{MCKP}$	
t_{RAC}	Access time from -RAS		$4t_{MCKP}$	
t_{RWL}	-WExx to RASn lead	$1t_{MCKP}$		
t_{WCS}	-WExx setup to -CAS	0		
t_{WCH}	-WExx hold referenced to -CAS	$1t_{MCKP}$		
t_{CWL}	-WExx to -CAS lead	$1t_{MCKP}$		
t_{WP}	-WExx pulse width	$1t_{MCKP}$+2		
t_{DS}	Data setup	$1t_{MCKP}$		
t_{DH}	Data hold	$1t_{MCKP}$