ST22XJ64

SMARTCARD 32-BIT RISC MCU WITH 64 KBYTES EEPROM AND JAVACARD™ HARDWARE EXECUTION

DATA BRIEFING

ST22XJ64 FEATURES

- 32-BIT RISC CPU WITH 24-BIT LINEAR MEMORY ADDRESSING
- 96 KBYTES USER ROM
- 4 KBYTES USER RAM
- 64 KBYTES USER EEPROM

32-BIT RISC CPU

- DUAL INSTRUCTION SET, JAVACARD™ AND NATIVE
- 4-STAGE PIPELINE
- 16 GENERAL PURPOSE 32-BIT REGISTERS, AND 10 SPECIAL REGISTERS
- 4 MASKABLE INTERRUPT LEVELS
- SUPERVISOR AND USER MODES

SECURITY

- CPU SECURITY INSTRUCTIONS
  - Clear all general purpose registers instruction
  - Hardware DES and 3DES instructions
  - Fast Multiply and Accumulate instructions for Public Key Cryptography
- CPU DPA/SPA COUNTERMEASURES
- FIPS-140 RANDOM NUMBER GENERATOR
- EEPROM FLASH PROGRAMMING MODE
- CLOCK AND POWER MANAGEMENT
- VOLTAGE, CLOCK FREQUENCY AND TEMPERATURE SENSORS

MEMORY

- HIGHLY RELIABLE CMOS EEPROM 0.35 µm TECHNOLOGY
  - Error Correction Code for single bit fail within a 32-bit word
  - 10 year data retention, 100,000 Erase/Write cycles endurance
  - 1 to 128 bytes Erase or Program in 2 ms typical
- HIGH PERFORMANCE MEMORY
  - Dual memory busses for data and instruction
  - Byte, Short (2) and Word (4) load and store
  - Address auto increment for vector walking
- ADVANCED MEMORY PROTECTION
  - Memory Protection Unit for application firewalling and peripheral access control
- THREE WORKING STACKS
  - Java stack with both 16 and 32-bit accesses
  - User and Supervisor mode stacks

OTHER FEATURES

- HARDWARE ASYNCHRONOUS SERIAL INTERFACE (UART)
  - Contact assignment compatible ISO 7816-2
  - serial IO ports compatible ISO 7816-3
- 3 20-BIT TIMERS WITH INTERRUPT, INTERNAL OR EXTERNAL CLOCK
- CENTRAL INTERRUPT CONTROLLER WITH UP TO 16 INPUT LINES
- 33 MHz INTERNAL CLOCK
- EXTERNAL CLOCK FROM 1 MHz TO 5 MHz
- 3 V ± 10% OR 5 V ± 10% SUPPLY VOLTAGE
- POWER CONSUMPTION 6 mA @ 5 MHz
- TEMPERATURE RANGE -25° C TO +85° C
- POWER REDUCTION IN STANDBY MODE
- ESD PROTECTION GREATER THAN 5000 V

DESCRIPTION

The ST22XJ64, is a member of the SmartJ™ platform using a 32-bit Reduced Instruction Set Computer (RISC) core to execute both native RISC instructions and JavaCard 2.1 Technology instruction (bytecodes) directly. See Figure 1, “SmartJ™ Platform Architecture”

- Direct JavaCard bytecode execution provides high performance advantage over processors that emulate the JavaCard bytecode instruction set.
- The ST22XJ64 features a 24-bit wide linear addressing capability and includes 96 KBytes of User ROM, 4 KBytes of User RAM and 64 KBytes of User EEPROM.

  Memory and Peripheral accesses are controlled by a Memory Protection Unit that allows to implement firewalls between applications.

  Volatile memory and non-volatile memory are accessed via two different busses, allowing simultaneous accesses to code and data.

  Memory load and stores can be performed at byte, short (2-bytes), or word (4-bytes) granularity, with optional pointer auto increment.

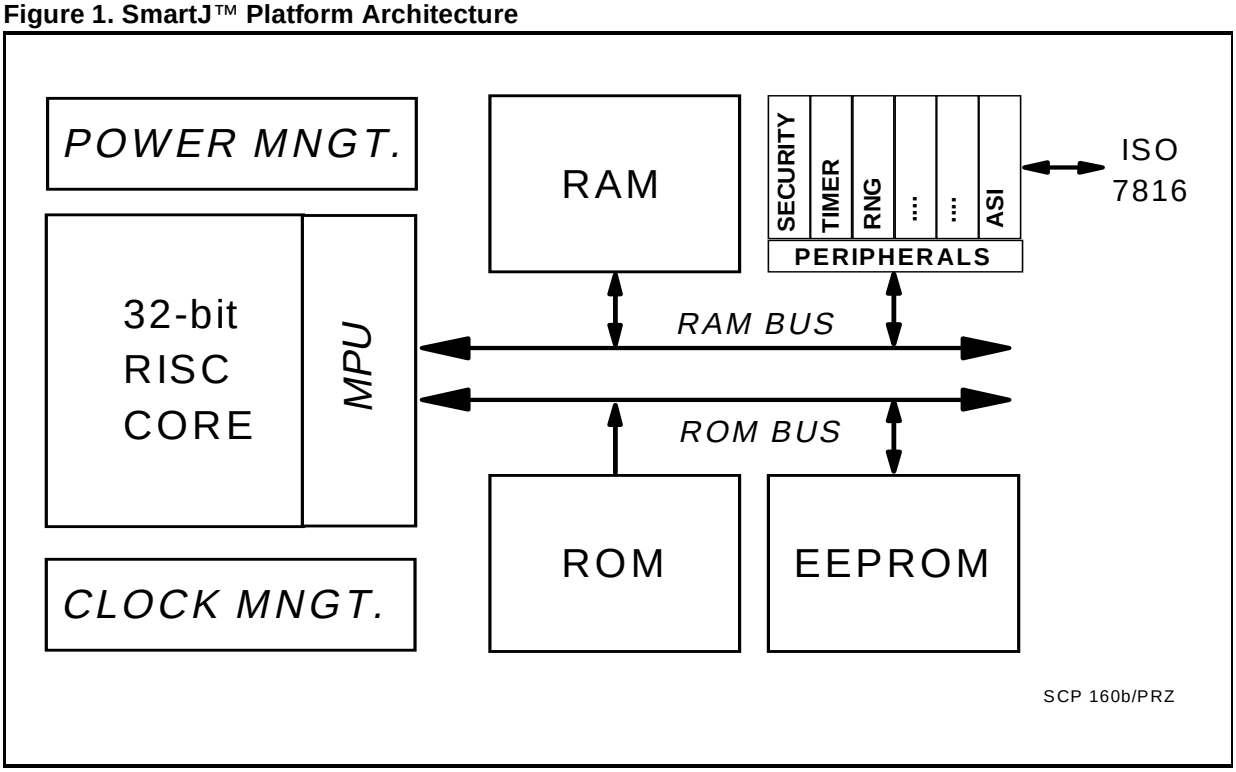
- The ST22 core includes dedicated DES instructions for Secret Key cryptography, and a fast Multiply and Accumulate instruction for Public Key cryptography (RSA). The ST22 core also includes specific instructions for security, such as clear all general purpose registers in a single cycle.
- The ST22XJ64 has clock and power management, 2 configurable Timers, a Central Interrupt Controller and a FIPS-140 Random Number Generator.

- The ST22XJ64 has two execution modes. Java mode is used when JavaCard 2.1 bytecodes are being executed. Native mode is used for long JavaCard 2.1 bytecodes, native methods and system routines. The processor enters Java mode when a dispatch instruction is encountered. When executing in native mode, there are two privilege levels, User and System. Some instructions can only be executed in System mode.

  The CPU core has 16 32-bit general purpose registers, as well as 10 special registers of variable length.

  Instructions are of variable length, from 1 to 4 bytes in native mode.

Figure 1. SmartJ™ Platform Architecture



- Special instructions exist for single-cycle stack operations, a frequent occurrence in Java code. Short Branches and conditional branches within a 1 KByte block or the entire 16 MByte instruction space are supported.

  ST22XJ64 has four stages of pipeline in native mode: fetch, decode, execute and write-back. In Java mode, there are five stages of pipeline: bytecode-fetch, bytecode-decode, decode, execute and write-back.
- The chip also features a very high performance Asynchronous Serial Interface to support high speed serial communication protocols compatible with both contact and contactless ISO standards.
- It is manufactured using the highly reliable ST CMOS EEPROM 0.35 µm technology.

EMBEDDED SOFTWARE

- The Hardware Software Interface (HSI) is a set of C interfaces to the ST22XJ64 EEPROM memory and peripherals. The drivers are:
  - EEPROM
  - Asynchronous Serial Input
  - Central Interrupt Controller
  - Timer
  - Random Number Generator
  - Clock Manager
  - Memory Protection Unit
  - Security Controller
  - Interrupt / Abort handlers

Important Note:

The HSI driver software layer is the only way to have access to the ST22XJ64 peripherals and EEPROM memory.

SOFTWARE DEVELOPMENT ENVIRONMENT

Modularity, flexibility and methodology are the key words for the SmartJ Development Tools Platform. Using the same interface, the developers are able to create, compile and debug a project.

The SmartJ Integrated Development environment (IDE) includes:

- A code Generation chain with capability for using C, C++ compilers, an Assembler/Linker and a Java Compiler.
- An instruction set simulator, a cycle accurate simulator, C, C++, and Java source level debuggers and hardware emulation tools.

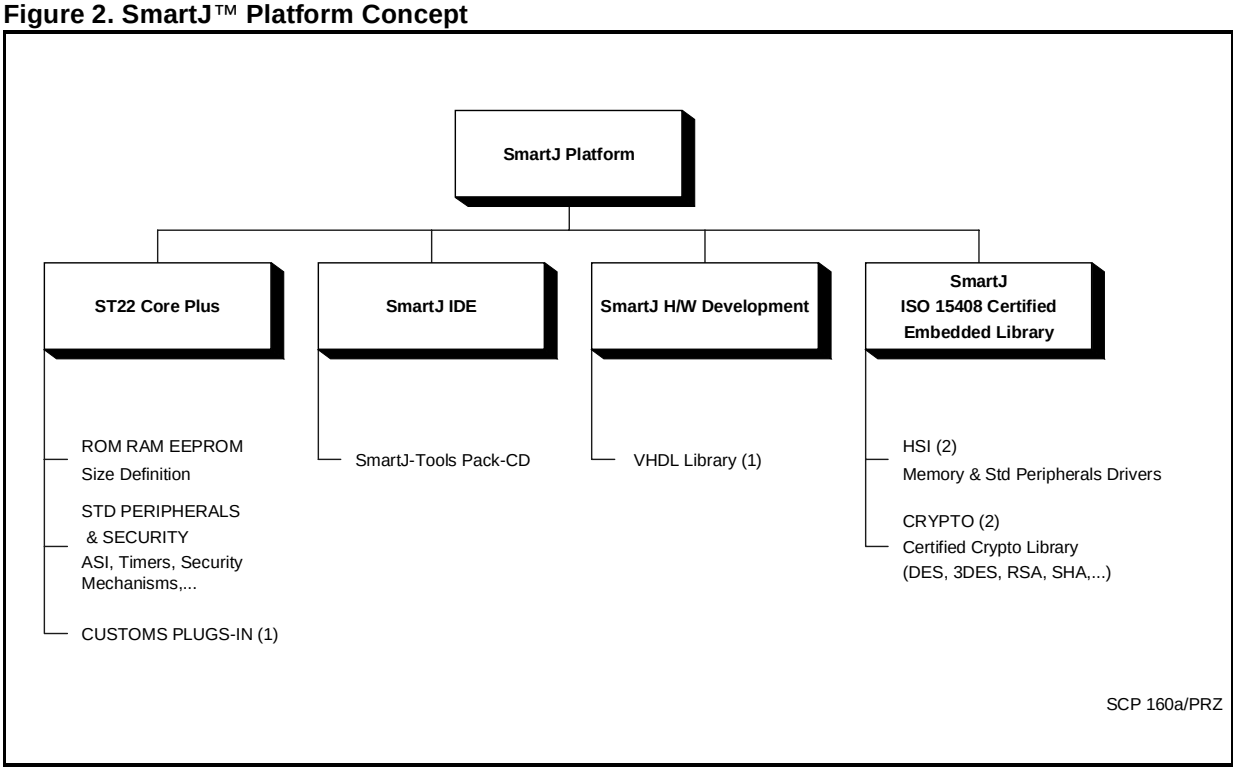
OEM DEVELOPMENT LICENSE TYPES

The ST22XJ64 is a product based on the SmartJ Platform. Developers have two types of licenses for access to the technology:

- STLDA
  The SmartJ Technology License and Distribution Agreement for Standard OEM Developers (Embedded Operating System and Application Software developers) and Card Embedders.

  They must use the SmartJ Hardware Software Interface (HSI) metalayer communication interface to access the ST22XJ64 hardware resources. The validation of the Embedded Software will be done using the Simulators of the Code Validation Tools chain.
- SPTLA
  The SmartJ Platform Technology License Agreement for OEM Platform Developers. The SPTLA is for developers who need to develop a customised architecture using the platform blocks assembled with a proprietary custom hardware plug-in logic block and associated firmware. The complete Code Validation Tools chain including the VHDL Emulator, must be used for both the hardware, software development integration and validation. The complete Code Validation Tool chain is accessible to OEM Platform Developers licensees only.

Figure 2. SmartJ™ Platform Concept



1. **SmartJ Platform Technology License Agreement required**
2. **SmartJ Technology License and Distribution Agreement required**

Figure 3. SmartJ™ IDE

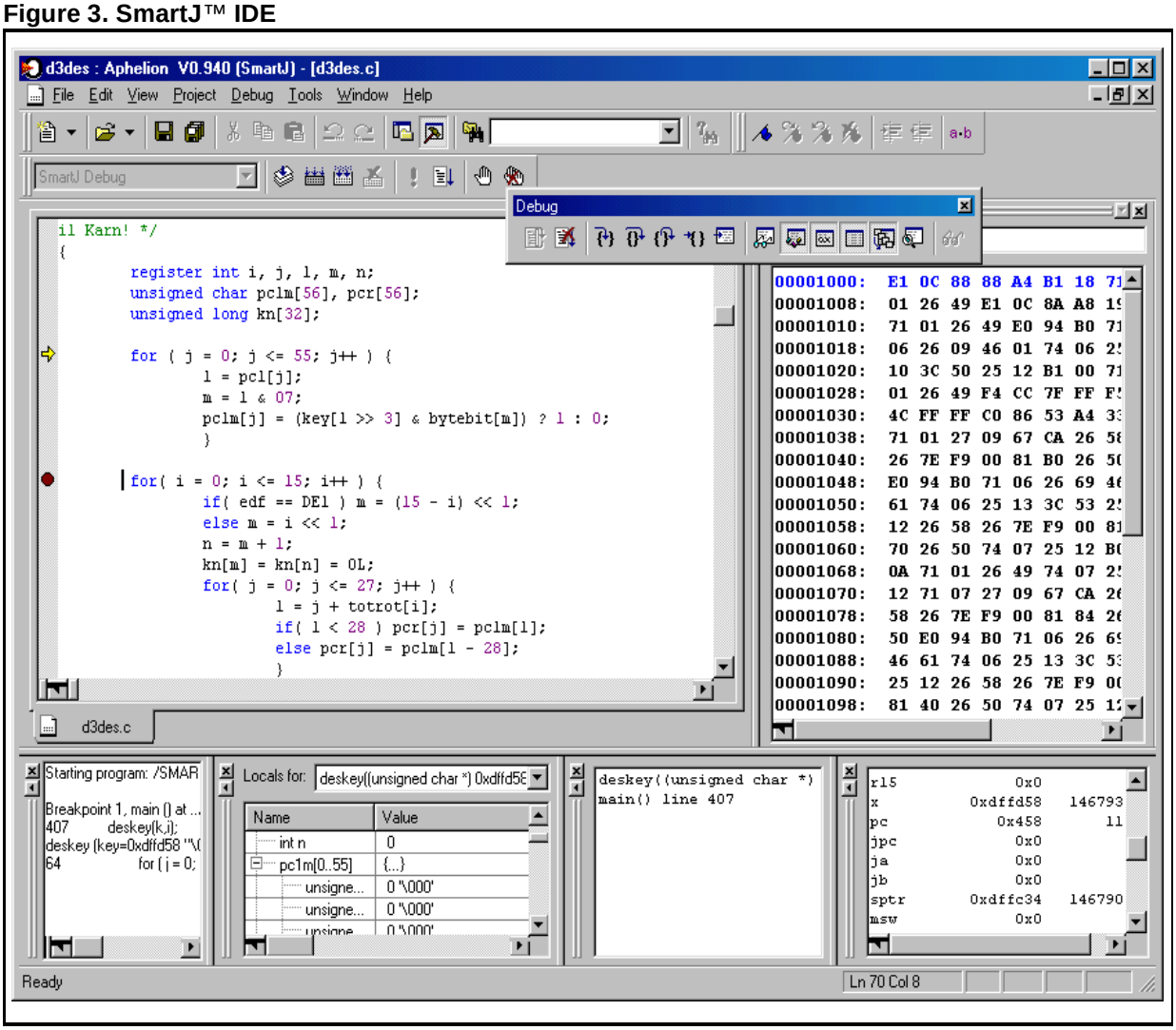


Figure 4. SmartJ™ Code Generation Tools

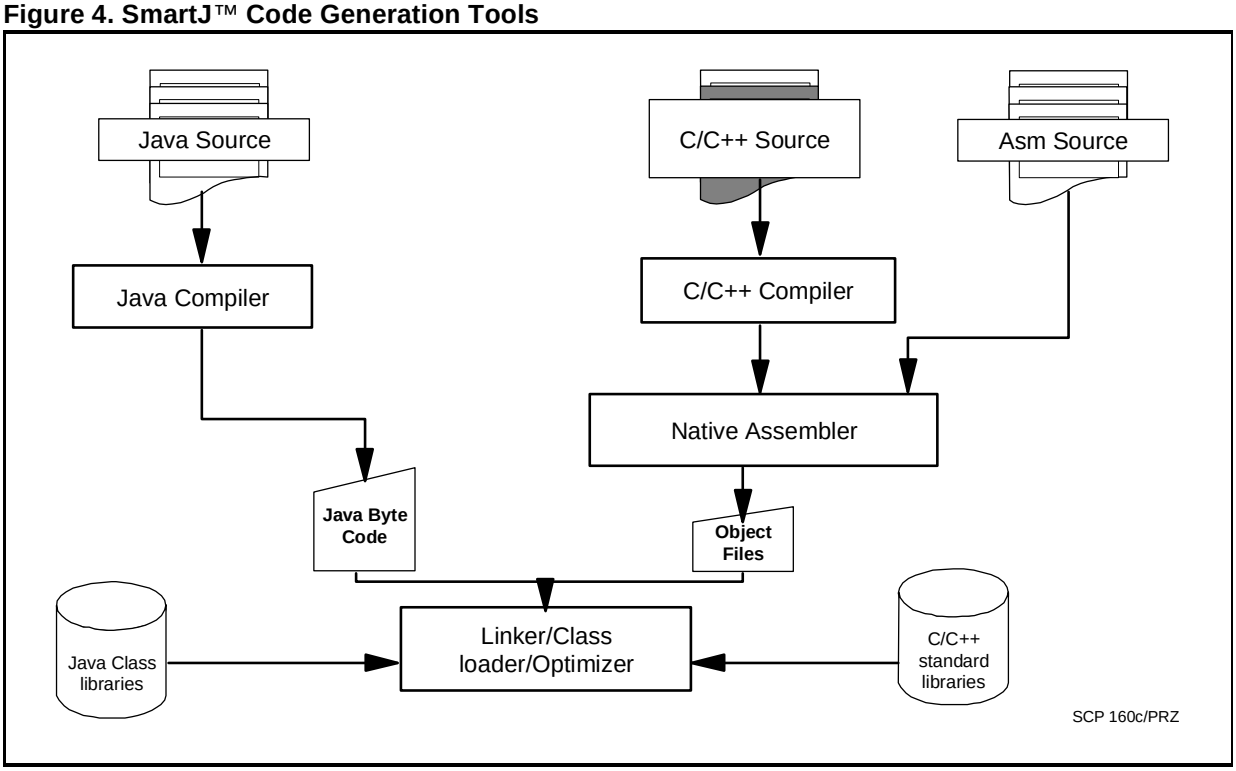
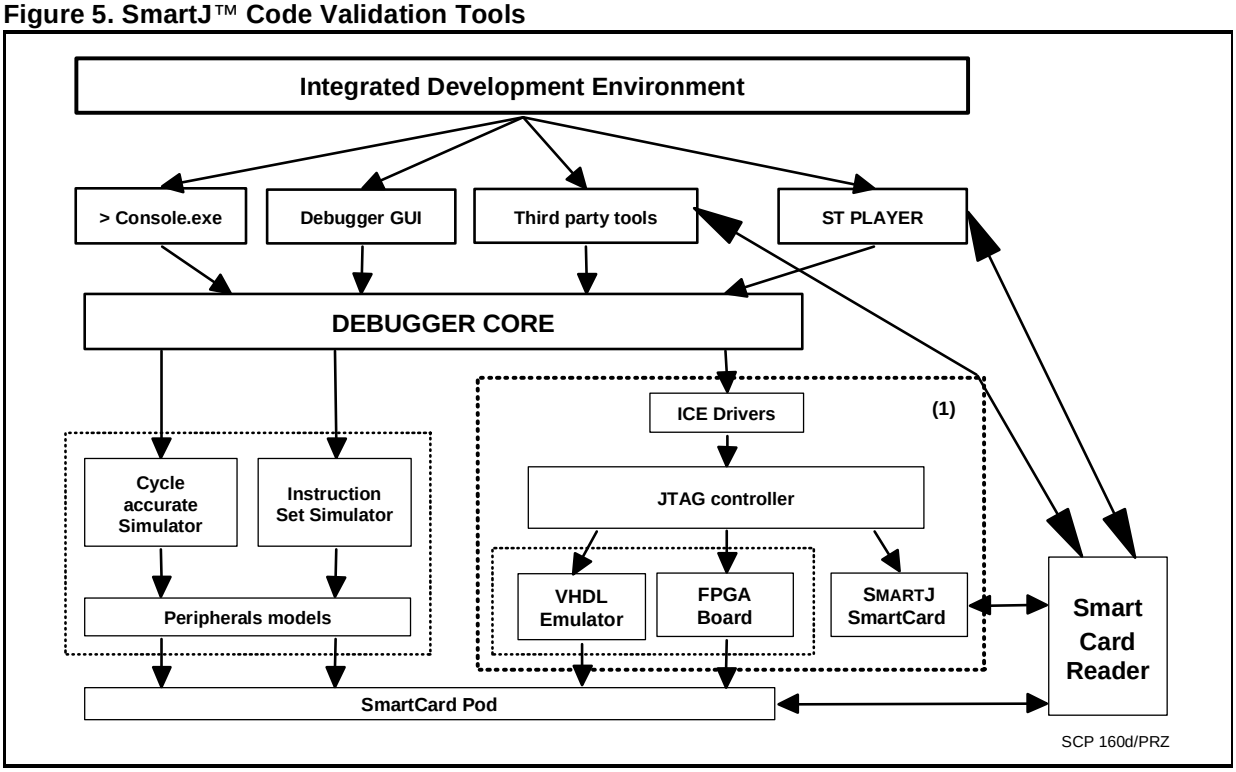


Figure 5. SmartJ™ Code Validation Tools



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3. **Contact ST Sales Office**