

HA19505

10-Bit D/A Converter

The HA19505 is a high-speed, low-power 10-bit D/A converter. The digital and clock inputs of this monolithic bipolar LSI are fully TTL/CMOS compatible. The noise-minimizing internal reference voltage generator and high conversion rate ($f_{CLK} = 50\text{MHz}$ typ) make this device suitable for high-speed image processing applications.

Features

- 10-bit resolution
- 50MHz (typ) conversion rate
- Single power supply: +5V
- TTL/CMOS compatible digital and clock inputs
- Internal reference voltage (+3.0V typ)
- Low power consumption: 225mW (typ)

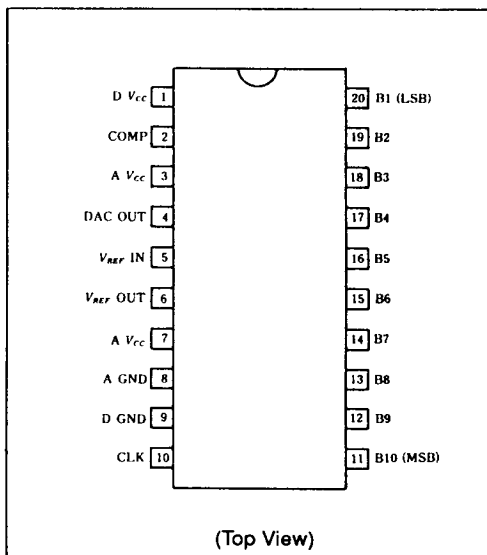
Applications

- Video signal processing
- Image processing, etc.

Ordering Information

Type No.	Package
HA19505	DP-20N

Pin Arrangement

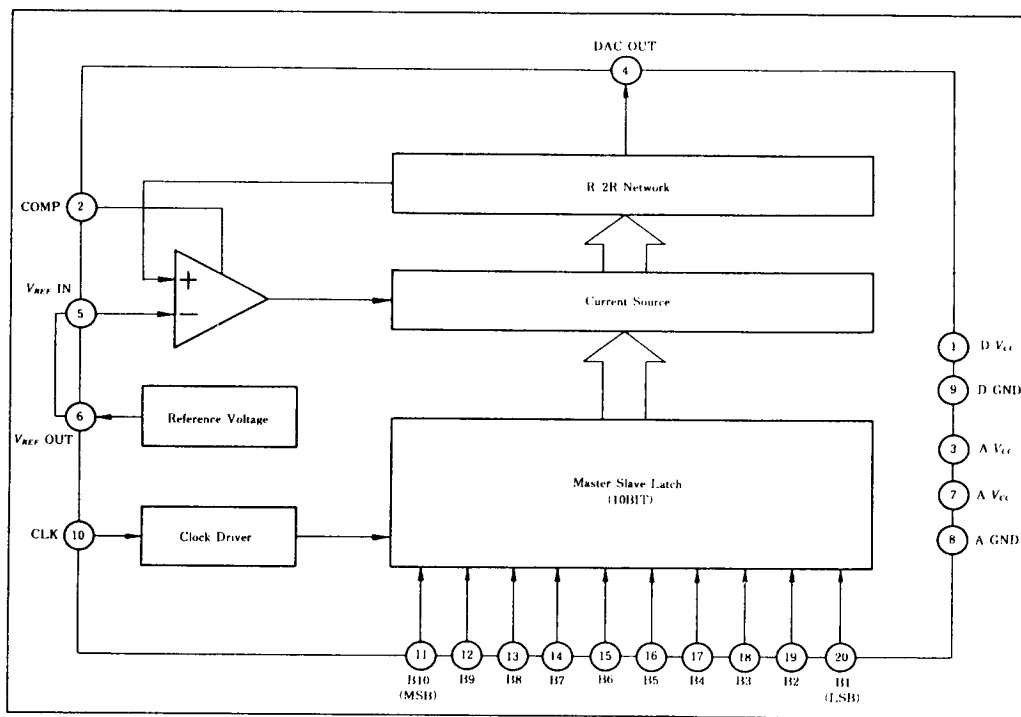


Pin Descriptions

Pin	Symbol	Function
1	DVcc	Digital power supply (+5V)
2	COMP	Phase compensation
3	AVcc	Analog power supply (+5V)
4	DAC OUT	Analog voltage output
5	VREF IN	Reference voltage input
6	VREF OUT	Reference voltage output
7	A Vcc	Analog power supply (+5V)
8	AGND	Analog ground
9	DGND	Digital ground
10	CLK	Clock input

Pin	Symbol	Function
11	B10	Digital input (MSB)
12	B9	Digital input
13	B8	Digital input
14	B7	Digital input
15	B6	Digital input
16	B5	Digital input
17	B4	Digital input
18	B3	Digital input
19	B2	Digital input
20	B1	Digital input (LSB)

Block Diagram



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$, unless otherwise specified)

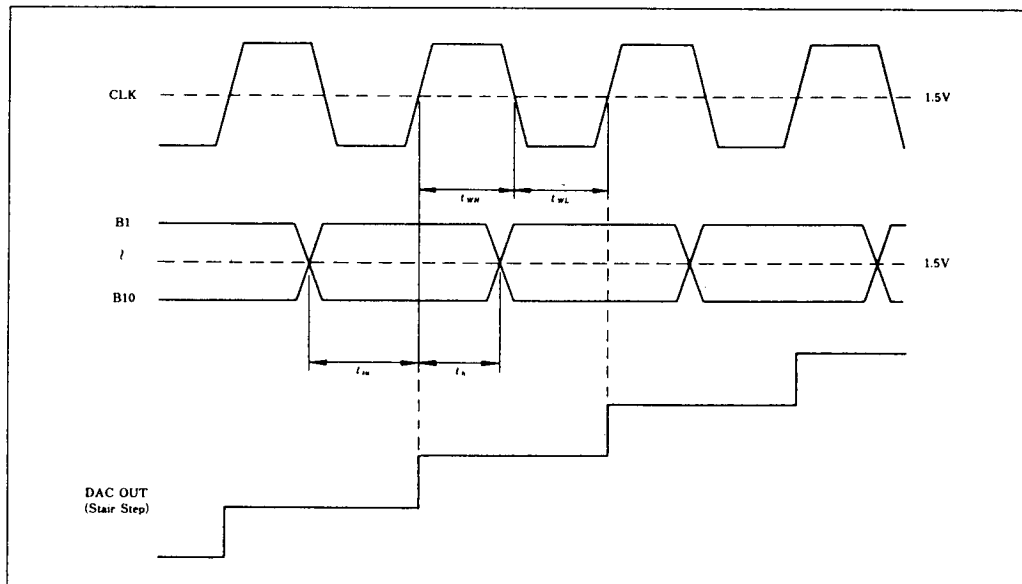
Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	+7.0	V
Digital input voltage	V_{IN}	0 to V_{CC}	V
Power dissipation	P_T	500	mW
Operating temperature	T_{opr}	0 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, and pins 5 and 6 are shorted, unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resolution		—	10	—	bit	
Conversion rate	f_{CLK}	40	50	—	MHz	
Linearity error	LE	-0.12	—	+0.2	% FS	
Clock pulsewidth H level	t_{WH}	12.5	—	—	ns	$f_{CLK} = 40\text{MHz}$
Clock pulsewidth L level	t_{WL}	12.5	—	—	ns	$f_{CLK} = 40\text{MHz}$
Data setup time	t_{su}	10	—	—	ns	$f_{CLK} = 40\text{MHz}$
Data hold time	t_h	10	—	—	ns	$f_{CLK} = 40\text{MHz}$
Power supply voltage	V_{CC}	4.75	5.00	5.25	V	
Current consumption	I_{CC}	—	45	60	mA	
Digital input voltage	V_{IH}	2.0	—	V_{CC}	V	
	V_{IL}	0	—	0.8	V	
Digital input current	I_{IH}	—	—	20	μA	$V_{IH} = 2.7\text{V}$
	I_{IL}	-400	—	—	μA	$V_{IL} = 0.4\text{V}$
Reference input current	$I_{REF IN}$	-20	0	20	μA	$V_{REF IN} = 3.0\text{V}$
Reference input voltage	$V_{REF IN}$	2.0	3.0	4.0	V	
Reference output voltage	$V_{REF OUT}$	—	3.0	—	V	
Analog output voltage	Full scale	$V_{CC} - 15\text{m}$	V_{CC}	$V_{CC} + 15\text{m}$	V	$V_{IH} \geq 2.0\text{V}$
	Zero scale	—	4.001	—	V	$V_{IL} \leq 0.8\text{V}$
Output impedance	Z_{out}	55	75	95	Ω	



Timing Chart



Input Code Table

B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A _{out}
0	0	0	0	0	0	0	0	0	0	V _{ZS}
0	0	0	0	0	0	0	0	0	1	V _{ZS} + 1 LSB
.	.	.	.	.	.	.	.	.	.	.
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.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	V _{FS} - 1 LSB
1	1	1	1	1	1	1	1	1	1	V _{FS}

Note: 1 LSB = (V_{FS} - V_{ZS})/1023

