16,384 BIT ROM WITH I/O PORTS

GENERAL DESCRIPTION

The TMP8355P is a ROM and I/O chip to be used in the TLCS-85A microcomputer system. The ROM portion is organized as 2,048 words by 8 bits.
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

FEATURES

- 2048 words x 8 bits ROM
- Single + 5V Power Supply
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Access Time : 400 ns (MAX.)
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 pin DIP
- Compatible with Inptel's 8355

PIN CONNECTIONS (TOP VIEW)

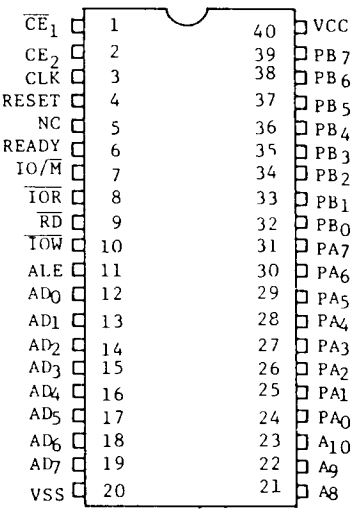

FIGURE 1 TMP8355P PINOUT DIAGRAM

BLOCK DIAGRAM

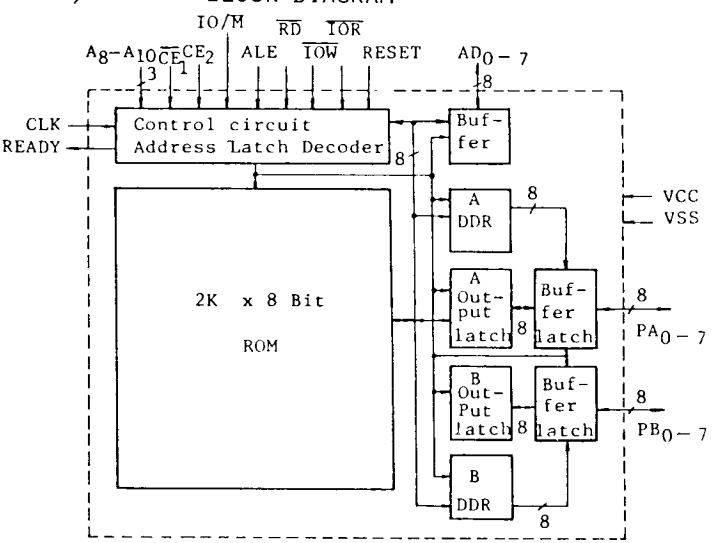

FIGURE 2 TMP8355P FUNCTIONAL BLOCK DIAGRAM

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PIN NAMES AND PIN DESCRIPTION

ALE (INPUT)

When Address Latch Enable goes high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE_2, and $\overline{CE_1}$, enter the address latches. The signals (AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE_2, $\overline{CE_1}$) are latched in at the trailing edge of ALE.

AD_{0-7} (INPUT/OUTPUT, 3-STATE)

Bi-directional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.

A_{8-10} (INPUT)

These are the high order bits of the ROM address. They do not affect I/O operations.

$\overline{CE1}$, CE2 (INPUT)

CHIP ENABLE INPUTS: $\overline{CE_1}$ is active low and CE_2 is active high. Both chip enables must be active to permit accessing the ROM.

IO/$\overline{M}$ (INPUT)

If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.

$\overline{RD}$ (INPUT)

If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port.
When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.

$\overline{IOW}$ (INPUT)

If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}.
The state of IO/$\overline{M}$ is ignored.

CLK (INPUT)

The CLK is used to force the READY into its high state after it has been forced low by $\overline{CE_1}$ low, CE_2 high, and ALE high.

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READY (OUTPUT, 3-STATE)

READY is a 3-state output controlled by $\overline{CE}_1$, CE_2, ALE and CLK.
READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.

PA_0 - PA_7 (INPUT/OUTPUT, 3-STATE)

These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active, and $\overline{IOW}$ is low and a 0 was previously latched from AD_0.
Read operation is selected by either $\overline{IOR}$ low, active Chip Enables and AD_0 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 low.

PB_0 - PB7 (INPUT/OUTPUT, 3-STATE)

This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.

RESET (INPUT)

In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).

$\overline{IOR}$ (INPUT)

When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} "1".

V_{CC} (POWER)

+5 volt supply.

V_{SS} (POWER)

Ground Reference

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FUNCTIONAL DESCRIPTION

ROM SECTION

The TMP8355P contains an 8-bit address latch which allows it to interface circectly to TLCS-85A microcomputer system without additional hardware.
The ROM portion of the chip is addressed by the 11-bit address (A8-10, AD_{0-7}) and CE. The address, IO/$\overline{M}$, CE_2 and $\overline{CE_1}$ are latched into the address latches on falling edge of ALE. If the Chip Enables (CE_2 and $\overline{CE_1}$) are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O SECTION

The I/O port portion consits of two 8-bit I/O ports and two 8-bit Data Direction Registers (DDR). The I/O portion of the chip is addressed by the latched value of AD_0 and AD_1. Contents of Port A and Port B can be read and written, but the contents of DDR's cannot be read. The contents of the selected I/O port can be read out when the latched Chip Enable are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low.
The two 8-bit DDR's (DDRA and DDRB) are used to determine the input/output status of each pin in the corresponding port.
A '0' specifies an input mode and a '1' specifies an output mode.
The two 8-bit DDR's are cleared by RESET signal. The table 1 summarize Port and DDR designation.

TABLE 1, SELECTION OF PORT AND DDR DESIGNATION

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

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ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to V_{SS}	-0.5V to 7.0V
V_{IN}	Input Voltage with Respect to V_{SS}	-0.5V to 7.0V
V_{OUT}	Output Voltage with Respect to V_{SS}	-0.5V to 7.0V
P_D	Power Dissipation	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10sec.)	260°C
T_{STG}	Storage Temperature	-55°C to+150°C
T_{OPR}	Operating Temperature	0°C to+70°C

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V $\pm$ 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4			V
I_{IL}	Input Leakage Current	V_{IN} = V_{CC} to 0V			$\pm$ 10	μA
I_{LO}	Output Leakage Current	0.45 ≤ Vout ≤ V_{CC}			$\pm$ 10	μA
I_{CC}	V_{CC} Supply Current				180	mA

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A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{CYC}	Clock Cycle Time		320			ns
t_L	CLK Low Width		80			ns
t_H	CLK High Width		120			ns
t_r, t_f	CLK Rise and Fall Time				30	ns
t_{AL}	Address to Latch Set Up Time		50			ns
t_{LA}	Address Hold Time after Latch		80			ns
t_{LC}	Latch to READ/WRITE Control		100			ns
t_{RD}	Valid Data Out Delay from READ Control	150pF			170	ns
t_{AD}	Address Stable to Data Out Valid	Load			400	ns
t_{LL}	Latch Enable Width		100			ns
t_{RDF}	Data Bus Float after READ		0		100	ns
t_{CL}	READ/WRITE Control to Latch Enable		20			ns
t_{CC}	READ/WRITE Control Width		250			ns
t_{DW}	Data In to WRITE Set Up Time		150			ns
t_{WD}	Data In Hold Time after WRITE		10			ns
t_{WP}	WRITE to Port Output				400	ns
t_{PR}	Port Input Set Up Time		50			ns
t_{RP}	Port Input Hold Time		50			ns
t_{RYH}	READY Hold Time		0		160	ns
t_{ARY}	ADDRESS (CE) to READY				160	ns
t_{RV}	Recovery Time between Controls		300			ns
t_{RDE}	Data Out Delay from READ Controls		10			ns
t_{LCK}	ALE Low during CLK High		100			ns

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TIMING WAVEFORMS

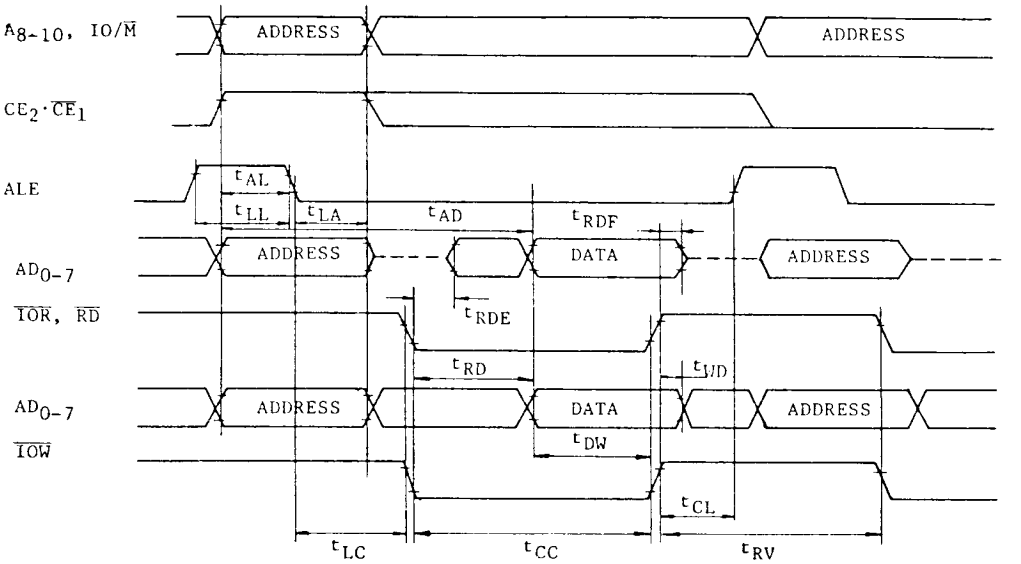

FIGURE 3 PROM READ, I/O READ, AND WRITE TIMING

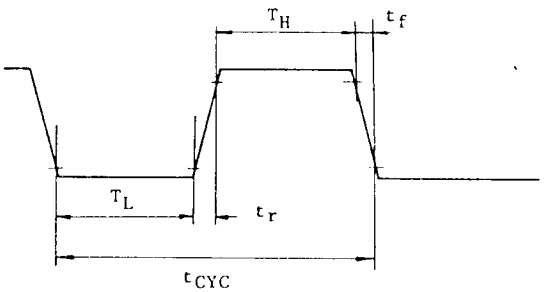

FIGURE 4 CLOCK SPECIFICATION FOR TMP8355P

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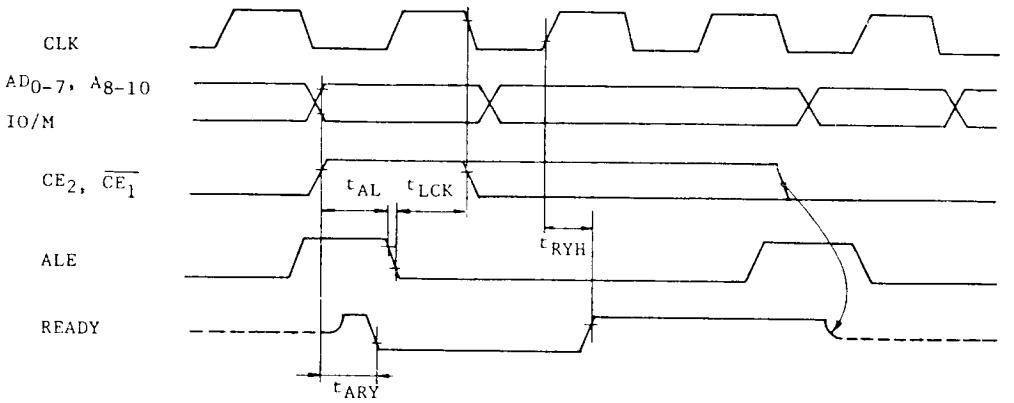
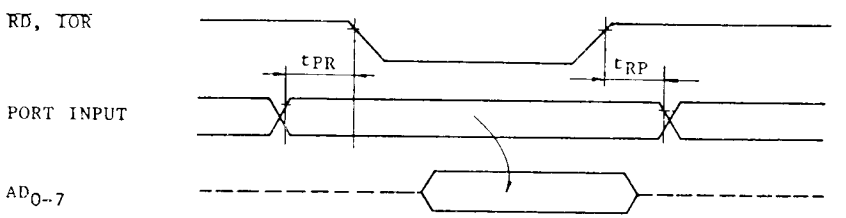


FIGURE 5 WAIT STATE TIMING (READY = 0)

A. INPUT MODE



B. OUTPUT MODE

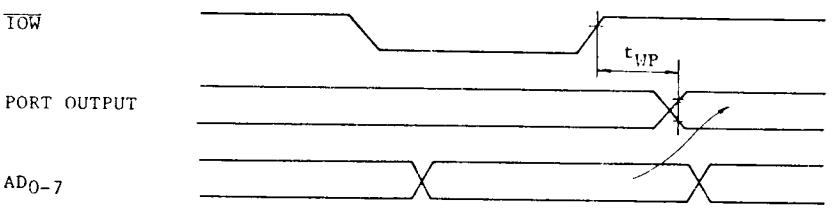


FIGURE 6 I/O PORT TIMING

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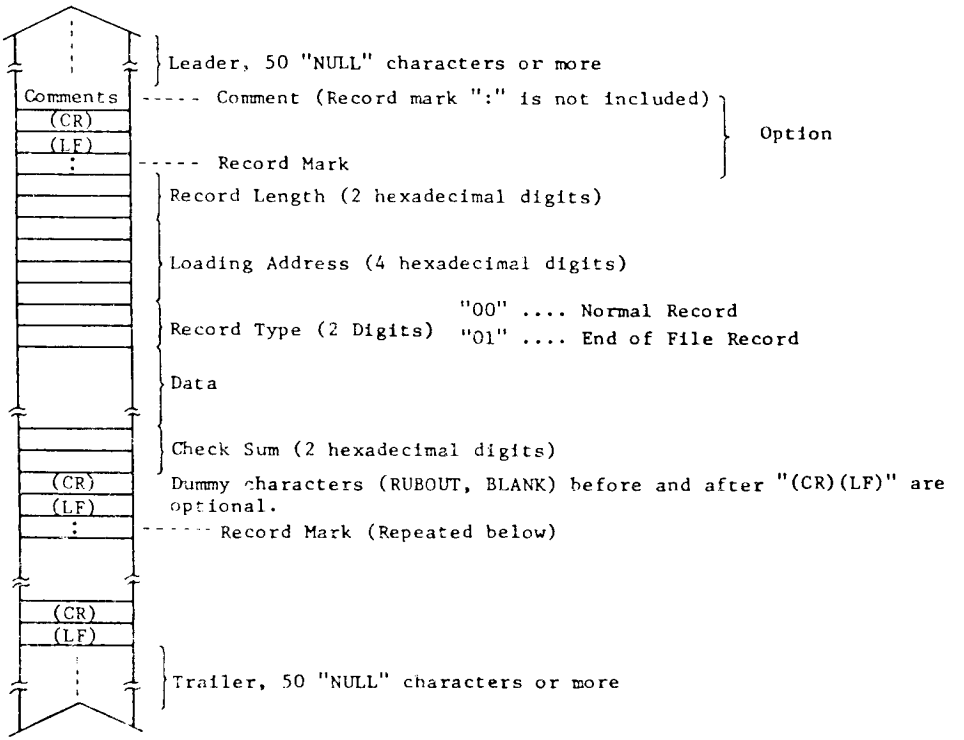
PROGRAM TAPE FORMAT

TMP8355P programs are delivered in the form of punched paper tape or the 8755A from which to copy. In case of the 8755A, Toshiba needs two pieces.

(1) Tape Format



(2) Example of Tape List

```
TOSHIBA MICRO COMPUTER TLCS-84
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884DDE67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                    :
                    :
                    :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8B31977E3FB5AD1F41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20VC372BF60BD6
:00000001FF
```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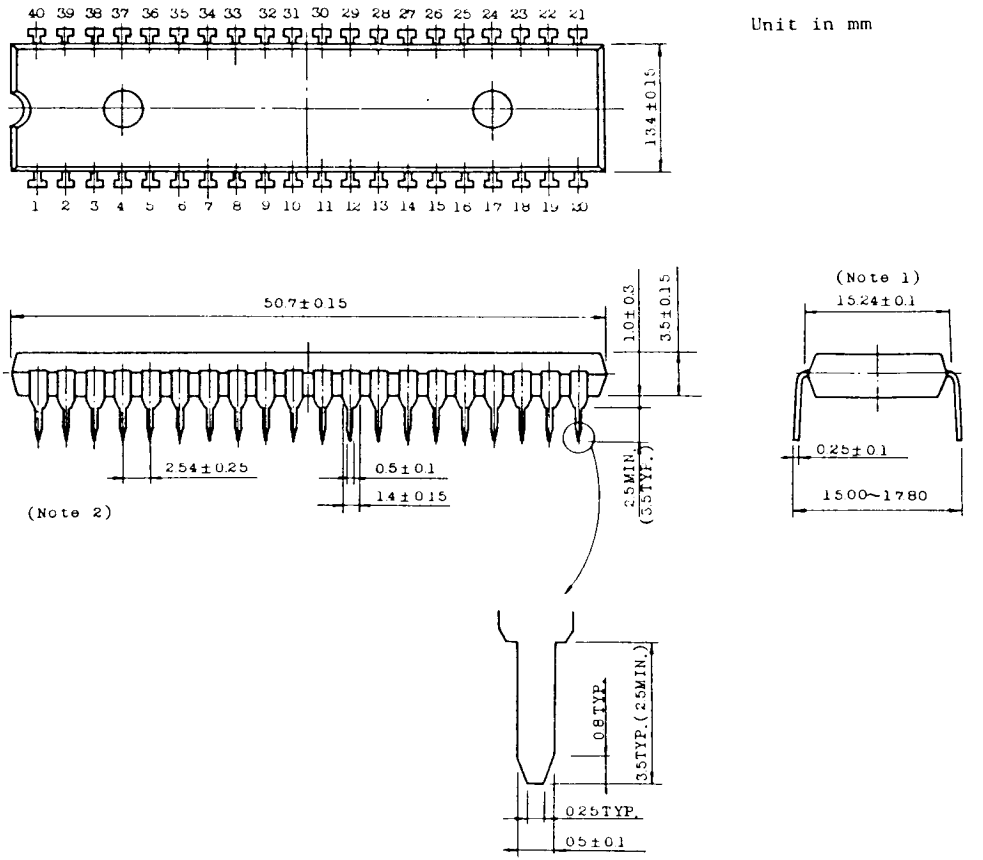
OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

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