CONNOR WINFIELD

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CRYSTAL CONTROLLED OSCILLATORS

SURFACE MOUNT PLL-BASED PECL VCXO

SPECIFICATIONS		GV93-52*	GV93-53*	GV93-54*	GV93-62*	GV93-63*	GV93-64*
Available Frequency Ranges		120 to 135 MHz 144 to 168 MHz 174 to 205 MHz 232 to 270 MHz 288 to 336 MHz 348 to 410 MHz 464 to 540 MHz 576 to 672 MHz			144 to 168 MHz 174 to 205 MHz 288 to 336 MHz 348 to 410 MHz 576 to 672 MHz		
Frequency Stability		±50ppm	±100ppm	±20ppm	±50ppm	±100ppm	±20ppm
Operating Temp Range		0°C to +70°C			-40°C to +85°C		
Storage Temp Range		-55°C to +125°C					
Output	Waveform	PECL Squarewave , 100K Compatible					
	Load	Output must be terminated into 50 Ohms to 3Vdc.					
	Voltage Voh	4.0V Minimum , 4.5V Maximum					
	Voltage Vol	2.9V Minimum , 3.4V Maximum					
	Symmetry	45/55 Maximum measured at 50% level					
	Rise/Fall Time	750pS Maximum					
	Jitter	10pS rms Maximum , Full Bandwidth					
		3pS rms Maximum , 12KHz to 20MHz Bandwidth					
	SSB Phase Noise	-100dBc/Hz typical @ 10KHz offset					
Frequency Control		Positive Transfer Characteristic					
	Control Voltage	0.5 to 4.5Vdc					
	Deviation @25°C	±75ppm Minimum , ±140ppm Maximum					
	Center Frequency @25°C	Control Voltage 2.5Vdc ±0.5Vdc					
	Linearity	< ±10%					
	Input Impedance	> 50K ohms at < 10KHz					
Enable/ Disable Option (Pin 1):	Enable (Vil)	0.5Vdc Maximum					
	Disable (Vih)	1.5Vdc Minimum Q (Pin 7) disables to low state, Option $\overline{Q}$ (Pin 6) disables to high state. When Pin 1 is floating, output is in disabled state.					
Supply Voltage		+5Vdc ±5%					
Supply Current		100mA Maximum					
Package		Hermetically sealed, leadless ceramic package					
Options * - add suffix to model number		0	No Connection on Pin 1 and Pin 6				
		1	Complementary Output on Pin 6 , N/C on Pin 1				
		2	Enable/Disable on Pin 1 , N/C on Pin 6				
		3	Enable/Disable on Pin 1 , Complementary Output on Pin 6				

Specifications subject to change without notice.

ISSUED BY: _____

Dimensional Tolerance: ±.02" ±.005"

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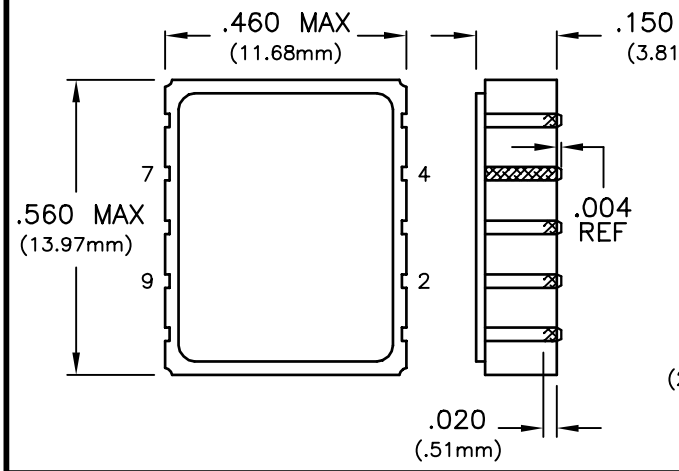
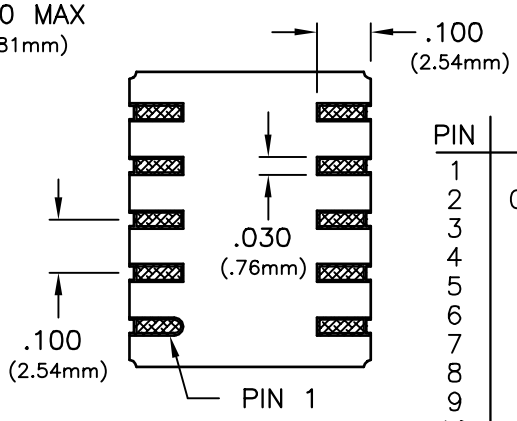
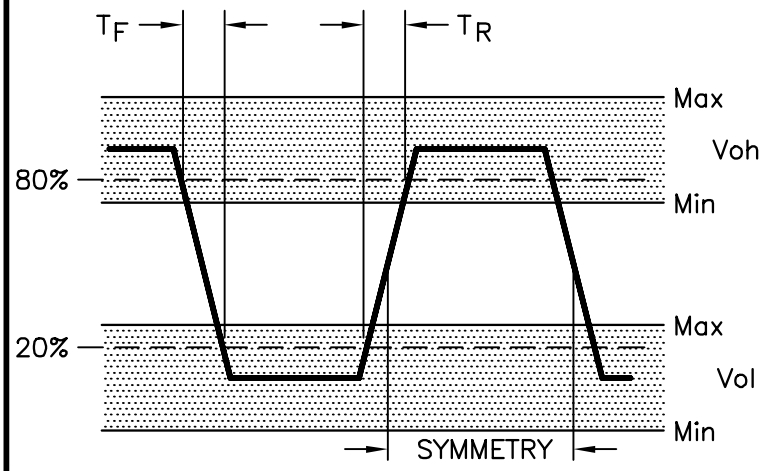


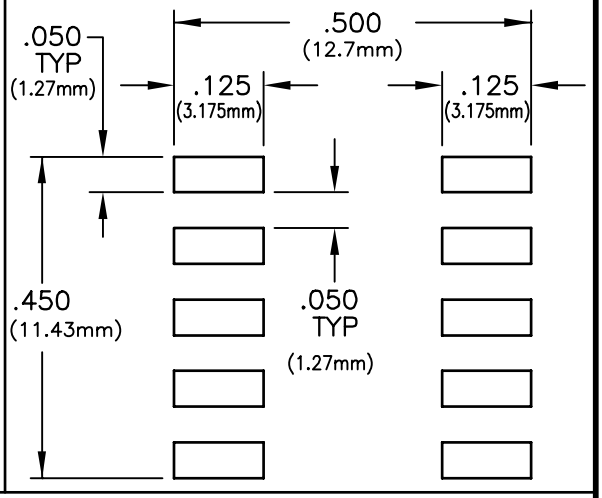


PIN	CONNECTION
1	(E/D or N/C)
2	CONTROL VOLTAGE
3	N/C
4	Vee
5	N/C
6	($\overline{Q}$ or N/C)
7	OUTPUT Q
8	INTERNAL TEST
9	Vcc
10	N/C

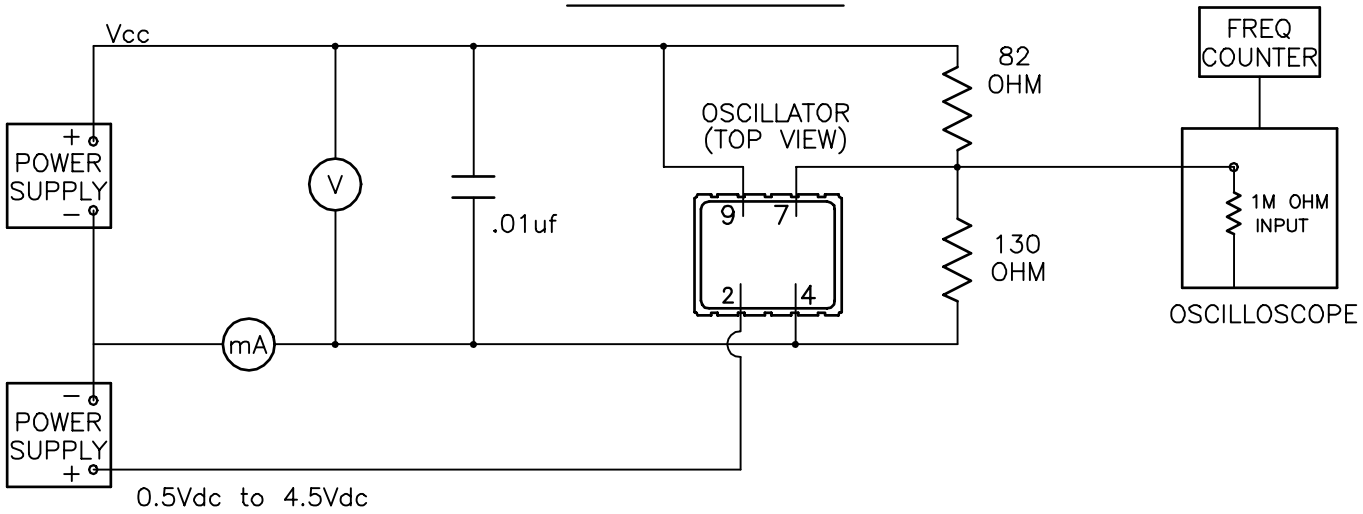
OUTPUT WAVEFORM



SUGGESTED PAD LAYOUT



TEST CIRCUIT



BULLETIN #: GA003	REV: 08	Specifications subject to change without notice.	C-W © 2000
PAGE 2 OF 2	DATE: 2/8/01	ISSUED BY:	Dimensional Tolerance: ±.02" ±.005"