PC133 144pin Unbuffered SDRAM SODIMM SPD Specification(Intel Gerber 1.2ver. base)



• Revision History

[Revision 0.0] Nov. 03, 2000 Intel Gerber 1.2ver. based PC133 SODIMM SPD Published.

• SPD Spec List

M464S0424DT2-L75/C75 M464S0424ET2-L75/C75 M464S0824DT2-L75/C75 M464S0924BT2-L75/C75 M464S0924CT2-L75/C75 M464S1724BT2-L75/C75 M464S1724CT2-L75/C75 M464S1654AT2-L75/C75 M464S1654BT2-L75/C75 M464S3254AT2-L75/C75



M464S0424DT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 4MX64 •Composition : 4MX16 *4 •Used component part # : K4S641632D-TL75/TC75 •# of rows in module : 1 row •# of banks in component : 4 banks •Feature : 1,000 mil height & double sided •Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note
Byte #		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 32MB	08h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function \$	Supported	Hex va	alue	Note
Dyte #	runction described	-7	′5	-75	5	- 1101
35	Data signal input hold time	0.8ns		081	ı	
36~61	Superset information (maybe used in future)	-		001	า	
62	SPD data revision code	Intel	1.2B	12	า	
63	Checksum for bytes 0 ~ 62			9B	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	า	
72	Manufacturing location	Onyang	g Korea	011	า	
73	Manufacturer part # (Memory module)	N	Λ	4D	h	
74	Manufacturer part # (DIMM Configuration)	2	1	34	า	
75	Manufacturer part # (Data bits)	Bla	ank	201	า	
76	Manufacturer part # (Data bits)	6	6	361	า	
77	Manufacturer part # (Data bits)	4	1	34	า	
78	Manufacturer part # (Mode & operating voltage)	5	6	531	า	
79	Manufacturer part # (Module depth)	()	30h		
80	Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	D		44h		
84	Manufacturer part # (Package type)	٦	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	321	า	
86	Manufacturer part # (Hyphen)	۳.	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	371	า	
89	Manufacturer part # (Minimum cycle time)	5	5	351	า	
90	Manufacturer part # (TBD)	Bla	ank	201	า	
91	Manufacturer revision code (For PCB)	2	2	321	า	
92	Manufacturer revision code (For component)	D-die (5	th Gen.)	44	า	
93	Manufacturing date (Week)			-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved			641	า	6
127	Reserved	Detailed PC10	00 Information	8D	h	6
128+	Unused storage locations	Unde	fined	-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.



M464S0424ET2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 4MX64 •Composition : 4MX16 *4 •Used component part # : K4S641632E-TL75/TC75 •# of rows in module : 1 row •# of banks in component : 4 banks •Feature : 1,000 mil height & double sided •Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note	
2,10 "		-75	-75		
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	12	0Ch	1	
4	# of column address on this assembly	8	08h	1	
5	# of module Rows on this assembly	1 Row	01h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	15.625us, support self refresh	80h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	1 Row of 32MB	08h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function \$	Supported	Hex va	alue	Note
Dyte #	runction described	-7	′5	-75	5	
35	Data signal input hold time	0.8ns		081	ı	
36~61	Superset information (maybe used in future)	-		001	า	
62	SPD data revision code	Intel	1.2B	12	า	
63	Checksum for bytes 0 ~ 62			9B	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	า	
72	Manufacturing location	Onyang	g Korea	011	า	
73	Manufacturer part # (Memory module)	N	Λ	4D	h	
74	Manufacturer part # (DIMM Configuration)	2	1	34	า	
75	Manufacturer part # (Data bits)	Bla	ank	201	า	
76	Manufacturer part # (Data bits)	6	6	361	า	
77	Manufacturer part # (Data bits)	4	1	34	า	
78	Manufacturer part # (Mode & operating voltage)	5	6	531	า	
79	Manufacturer part # (Module depth)	()	30h		
80	Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	E		45h		
84	Manufacturer part # (Package type)	1	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	321	า	
86	Manufacturer part # (Hyphen)	".	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	371	า	
89	Manufacturer part # (Minimum cycle time)	Ę	5	351	า	
90	Manufacturer part # (TBD)	Bla	ank	201	า	
91	Manufacturer revision code (For PCB)	2	2	321	า	
92	Manufacturer revision code (For component)	E-die (6	th Gen.)	451	า	
93	Manufacturing date (Week)			-		3
94	Manufacturing date (Year)	- 1		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved			641	า	6
127	Reserved	Detailed PC10	00 Information	8D	h	6
128+	Unused storage locations	Unde	fined	-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.



M464S0824DT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8MX64 •Composition : 4MX16 *8 •Used component part # : K4S641632D-TL75/TC75 •# of rows in module : 2 rows •# of banks in component : 4 banks •Feature : 1,250 mil height & double sided •Refresh : 4K/64ms •Contents :

•Contents :

Byte #	Function described	Function Supported	Hex value	Note	
Dyte #	r difetion described	-75	-75	Note	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	12	0Ch	1	
4	# of column address on this assembly	8	08h	1	
5	# of module Rows on this assembly	2 Rows	02h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	15.625us, support self refresh	80h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	2 Rows of 32MB	08h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function \$	Function Supported		alue	Note
byte #	Function described	-7	′5	-75	5	
35	Data signal input hold time	0.8ns		08	h	
36~61	Superset information (maybe used in future)	-		001	h	
62	SPD data revision code	Intel 1.2B		12	h	
63	Checksum for bytes 0 ~ 62			9C	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	h	
72	Manufacturing location	Onyanç	g Korea	011	h	
73	Manufacturer part # (Memory module)	Ν	Λ	4D	h	
74	Manufacturer part # (DIMM Configuration)	4	1	34	h	
75	Manufacturer part # (Data bits)	Bla	ank	201	h	
76	Manufacturer part # (Data bits)	6	3	361	h	
77	Manufacturer part # (Data bits)	2	1	34	h	
78	Manufacturer part # (Mode & operating voltage)	5	6	531	h	
79	Manufacturer part # (Module depth)	()	30h		
80	Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	[)	44h		
84	Manufacturer part # (Package type)	٦	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	321	h	
86	Manufacturer part # (Hyphen)	۳.	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	371	h	
89	Manufacturer part # (Minimum cycle time)	5	5	351	h	
90	Manufacturer part # (TBD)	Bla	ank	201	h	
91	Manufacturer revision code (For PCB)	2	2	32	h	
92	Manufacturer revision code (For component)	D-die (5	th Gen.)	44	h	
93	Manufacturing date (Week)			-		3
94	Manufacturing date (Year)			-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved			641	h	6
127	Reserved	Detailed PC10	00 Information	CD	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.



M464S0824ET2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8MX64 •Composition : 4MX16 *8 •Used component part # : K4S641632E-TL75/TC75 •# of rows in module : 2 rows •# of banks in component : 4 banks •Feature : 1,250 mil height & double sided •Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note
Dyte #	runction described	-75	-75	NOLE
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 32MB	08h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function \$	Function Supported		alue	Note
Буге #	Function described	-7	′5	-75	5	
35	Data signal input hold time	0.8ns		08	า	
36~61	Superset information (maybe used in future)	-		001	า	
62	SPD data revision code	Intel	1.2B	12	า	
63	Checksum for bytes 0 ~ 62			9C	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	ı	
72	Manufacturing location	Onyanç	g Korea	011	ı	
73	Manufacturer part # (Memory module)	Ν	Λ	4D	h	
74	Manufacturer part # (DIMM Configuration)	4	1	34	ı	
75	Manufacturer part # (Data bits)	Bla	ank	201	ı	
76	Manufacturer part # (Data bits)	6	3	361	ı	
77	Manufacturer part # (Data bits)	2	1	34	า	
78	Manufacturer part # (Mode & operating voltage)	5	6	53	า	
79	Manufacturer part # (Module depth)	()	30h		
80	Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	E		45h		
84	Manufacturer part # (Package type)	7	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	32	ı	
86	Manufacturer part # (Hyphen)	" .	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	371	ı	
89	Manufacturer part # (Minimum cycle time)	5	5	351	ı	
90	Manufacturer part # (TBD)	Bla	ank	201	ı	
91	Manufacturer revision code (For PCB)	2	2	32	ı	
92	Manufacturer revision code (For component)	E-die (6	th Gen.)	451	ı	
93	Manufacturing date (Week)			-		3
94	Manufacturing date (Year)			-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved			641	า	6
127	Reserved	Detailed PC10	00 Information	CD	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.



M464S0924BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8Mx64 •Composition : 8Mx16 *4 •Used component part # : K4S281632B-TL75/TC75 •# of rows in module : 1 row •# of banks in component : 4 banks •Feature : 1,000 mil height & double sided •Refresh : 4K/64ms

•Contents :

Dute #	Function described	Function Supported	Hex value	Note	
Byte #	Function described	-75	-75	Note	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	12	0Ch	1	
4	# of column address on this assembly	9	09h	1	
5	# of module Rows on this assembly	1 Row	01h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	15.625us, support self refresh	80h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	1 Row of 64MB	10h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function S	Function Supported		alue	Note
Byte #	Function described	-7	5	-75		
35	Data signal input hold time	0.8ns		08	า	
36~61	Superset information (maybe used in future)	-		00	า	
62	SPD data revision code	Intel 1.2B		12	า	
63	Checksum for bytes 0 ~ 62	-		A4	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	00	ı	
72	Manufacturing location	Onyang	g Korea	01	ı	
73	Manufacturer part # (Memory module)	N	1	4D	h	
74	Manufacturer part # (DIMM Configuration)	4	1	34	ı	
75	Manufacturer part # (Data bits)	Bla	ink	20	ı	
76	Manufacturer part # (Data bits)	6	3	36	า	
77	Manufacturer part # (Data bits)	4	1	34	า	
78	Manufacturer part # (Mode & operating voltage)	0	3	53	า	
79	Manufacturer part # (Module depth)	C)	30h		
80	Manufacturer part # (Module depth)	9		39h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	E	3	42h		
84	Manufacturer part # (Package type)	Т	T	54h		
85	Manufacturer part # (PCB revision & type)	2	2	32	า	
86	Manufacturer part # (Hyphen)	" -	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	37	า	
89	Manufacturer part # (Minimum cycle time)	5	5	35	า	
90	Manufacturer part # (TBD)	Bla	ink	20	า	
91	Manufacturer revision code (For PCB)	2	2	32	า	
92	Manufacturer revision code (For component)	B-die (3)	rd Gen.)	42	า	
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~12	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved	-		64	า	6
127	Reserved	Detailed PC10	00 Information	8D	h	6
128+	Unused storage locations	Unde	fined	-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S0924CT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8Mx64 •Composition : 8Mx16 *4 •Used component part # : K4S281632C-TL75/TC75 •# of rows in module : 1 row •# of banks in component : 4 banks •Feature : 1,000 mil height & double sided •Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note	
Dyte #	runction described	-75	-75	Note	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	12	0Ch	1	
4	# of column address on this assembly	9	09h	1	
5	# of module Rows on this assembly	1 Row	01h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	15.625us, support self refresh	80h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	1 Row of 64MB	10h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function	Function Supported		alue	Note
Буте #	Function described	-7	75	-75		Note
35	Data signal input hold time	0.8ns		08	h	
36~61	Superset information (maybe used in future)	-		00	h	
62	SPD data revision code	Intel	1.2B	12	h	
63	Checksum for bytes 0 ~ 62		-	A4	h	
64	Manufacturer JEDEC ID code	Sam	isung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	isung	00	h	
72	Manufacturing location	Onyan	g Korea	01	h	
73	Manufacturer part # (Memory module)	1	N	4D	h	
74	Manufacturer part # (DIMM Configuration)		4	34	h	
75	Manufacturer part # (Data bits)	Bla	ank	20	h	
76	Manufacturer part # (Data bits)		6	36	h	
77	Manufacturer part # (Data bits)		4	34	h	
78	Manufacturer part # (Mode & operating voltage)	:	S	53	h	
79	Manufacturer part # (Module depth)		0	30h		
80	Manufacturer part # (Module depth)	9		39h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-		2	32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	(С	43h		
84	Manufacturer part # (Package type)	-	Т	54h		
85	Manufacturer part # (PCB revision & type)		2	32h		
86	Manufacturer part # (Hyphen)	"	- "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)		7	37	h	
89	Manufacturer part # (Minimum cycle time)		5	35	h	
90	Manufacturer part # (TBD)	Bla	ank	20	h	
91	Manufacturer revision code (For PCB)	:	2	32	h	
92	Manufacturer revision code (For component)	C-die (4	Ith Gen.)	43	h	
93	Manufacturing date (Week)		-	-		3
94	Manufacturing date (Year)		-	-		3
95~98	Assembly serial #	-		-		4
99~12	Manufacturer specific data (may be used in future)	Unde	efined	-		5
126	Reserved		-	64	h	6
127	Reserved	Detailed PC1	00 Information	8D	h	6
128+	Unused storage locations	Unde	efined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S1724BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64 •Composition : 8MX16 *8 •Used component part # : K4S281632B-TL75/TC75 •# of rows in module : 2 rows •# of banks in component : 4 banks •Feature : 1,250 mil height & double sided •Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note	
Dyte #	r unction described	-75	-75	NOLE	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	12	0Ch	1	
4	# of column address on this assembly	9	09h	1	
5	# of module Rows on this assembly	2 Rows	02h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	15.625us, support self refresh	80h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	2 Rows of 64MB	10h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function \$	Supported	Hex va	alue	Note
Dyte #	runction described	-7	′5	-75	5	
35	Data signal input hold time	0.8ns		081	h	
36~61	Superset information (maybe used in future)	-		001	h	
62	SPD data revision code	Intel 1.2B		12	h	
63	Checksum for bytes 0 ~ 62			A5	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	h	
72	Manufacturing location	Onyang	g Korea	011	h	
73	Manufacturer part # (Memory module)	N	Λ	4D	h	
74	Manufacturer part # (DIMM Configuration)	2	1	34	h	
75	Manufacturer part # (Data bits)	Bla	ank	201	h	
76	Manufacturer part # (Data bits)	6	6	361	h	
77	Manufacturer part # (Data bits)	4	1	34	h	
78	Manufacturer part # (Mode & operating voltage)	5	6	531	h	
79	Manufacturer part # (Module depth)	1	l	31h		
80	Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	2	32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	E	3	42h		
84	Manufacturer part # (Package type)	1	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	32h		
86	Manufacturer part # (Hyphen)	".	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	371	h	
89	Manufacturer part # (Minimum cycle time)	Ę	5	351	h	
90	Manufacturer part # (TBD)	Bla	ank	201	h	
91	Manufacturer revision code (For PCB)	2	2	321	h	
92	Manufacturer revision code (For component)	B-die (3	rd Gen.)	421	h	
93	Manufacturing date (Week)			-		3
94	Manufacturing date (Year)			-		3
95~98	Assembly serial #			-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved			641	h	6
127	Reserved	Detailed PC10	00 Information	CD	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S1724CT2-L75/C75(Intel SPD 1.2B ver. based)

Organization : 16MX64
Composition : 8MX16 *8
Used component part # : K4S281632C-TL75/TC75
of rows in module : 2 rows
of banks in component : 4 banks
Feature : 1,250 mil height & double sided
Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note
Dyte #	r unction described	-75	-75	- Note
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	



PC133 SODIMM

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function	Supported	Hex va	alue	Note
Dyte #	runction described	-7	75	-75	5	
35	Data signal input hold time	0.8ns		081	ı	
36~61	Superset information (maybe used in future)	-		001	า	
62	SPD data revision code	Intel 1.2B		12	า	
63	Checksum for bytes 0 ~ 62		-	A5	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	า	
72	Manufacturing location	Onyang	g Korea	011	า	
73	Manufacturer part # (Memory module)	N	Л	4D	h	
74	Manufacturer part # (DIMM Configuration)	4	1	34	า	
75	Manufacturer part # (Data bits)	Bla	ank	201	า	
76	Manufacturer part # (Data bits)	6	6	361	า	
77	Manufacturer part # (Data bits)	4	1	34	า	
78	Manufacturer part # (Mode & operating voltage)	5	6	531	า	
79	Manufacturer part # (Module depth)		1	31h		
80	Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	2	32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	(0	43h		
84	Manufacturer part # (Package type)	-	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	32h		
86	Manufacturer part # (Hyphen)	۳.	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	371	า	
89	Manufacturer part # (Minimum cycle time)	Ę	5	351	า	
90	Manufacturer part # (TBD)	Bla	ank	201	า	
91	Manufacturer revision code (For PCB)	2	2	321	า	
92	Manufacturer revision code (For component)	C-die (4	th Gen.)	431	า	
93	Manufacturing date (Week)		-	-		3
94	Manufacturing date (Year)		-	-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved		-	641	า	6
127	Reserved	Detailed PC10	00 Information	CD	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S1654AT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64 •Composition : 16MX16 *4 •Used component part # : K4S561632A-TL75/TC75 •# of rows in module : 1 row •# of banks in component : 4 banks •Feature : 1,000 mil height & double sided •Refresh : 8K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note
Dyte #	r unction described	-75	-75	Note
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	



PC133 SODIMM

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function S	Function Supported		alue	Note
byte #	Function described	-7	5	-75	5	
35	Data signal input hold time	0.8ns		08	h	
36~61	Superset information (maybe used in future)	-		001	h	
62	SPD data revision code	Intel 1.2B		12	h	
63	Checksum for bytes 0 ~ 62	-		B7	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	h	
72	Manufacturing location	Onyang	j Korea	011	h	
73	Manufacturer part # (Memory module)	N	1	4D	h	
74	Manufacturer part # (DIMM Configuration)	4	ŀ	341	h	
75	Manufacturer part # (Data bits)	Bla	ink	201	h	
76	Manufacturer part # (Data bits)	6	5	361	h	
77	Manufacturer part # (Data bits)	4	Ļ	34	h	
78	Manufacturer part # (Mode & operating voltage)	S	6	531	h	
79	Manufacturer part # (Module depth)	1		31h		
80	Manufacturer part # (Module depth)	6	5	36h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	5	35h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	A	A Contraction of the second se	41h		
84	Manufacturer part # (Package type)	Г	-	54h		
85	Manufacturer part # (PCB revision & type)	2	2	321	h	
86	Manufacturer part # (Hyphen)	" -	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	,	37	h	
89	Manufacturer part # (Minimum cycle time)	5	5	351	h	
90	Manufacturer part # (TBD)	Bla	ink	201	h	
91	Manufacturer revision code (For PCB)	2	2	321	h	
92	Manufacturer revision code (For component)	A-die (2r	nd Gen.)	411	h	
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved	-		641	h	6
127	Reserved	Detailed PC10	0 Information	8D	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S1654BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64 •Composition : 16MX16 *4 •Used component part # : K4S561632B-TL75/TC75 •# of rows in module : 1 row •# of banks in component : 4 banks •Feature : 1,000 mil height & double sided •Refresh : 8K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note	
Dyte #	r unction described	-75	-75	Note	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	13	0Dh	1	
4	# of column address on this assembly	9	09h	1	
5	# of module Rows on this assembly	1 Row	01h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	7.8us, support self refresh self	82h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	1 Row of 128MB	20h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function S	Function Supported		alue	Note
byte #	Function described	-7	5	-75	5	
35	Data signal input hold time	0.8ns		08	า	
36~61	Superset information (maybe used in future)	-		001	า	
62	SPD data revision code	Intel 1.2B		12	า	
63	Checksum for bytes 0 ~ 62	-		B7	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	001	ſ	
72	Manufacturing location	Onyang	j Korea	011	ſ	
73	Manufacturer part # (Memory module)	Ν	1	4D	h	
74	Manufacturer part # (DIMM Configuration)	4	ļ	34	า	
75	Manufacturer part # (Data bits)	Bla	ink	201	า	
76	Manufacturer part # (Data bits)	6	6	361	า	
77	Manufacturer part # (Data bits)	4	ļ	34	า	
78	Manufacturer part # (Mode & operating voltage)	9	6	53	า	
79	Manufacturer part # (Module depth)	1		31h		
80	Manufacturer part # (Module depth)	6		36h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	5	35h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	E	3	42h		
84	Manufacturer part # (Package type)	1	-	54h		
85	Manufacturer part # (PCB revision & type)	2	2	32	ı	
86	Manufacturer part # (Hyphen)	" -	. "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	,	37	า	
89	Manufacturer part # (Minimum cycle time)	5	5	351	า	
90	Manufacturer part # (TBD)	Bla	nk	201	า	
91	Manufacturer revision code (For PCB)	2	2	32	า	
92	Manufacturer revision code (For component)	B-die (3)	rd Gen.)	42	า	
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved	-		64	า	6
127	Reserved	Detailed PC10	00 Information	8D	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S3254AT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 32MX64 •Composition : 16MX16 *8 •Used component part # : K4S561632A-TL75/TC75 •# of rows in module : 2 rows •# of banks in component : 4 banks •Feature : 1,250 mil height & double sided •Refresh : 8K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note	
byte #	r difetion described	-75	-75	Note	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h		
2	Fundamental memory type	SDRAM	04h		
3	# of row address on this assembly	13	0Dh	1	
4	# of column address on this assembly	9	09h	1	
5	# of module Rows on this assembly	2 Rows	02h		
6	Data width of this assembly	64 bits	40h		
7	Data width of this assembly	-	00h		
8	Voltage interface standard of this assembly	LVTTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2	
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2	
11	DIMM configuration type	Non parity	00h		
12	Refresh rate & type	7.8us, support self refresh self	82h		
13	Primary SDRAM width	x16	10h		
14	Error checking SDRAM width	None	00h		
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h		
18	SDRAM device attributes : CAS latency	3	04h		
19	SDRAM device attributes : CS latency	0 CLK	01h		
20	SDRAM device attributes : Write latency	0 CLK	01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh		
23	SDRAM cycle time @CAS latency of 2	-	00h	2	
24	SDRAM access time @CAS latency of 2	-	00h	2	
25	SDRAM cycle time @CAS latency of 1	-	00h	2	
26	SDRAM access time @CAS latency of 1	-	00h	2	
27	Minimum row precharge time (=tRP)	20ns	14h		
28	Minimum row active to row active delay (tRRD)	15ns	0Fh		
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h		
30	Minimum activate precharge time (=tRAS)	45ns	2Dh		
31	Module Row density	2 Rows of 128MB	20h		
32	Command and Address signal input setup time	1.5ns	15h		
33	Command and Address signal input hold time	0.8ns	08h		
34	Data signal input setup time	1.5ns	15h		



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function	Function Supported		alue	Note
Dyte #	Function described	-7	75	-75	5	
35	Data signal input hold time	0.8ns		08	h	
36~61	Superset information (maybe used in future)	-		00	h	
62	SPD data revision code	Intel 1.2B		12	h	
63	Checksum for bytes 0 ~ 62		-	B8	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	00	h	
72	Manufacturing location	Onyanç	g Korea	01	h	
73	Manufacturer part # (Memory module)	Ν	N	4D	h	
74	Manufacturer part # (DIMM Configuration)	2	4	34	h	
75	Manufacturer part # (Data bits)	Bla	ank	20	h	
76	Manufacturer part # (Data bits)	6	6	36	h	
77	Manufacturer part # (Data bits)	4	4	34	h	
78	Manufacturer part # (Mode & operating voltage)	5	S	53	h	
79	Manufacturer part # (Module depth)	:	3	33h		
80	Manufacturer part # (Module depth)	2		32h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5		35h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	ŀ	4	41h		
84	Manufacturer part # (Package type)	-	Г	54h		
85	Manufacturer part # (PCB revision & type)	2	2	32	h	
86	Manufacturer part # (Hyphen)	".	- "	2D	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7	7	37	h	
89	Manufacturer part # (Minimum cycle time)	Ę	5	35	h	
90	Manufacturer part # (TBD)	Bla	ank	20	h	
91	Manufacturer revision code (For PCB)	2	2	32	h	
92	Manufacturer revision code (For component)	A-die (2)	nd Gen.)	41	h	
93	Manufacturing date (Week)		-	-		3
94	Manufacturing date (Year)		-	-		3
95~98	Assembly serial #		-	-		4
99~125	Manufacturer specific data (may be used in future)	Unde	fined	-		5
126	Reserved		-	64	h	6
127	Reserved	Detailed PC10	00 Information	CD	h	6
128+	Unused storage locations	Unde	fined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.



M464S3254BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 32MX64 •Composition : 16MX16 *8 •Used component part # : K4S561632B-TL75/TC75 •# of rows in module : 2 rows •# of banks in component : 4 banks •Feature : 1,250 mil height & double sided •Refresh : 8K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note
byte #	r difetion described	-75	-75	note
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	



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SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function	Supported	Hex va	alue	Note
Буге #	Function described	-7	75	-75	5	
35	Data signal input hold time	0.8ns		081	า	
36~61	Superset information (maybe used in future)	-		001	า	
62	SPD data revision code	Intel 1.2B		121	า	
63	Checksum for bytes 0 ~ 62		-	B8I	h	
64	Manufacturer JEDEC ID code	Sam	sung	CE	h	
65~71	Manufacturer JEDEC ID code	Sam	sung	00	ſ	
72	Manufacturing location	Onyang	g Korea	011	ſ	
73	Manufacturer part # (Memory module)	Π	N	4DI	h	
74	Manufacturer part # (DIMM Configuration)	4	4	34	า	
75	Manufacturer part # (Data bits)	Bla	ank	201	า	
76	Manufacturer part # (Data bits)	(6	361	า	
77	Manufacturer part # (Data bits)	4	4	34	า	
78	Manufacturer part # (Mode & operating voltage)	5	S	531	า	
79	Manufacturer part # (Module depth)	:	3	33h		
80	Manufacturer part # (Module depth)	2		32h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5		35h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	E	3	42h		
84	Manufacturer part # (Package type)	-	Г	54h		
85	Manufacturer part # (PCB revision & type)	:	2	321	า	
86	Manufacturer part # (Hyphen)	".	- "	2DI	h	
87	Manufacturer part # (Power)	L	С	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	-	7	371	า	
89	Manufacturer part # (Minimum cycle time)		5	351	า	
90	Manufacturer part # (TBD)	Bla	ank	201	า	
91	Manufacturer revision code (For PCB)	:	2	321	า	
92	Manufacturer revision code (For component)	B-die (3	rd Gen.)	421	า	
93	Manufacturing date (Week)		-	-		3
94	Manufacturing date (Year)		-	-		3
95~98	Assembly serial #		-	-		4
99~125	Manufacturer specific data (may be used in future)	Unde	efined	-		5
126	Reserved		-	641	า	6
127	Reserved	Detailed PC1	00 Information	CD	h	6
128+	Unused storage locations	Unde	efined	-		5

Note: 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsungs own purpose.

