

μ A7307

1.6 WATT AUDIO AMPLIFIER FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μ A7307 is an integrated monolithic audio amplifier in an 8-pin plastic package. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use as a low frequency class B amplifier with wide range of supply voltage (3 to 16 V) and is primarily designed for low voltage portable radios and industrial applications where limited space and power consumption are important.

- MINIMUM WORKING VOLTAGE OF 3 V
- LOW QUIESCENT CURRENT
- LOW NUMBER OF EXTERNAL COMPONENTS
- GOOD RIPPLE REJECTION
- NO CROSS-OVER DISTORTION
- TYPICAL OUTPUT POWER:

1.6 W AT	9 V - 4 Ω
1.2 W AT	9 V - 8 Ω
0.75 W AT	6 V - 4 Ω
0.5 W AT	6 V - 8 Ω
0.22 W AT	3.5 V - 4 Ω
0.09 W AT	3 V - 4 Ω

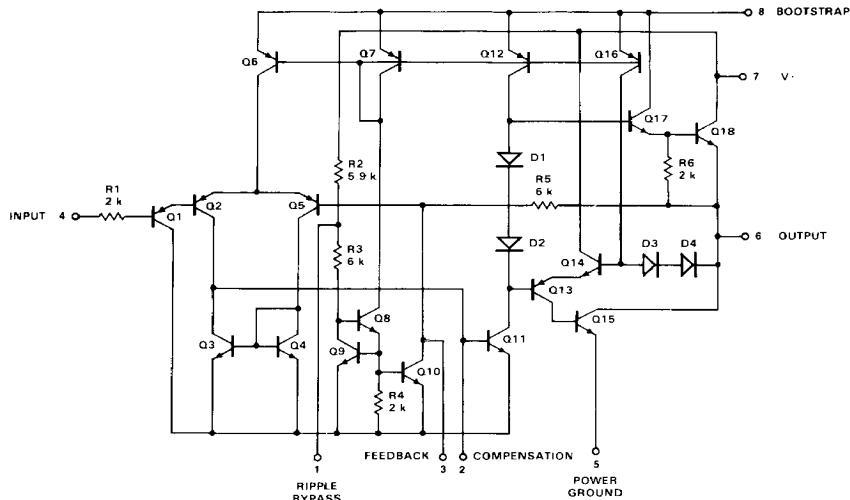
ABSOLUTE MAXIMUM RATINGS

Peak Voltage (Pin 8)	24 V
Supply Voltage	16 V
Output Peak Current	1.0 A
Power Dissipation at $T_{amb} \leq 50^\circ C$	1.05 W
Storage and Junction Temperature	-40°C to 150°C
Lead Temperature (Soldering 10 s)	260°C

THERMAL DATA

θ_{j-amb} Thermal Resistance Junction-Ambient (copper frame) max 95°C/W

EQUIVALENT CIRCUIT



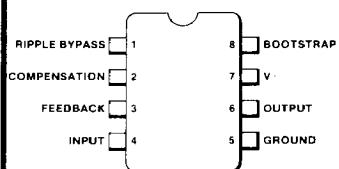
CONNECTION DIAGRAM

8-PIN MINI-DIP

*TOP VIEW

PACKAGE OUTLINE 9T

PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
7307C	μ A7307TC

ELECTRICAL CHARACTERISTICS: Power output measured at pin 6, $T_A = 25^\circ\text{C}$ unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		3		16	V
Quiescent Output Voltage (Pin 6)	$V_+ = 9 \text{ V}$	4	4.5	5	V
Quiescent Drain Current	$V_+ = 9 \text{ V}$		4	9	mA
Bias Current (Pin 4)	$V_+ = 9 \text{ V}$		0.1	0.7	μA
Power Output, Figure 1	THD = 10%, $R_{FB} = 120 \Omega$, $f = 1 \text{ kHz}$ $V_+ = 12 \text{ V}$, $R_L = 8 \Omega$ $V_+ = 9 \text{ V}$, $R_L = 4 \Omega$ $V_+ = 9 \text{ V}$, $R_L = 8 \Omega$ $V_+ = 6 \text{ V}$, $R_L = 4 \Omega$ $V_+ = 3.5 \text{ V}$, $R_L = 4 \Omega$ $V_+ = 3 \text{ V}$, $R_L = 4 \Omega$	0.9	2.0 1.6 1.2 0.75 0.22 0.09		W W W W W W
Input Sensitivity, Figure 1	$P_{OUT} = 1.2 \text{ W}$, $R_L = 8 \Omega$, $V_+ = 9 \text{ V}$, $f = 1 \text{ kHz}$ $R_{FB} = 33 \Omega$ $R_{FB} = 120 \Omega$		16 60	24 82	mV mV
Input Sensitivity, Figure 1	$P_{OUT} = 50 \text{ mW}$, $R_L = 8 \Omega$, $V_+ = 9 \text{ V}$, $f = 1 \text{ kHz}$ $R_{FB} = 33 \Omega$ $R_{FB} = 120 \Omega$			3.5 12	mV mV
Input Resistance			5		M Ω
Frequency Response (-3 dB) Figure 1	$V_+ = 9 \text{ V}$, $R_L = 8 \Omega$, $R_{FB} = 120 \Omega$ $C_{FB} = 680 \text{ pF}$ $C_{FB} = 220 \text{ pF}$		25- 7000 25- 20,000		Hz Hz
Total Harmonic Distortion Figure 1	$P_{OUT} = 500 \text{ mW}$, $R_L = 8 \Omega$, $V_+ = 9 \text{ V}$, $f = 1 \text{ kHz}$ $R_{FB} = 33 \Omega$ $R_{FB} = 120 \Omega$		0.8 0.4		% %
Voltage Gain (Open Loop)	$V_+ = 9 \text{ V}$, $R_L = 8 \Omega$, $f = 1 \text{ kHz}$		75		dB
Voltage Gain (Closed Loop)	$V_+ = 9 \text{ V}$, $R_L = 8 \Omega$, $f = 1 \text{ kHz}$ $R_{FB} = 33 \Omega$ $R_{FB} = 120 \Omega$	31	45 34	37	dB dB
Input Noise Voltage	$V_+ = 9 \text{ V}$, BW (-3.0 dB) = 25-20,000 Hz		3.5		μV
Input Noise Current	$V_+ = 9 \text{ V}$, BW (-3.0 dB) = 25-20,000 Hz		0.4		nA
Signal Plus Noise to Noise Ratio	$V_+ = 9 \text{ V}$, $R_L = 8 \Omega$, $R_{FB} = 120 \Omega$ BW (-3.0 dB) = 25-20,000 Hz $R_1 = 100 \text{ k}\Omega$, $P_{OUT} = 1.2 \text{ W}$			70	dB
Supply Voltage Rejection, Figure 2	$V = 9 \text{ V}$, $R_L = 8 \Omega$, f (ripple) = 100 Hz, $C_6 = 50 \mu\text{F}$, $R_{FB} = 120 \Omega$			42	dB

APPLICATIONS INFORMATION

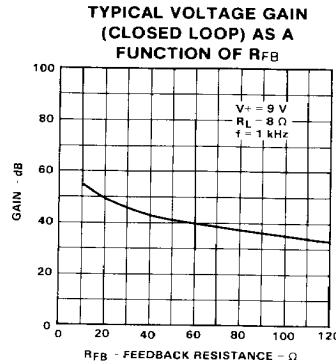
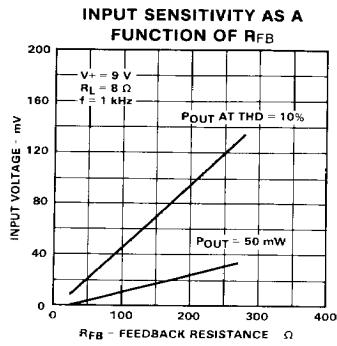
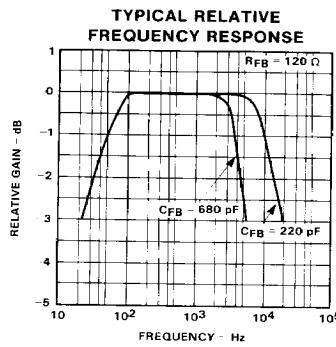
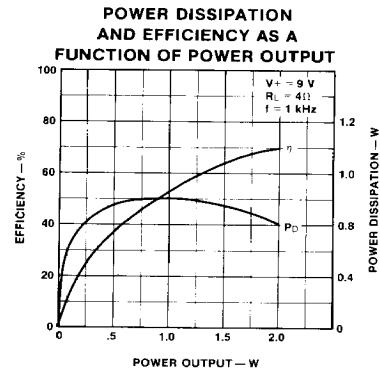
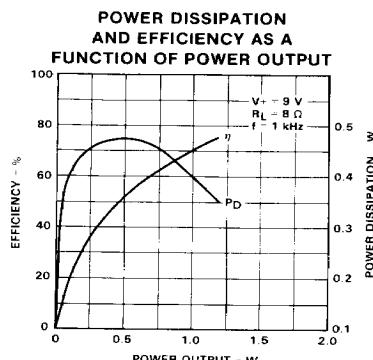
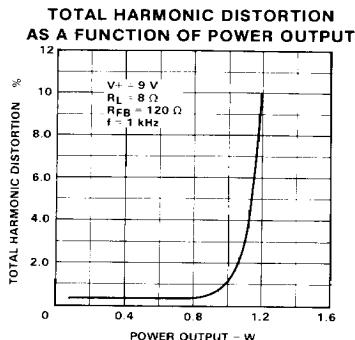
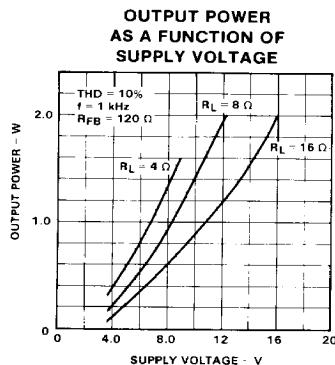
Two typical application circuits are shown in Figures 1 and 2. The ripple bypass capacitor C_6 may be omitted in most battery operated applications or where high ripple rejection is not required.

Resistor R_2 must be included in series with C_3 to assure stable operation of the μ A7307.

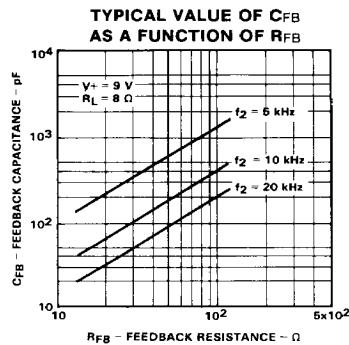
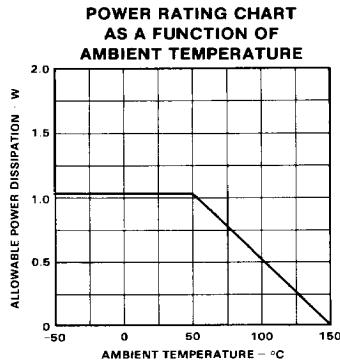
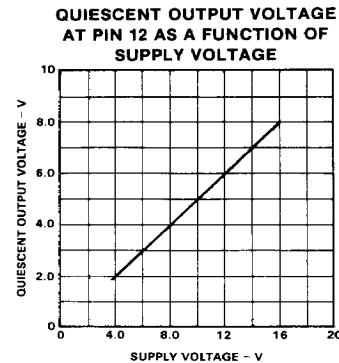
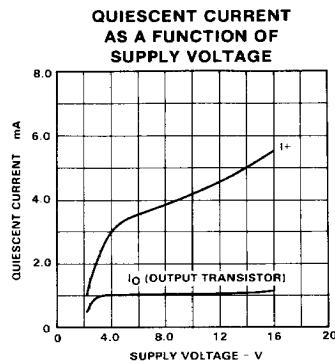
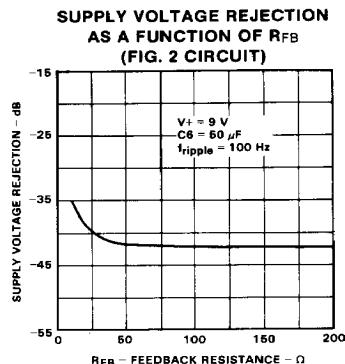
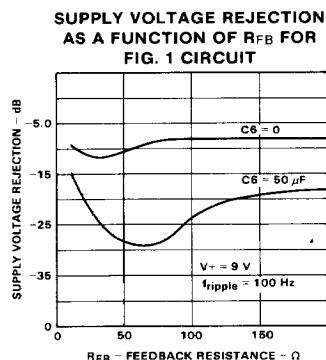
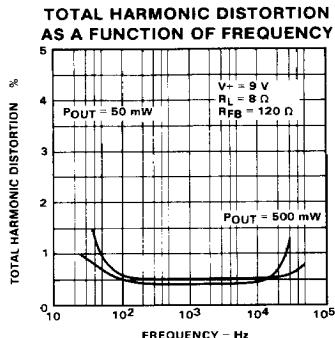
A PC board layout for the circuit of Figure 1 is shown to scale in Figure 3. A photograph of a finished module is shown in Figure 4.

The PC board layout for the circuit of Figure 2 is shown to scale in Figure 5, and a photograph is shown in Figure 6.

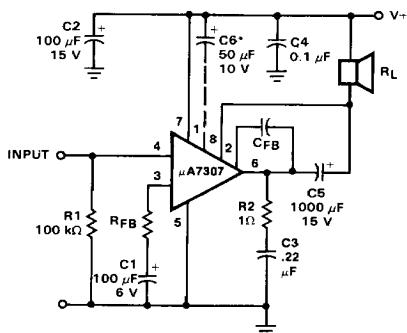
TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES



TEST AND APPLICATION CIRCUITS



*Capacitor C6 must be used when high ripple rejection is desired.

Fig. 1 Circuit Diagram with Load Connected to the Supply Voltage

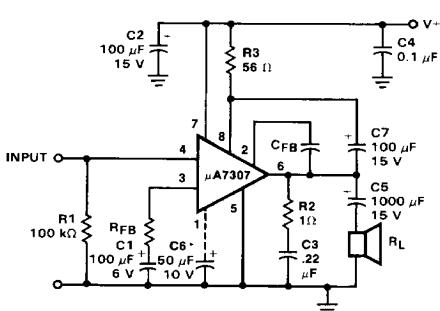


Fig. 2 Circuit Diagram with Load Connected to Ground



Bottom View

Fig. 3 1:1 Scale P.C. Board Layout for Circuit of Figure 1

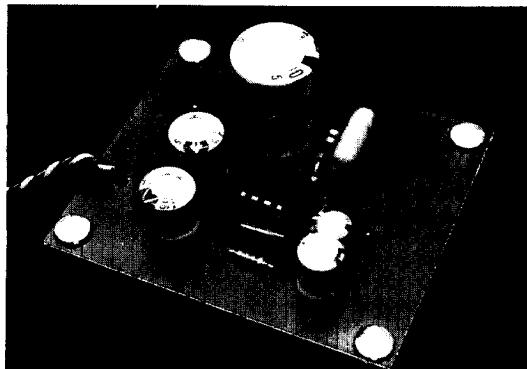
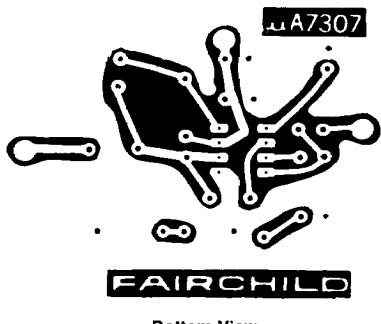


Fig. 4 Photograph of Assembled Board for Figure 1



Bottom View

Fig. 5 1:1 Scale P.C. Board Layout for Circuit of Figure 2

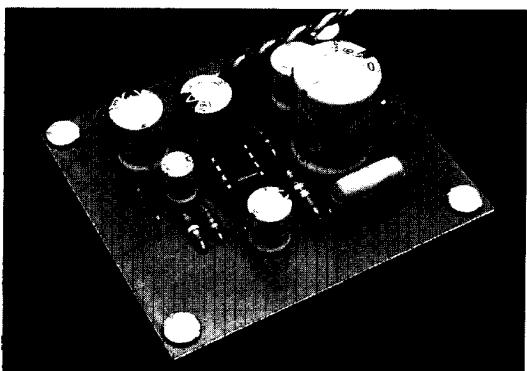


Fig. 6 Photograph of Assembled Board for Figure 2