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Semiconductor Product Information

Product Preview

DSP56012P/D
(Motorola Order Number)
Rev. 0, 09/98

DSP56012 24-Bit DVD Digital Signal Processor

Motorola developed the DSP56012 as a high-performance programmable digital signal processor (DSP) for digital versatile disc (DVD), high-definition television (HDTV), and advanced set-top audio decoding. The DSP56012 is optimized with audio-specific peripherals and customized memory configuration, and may be programmed with Motorola's certified software for Dolby AC-3 5.1 Channel Surround, Dolby Pro Logic, and MPEG1 Layer 2. These applications use Motorola's 24-bit DSP56000 architecture and are the highest quality solutions available. Flexible peripheral modules and interface software allow simple connection to a wide variety of video/ system decoders. In addition, the DSP56012 offers switchable memory space configuration, a large user-definable program ROM, two independent data RAMs and ROMs, a serial audio interface (SAI), Serial host interface (SHI), parallel host interface (HI) with Direct Memory Access (DMA) for communicating with other processors, dedicated I/O lines, on-chip phase-locked loop (PLL), On-Chip Emulation (OnCE™) port, and an on-chip digital audio transmitter (DAX). Figure 1 shows the functional blocks of the DSP56012.

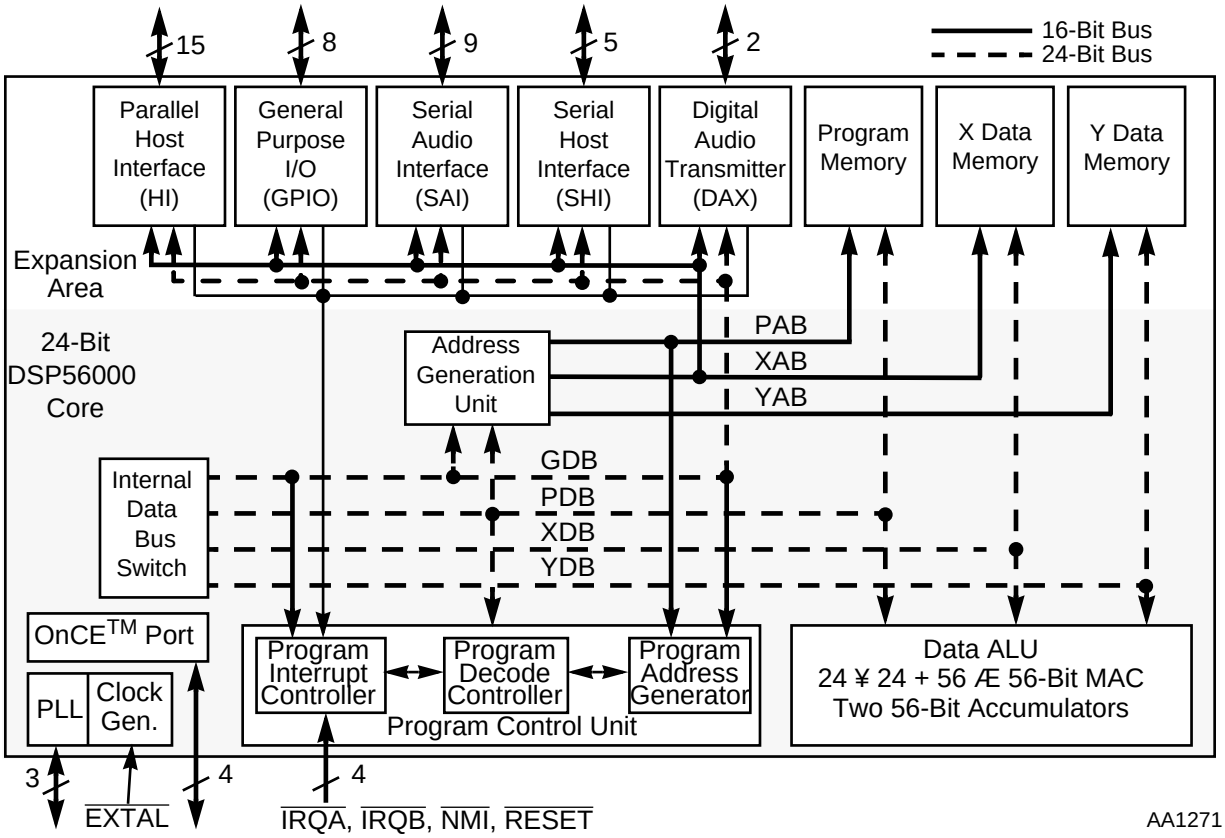

Figure 1 DSP56012 Block Diagram

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Features

Digital Signal Processing Core

- Efficient, object-code compatible, 24-bit DSP56000 family DSP engine
- 47.5 million instructions per second (MIPS) with 21.05 ns instruction cycle at 95 MHz
- Highly parallel instruction set with unique DSP addressing modes
- Two 56-bit accumulators including extension byte
- Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
- Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
- 56-bit addition/subtraction in 1 instruction cycle
- Fractional and integer arithmetic with support for multi-precision arithmetic
- Hardware support for block-floating point fast fourier transforms (FFT)
- Hardware nested DO loops
- Zero-overhead fast interrupts (2 instruction cycles)
- PLL-based clocking with a wide range of frequency multiplications (1 to 4096) and power saving clock divider (2^i: i = 0 to 15), which reduces clock noise
- Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories

Memory

- Modified Harvard architecture allows simultaneous access to program and data memories
- 15360 × 24-bit on-chip program ROM[1]
- 4096 × 24-bit on-chip X data RAM and 3584 × 24-bit on-chip X data ROM[1]
- 4352 × 24-bit on-chip Y data RAM and 2048 × 24-bit on-chip Y data ROM[1]
- 256 × 24-bit on-chip program RAM and 32 × 24-bit bootstrap ROM
- As much as 2304 × 24 bits of X and Y data RAM can be switched to program RAM, giving a total of 2560 × 24 bits of program RAM

1. These ROMs may be factory programmed with data/program provided by the application developer.

Table 1 lists the memory configurations of the DSP56012.

Table 1. DSP56012 Internal Memory Configurations

Memory Type	No Switch (PEA = 0, PEB = 0)	Switch A (PEA = 1, PEB = 0)	Switch B (PEA = 0, PEB = 1)	Switch A+B (PEA = 1, PEB = 1)
Program RAM	0.25K	1.0K	1.75K	2.5K
X data RAM	4.0K	3.25K	3.25K	2.5K
Y data RAM	4.25K	4.25K	3.5K	3.5K
Program ROM	15K	15K	15K	15K
X data ROM	3.5K	3.5K	3.5K	3.5K
Y data ROM	2.0K	2.0K	2.0K	2.0K

Peripheral and Support Circuits

- SAI includes:
  - — Two receivers and three transmitters
  - — Master or slave capability
  - — I^2S, Sony, and Matsushita audio protocol implementations
  - — Two sets of SAI interrupt vectors
- SHI features:
  - — Single master capability
  - — SPI and I^2C protocols
  - — 10-word receive FIFO
  - — Support for 8-, 16- and 24-bit words.
- Byte-wide parallel host interface with DMA support capable of reconfiguration as 15 general purpose input/output (GPIO) lines
- DAX features one serial transmitter capable of supporting S/PDIF, IEC958, CP-340, and AES/EBU formats.
- Eight dedicated, independent, programmable GPIO lines
- On-chip peripheral registers memory mapped in data memory space
- OnCE port for unobtrusive, processor speed-independent debugging
- Software programmable PLL-based frequency synthesizer for the core clock
- Power saving wait and stop modes
- Fully static, HCMOS design from specified operating frequency down to dc
- 100-pin plastic thin quad flat pack (TQFP) surface-mount package
- 5 V power supply

Documentation

Table 2 lists the documents that provide a complete description of the DSP56012 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 2. Additional DSP56012 Documentation

Document Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56012 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56012UM/AD
DSP56012 Technical Data	Electrical and timing specifications; pin and package descriptions	DSP56012/D

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