
HN58V256A Series

HN58V257A Series

256k EEPROM (32-kword × 8-bit)
Ready/Busy and $\overline{\text{RES}}$ function (HN58V257A)

HITACHI

ADE-203-357D (Z)
Rev. 4.0
Oct. 24, 1997

Description

The Hitachi HN58V256A and HN58V257A are electrically erasable and programmable ROMs organized as 32768-word × 8-bit. They have realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

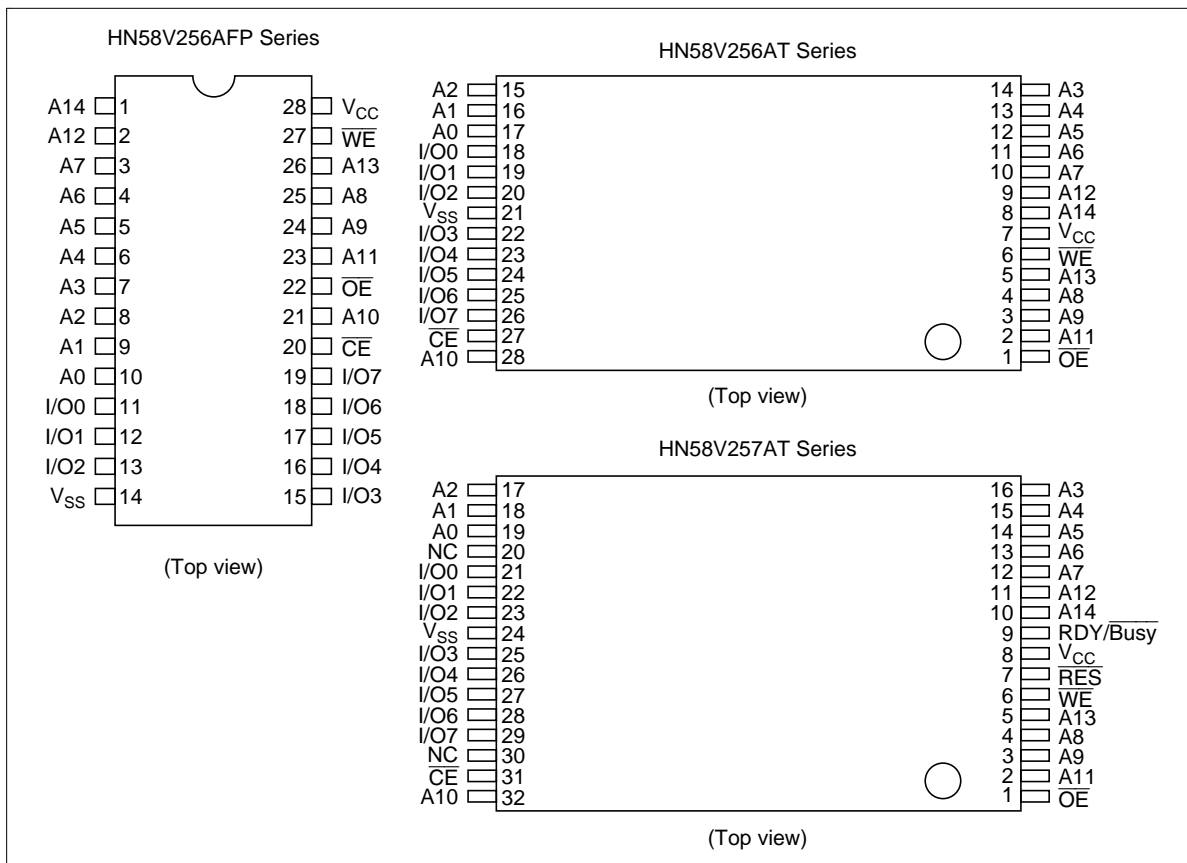
- Single 3 V supply: 2.7 to 5.5 V
- Access time: 120 ns max
- Power dissipation:
 - Active: 20 mW/MHz, (typ)
 - Standby: 110 μ W (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Ready/Busy (only the HN58V257A series)
- Data polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin (only the HN58V257A series)
- Industrial versions (Temperature range: – 20 to 85°C and – 40 to 85°C) are also available.

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Ordering Information

Type No.	Access time	Package
HN58V256AFP-12	120 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58V256AT-12	120 ns	28-pin plastic TSOP (TFP-28DB)
HN58V257AT-12	120 ns	8 × 14 mm ² 32-pin plastic TSOP (TFP-32DA)

Pin Arrangement



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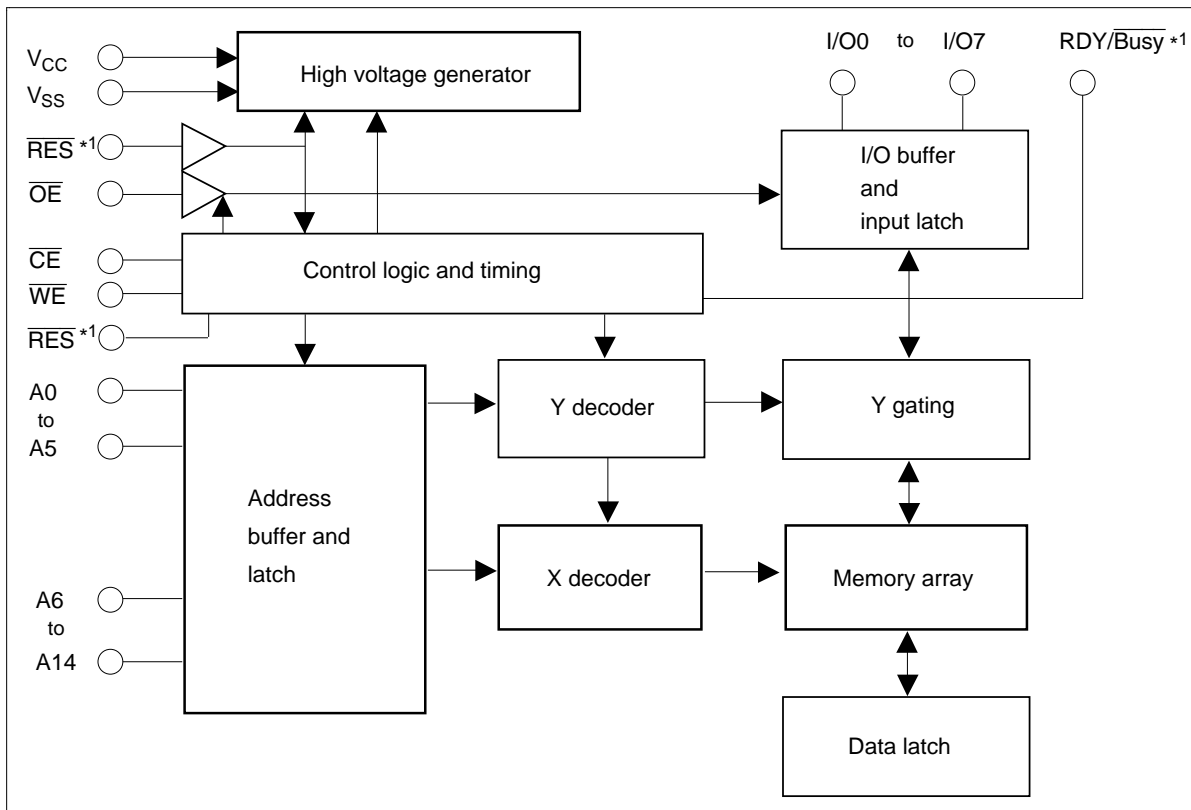
Pin Description

Pin name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
\overline{OE}	Output enable
\overline{CE}	Chip enable
\overline{WE}	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/\overline{Busy}^{*1}	Ready busy
\overline{RES}^{*1}	Reset
NC	No connection

Note: 1. This function is supported by only the HN58V257A series.

Block Diagram

Note: 1. This function is supported by only the HN58V257A series.



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Operation Table

Operation	\overline{CE}	\overline{OE}	\overline{WE}	\overline{RES}^{*3}	RDY/\overline{Busy}^{*3}	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H^{*1}	High-Z	Dout
Standby	V_{IH}	\times^{*2}	\times	\times	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write inhibit	\times	\times	V_{IH}	\times	—	—
	\times	V_{IL}	\times	\times	—	—
Data polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data out (I/O7)
Program reset	\times	\times	\times	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating condition.

2. \times : Don't care

3. This function is supported by only the HN58V267A series.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.6 to +7.0	V
Input voltage relative to V_{SS}	V_{in}	-0.5 ^{*1} to +7.0 ^{*3}	V
Operating temperature range ^{*2}	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Notes: 1. $V_{in\ min} = -3.0\ V$ for pulse width $\leq 50\ ns$

2. Including electrical characteristics and data retention

3. Should not exceed $V_{CC} + 1.0\ V$.

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Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	-0.3* ¹	—	0.6	V
	V_{IH}	1.9* ²	—	$V_{CC} + 0.3$ * ³	V
	V_H * ⁴	$V_{CC} - 0.5$	—	$V_{CC} + 1.0$	V
Operating temperature	T_{opr}	0	—	70	°C

- Notes: 1. V_{IL} min: -1.0 V for pulse width ≤ 50 ns.
 2. V_{IH} min for $V_{CC} = 3.6$ to 5.5 V is 2.4 V.
 3. V_{IH} max: $V_{CC} + 1.0$ V for pulse width ≤ 50 ns.
 4. This function is supported by only the HN58V257A series.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 2.7$ to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2* ¹	μA	$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V
Output leakage current	I_{LO}	—	—	2	μA	$V_{CC} = 5.5$ V, $V_{out} = 5.5/0.4$ V
Standby V_{CC} current	I_{CC1}	—	—	20	μA	$\overline{CE} = V_{CC}$
	I_{CC2}	—	—	1	mA	$\overline{CE} = V_{IH}$
Operating V_{CC} current	I_{CC3}	—	—	8	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 1 μs at $V_{CC} = 3.6$ V
		—	—	12	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 1 ns at $V_{CC} = 5.5$ V
		—	—	12	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 120 μs at $V_{CC} = 3.6$ V
		—	—	30	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 120 ns at $V_{CC} = 5.5$ V
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1$ mA
Output high voltage	V_{OH}	$V_{CC} \times 0.8$	—	—	V	$I_{OH} = -400$ μA

- Note: 1. I_{LI} on $\overline{RES} = 100$ μA max (only the HN58V257A series)

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Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V (V_{CC} ≤ 3.6V), 0.4V to 3.0 V (V_{CC} > 3.6 V)
0 V to V_{CC} (RES pin*2)
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 1.8 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.5 V, 1.5 V

Read Cycle

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-12						
Parameter	Symbol	Min	Max	Unit	Test conditions	
Address to output delay	t _{ACC}	—	120	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
\overline{CE} to output delay	t _{CE}	—	120	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
\overline{OE} to output delay	t _{OE}	10	60	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	
Address to output hold	t _{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
\overline{OE} (\overline{CE}) high to output float*1	t _{DF}	0	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	
\overline{RES} low to output float*1,2	t _{DFR}	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
\overline{RES} to output delay*2	t _{RR}	0	600	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	

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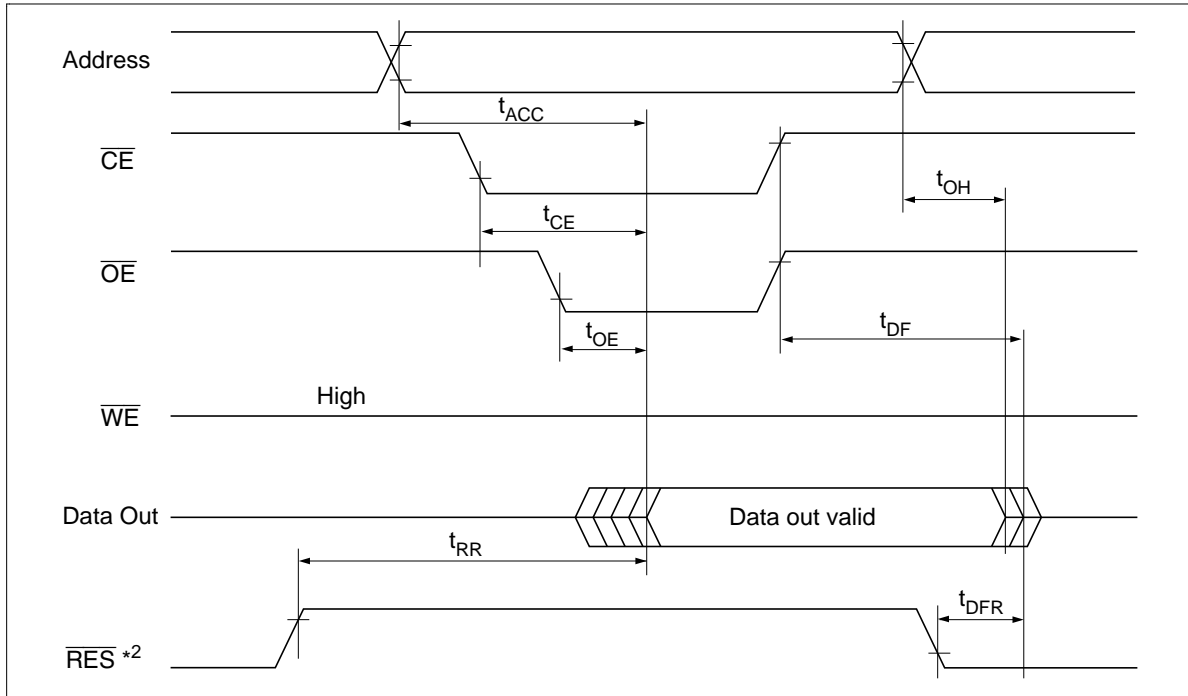
Write Cycle

Parameter	Symbol	Min* ³	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
\overline{CE} to write setup time (\overline{WE} controlled)	t_{CS}	0	—	—	ns	
\overline{CE} hold time (\overline{WE} controlled)	t_{CH}	0	—	—	ns	
\overline{WE} to write setup time (\overline{CE} controlled)	t_{WS}	0	—	—	ns	
\overline{WE} hold time (\overline{CE} controlled)	t_{WH}	0	—	—	ns	
\overline{OE} to write setup time	t_{OES}	0	—	—	ns	
\overline{OE} hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	70	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
\overline{WE} pulse width (\overline{WE} controlled)	t_{WP}	200	—	—	ns	
\overline{CE} pulse width (\overline{CE} controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.3	—	30	μ s	
Byte load window	t_{BL}	100	—	—	μ s	
Write cycle time	t_{WC}	—	—	10^{*4}	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0^{*5}	—	—	ns	
Reset protect time* ²	t_{RP}	100	—	—	μ s	
Reset high time* ^{2,6}	t_{RES}	1	—	—	μ s	

- Notes:
- t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
 - This function is supported by only the HN58V257A series.
 - Use this device in longer cycle than this value.
 - t_{WC} must be longer than this value unless polling techniques or $\overline{RDY}/\overline{Busy}$ (only the HN58V257A series) are used. This device automatically completes the internal write operation within this value.
 - Next read or write operation can be initiated after t_{DW} if polling techniques or $\overline{RDY}/\overline{Busy}$ (only the HN58V257A series) are used.
 - This parameter is sampled and not 100% tested.
 - A6 through A14 are page addresses and these addresses are latched at the first falling edge of \overline{WE} .
 - A6 through A14 are page addresses and these addresses are latched at the first falling edge of \overline{CE} .
 - See AC read characteristics.

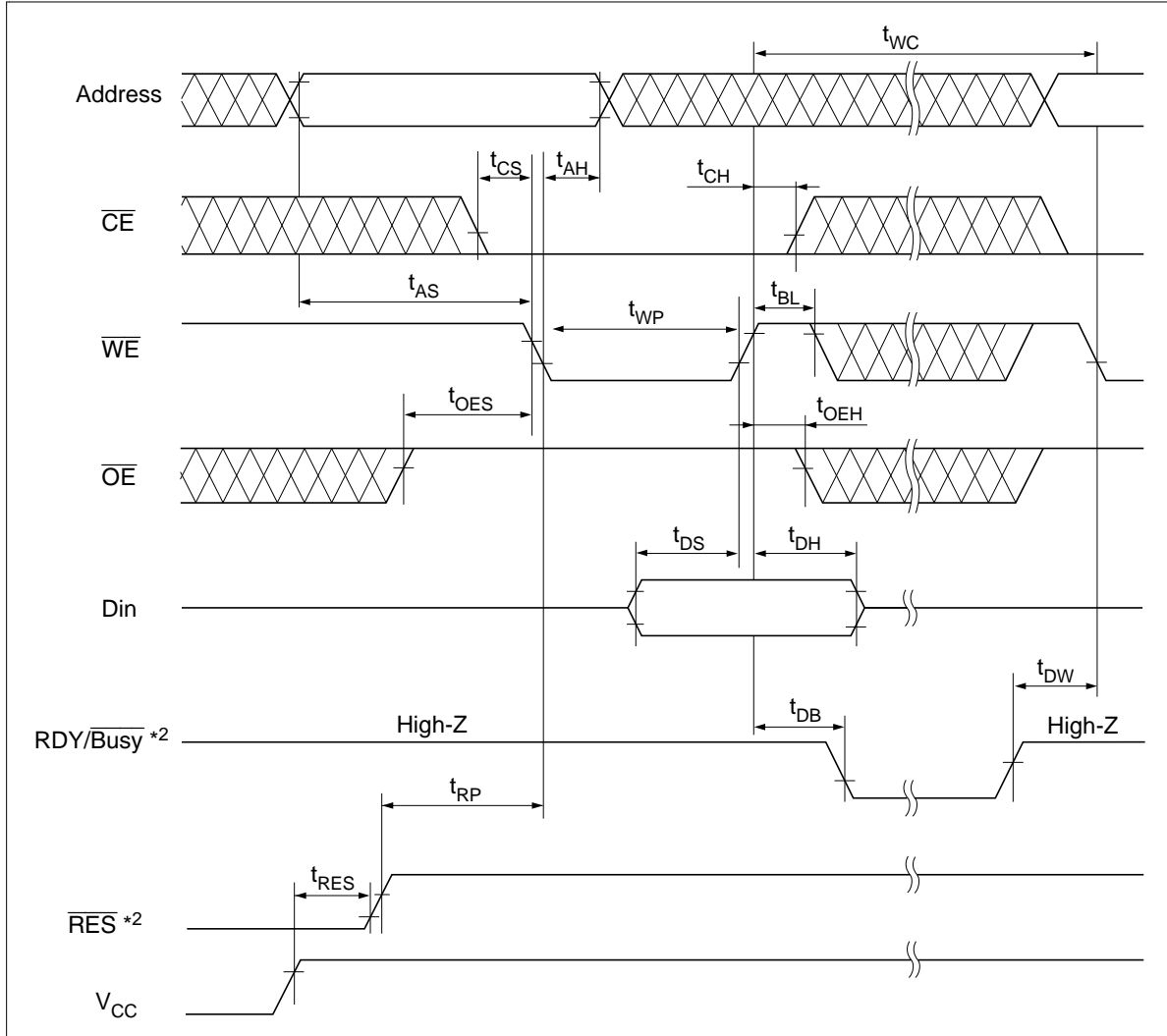
HN58V256A Series HN58V257A Series

Read Timing Waveform



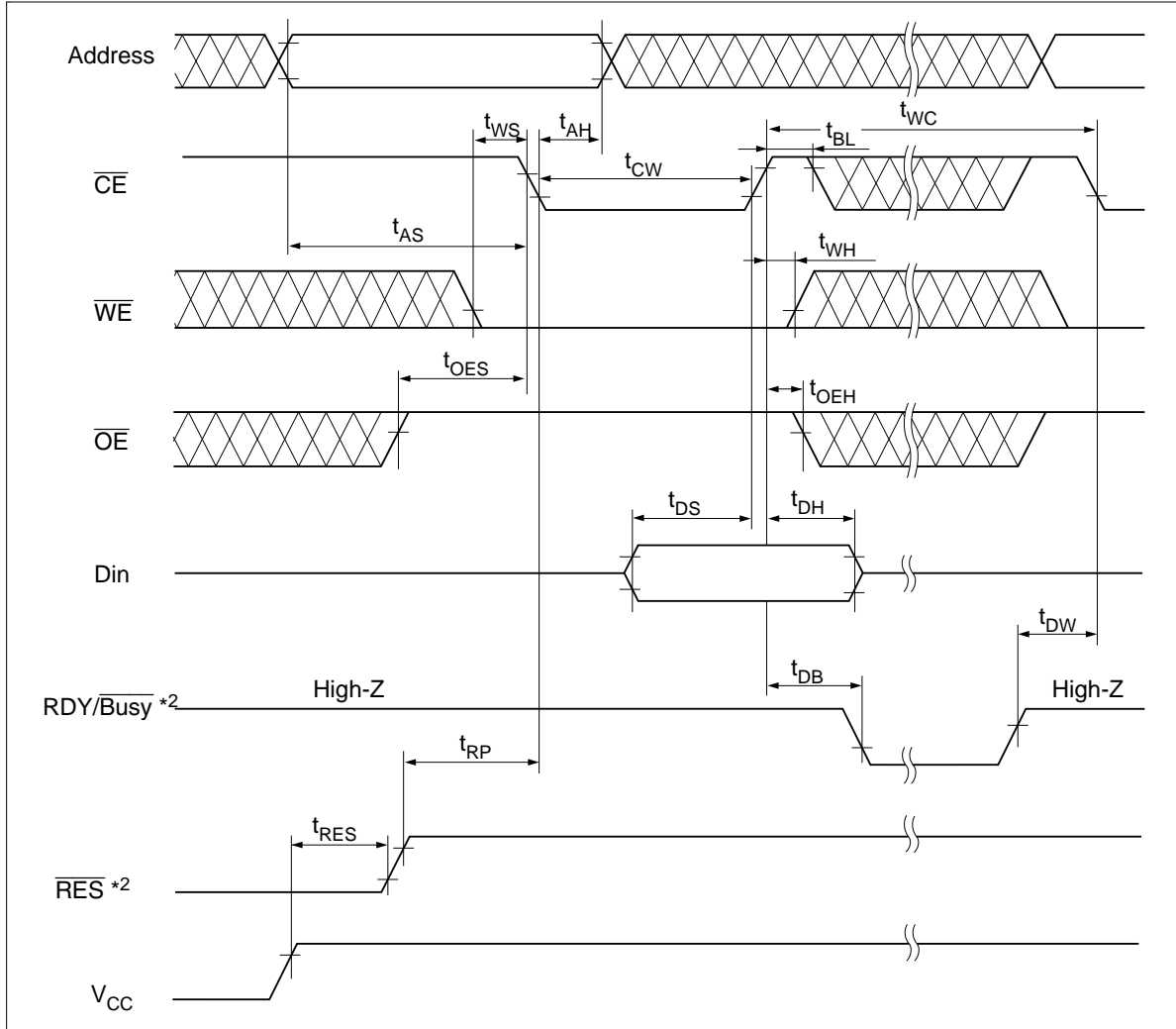
HN58V256A Series, HN58V257A Series

Byte Write Timing Waveform (1) (\overline{WE} Controlled)



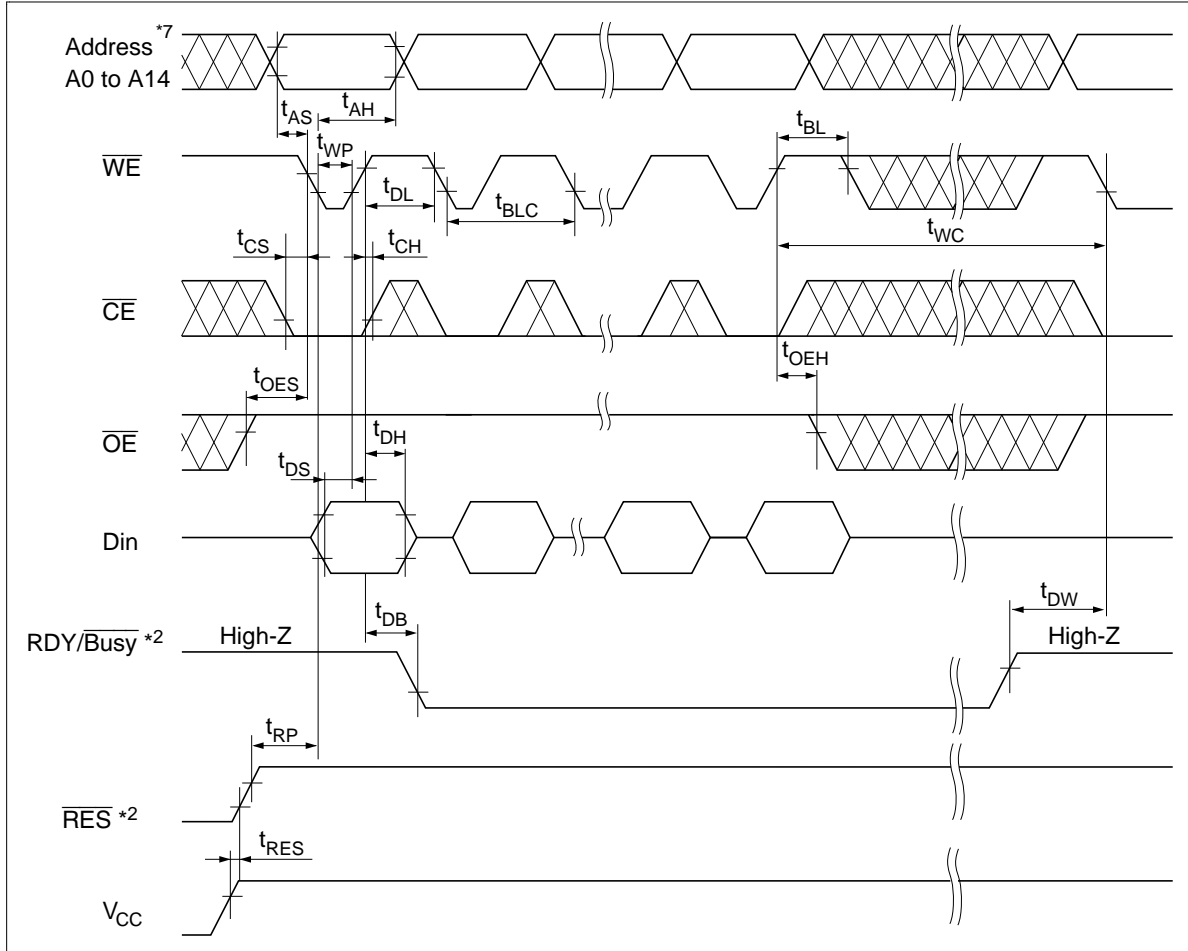
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Byte Write Timing Waveform (2) (\overline{CE} Controlled)



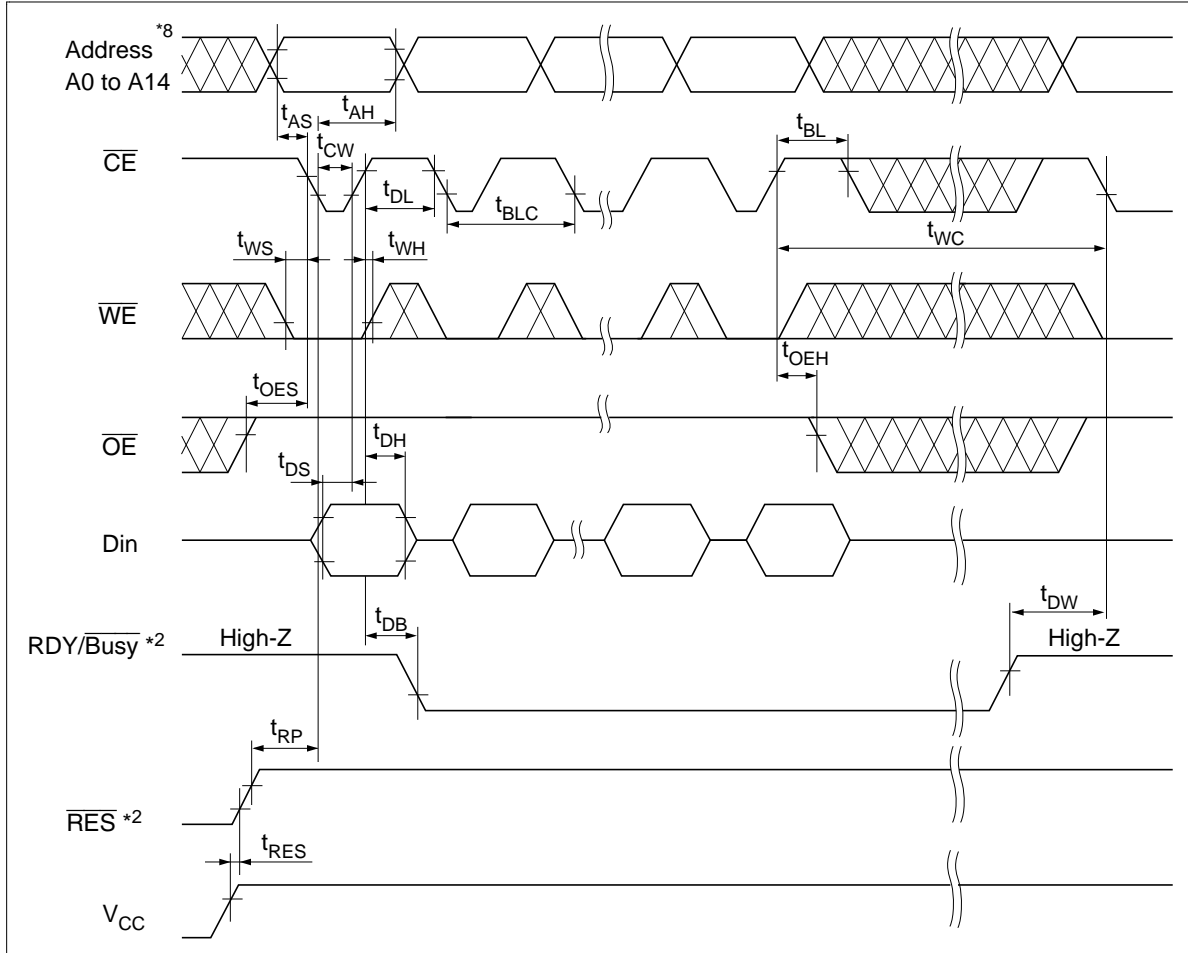
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Page Write Timing Waveform (1) ($\overline{\text{WE}}$ Controlled)



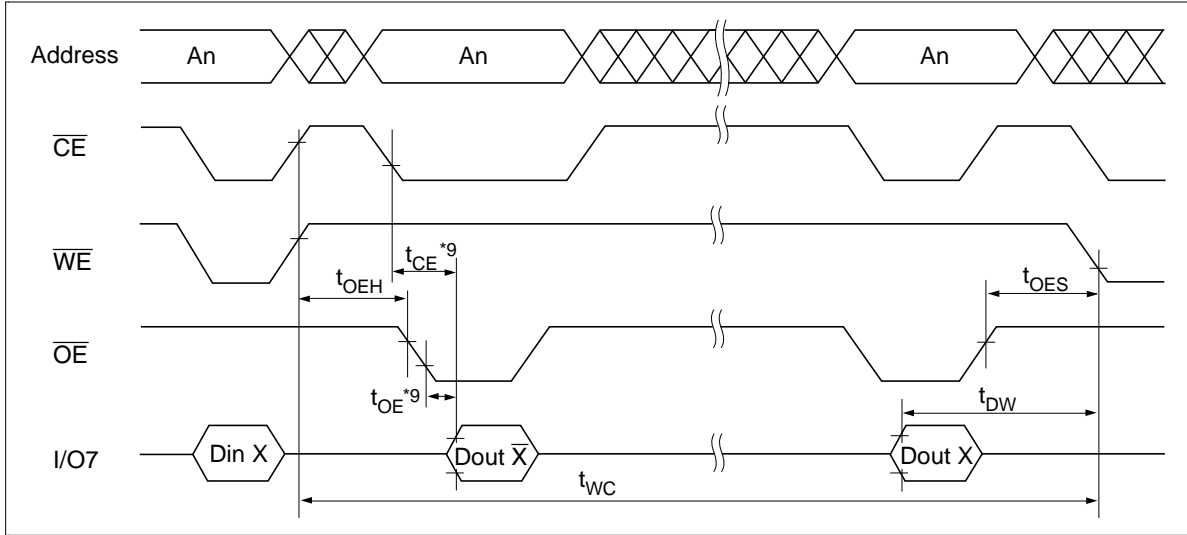
HN58V256A Series HN58V257A Series

Page Write Timing Waveform (2) ($\overline{\text{CE}}$ Controlled)



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Data Polling Timing Waveform



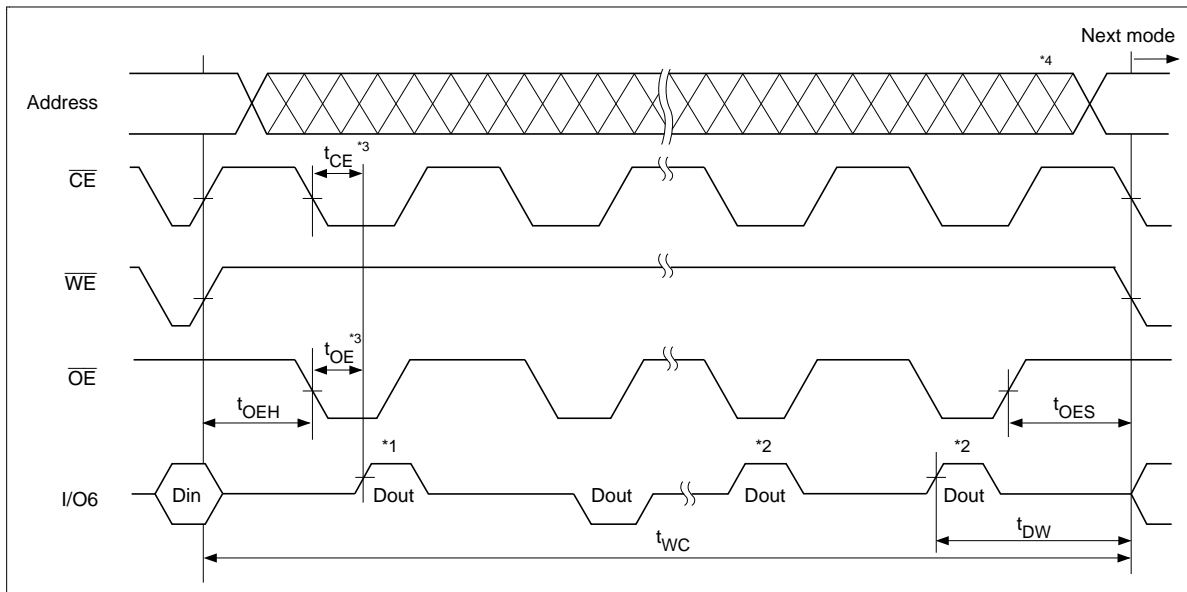
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Toggle bit

This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (togglng) for each read. When the internal programming cycle is finished, togglng of I/O6 will stop and the device can be accessible for next read or program.

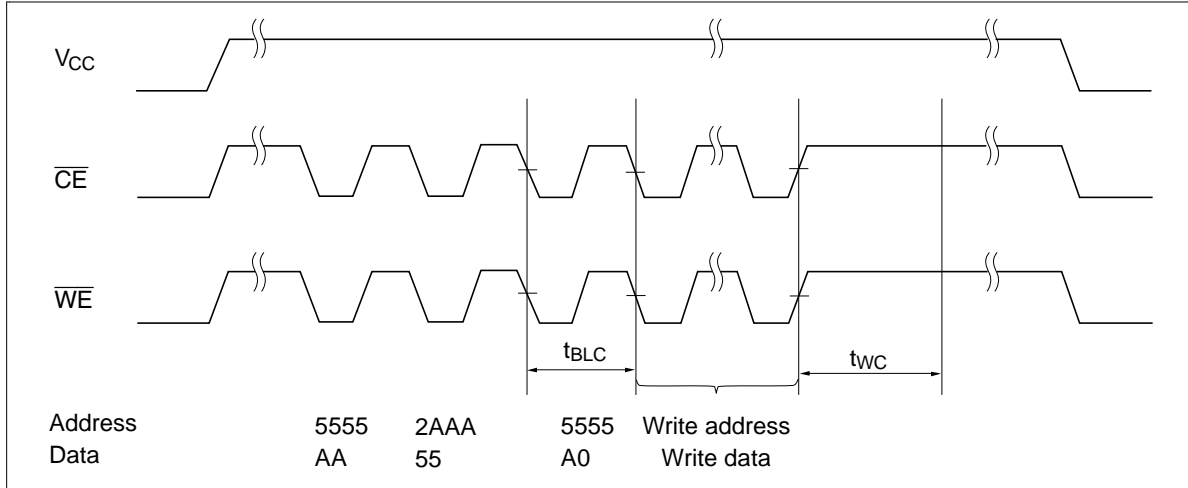
Toggle bit Waveform

- Notes: 1. I/O6 beginning state is “1”.
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.

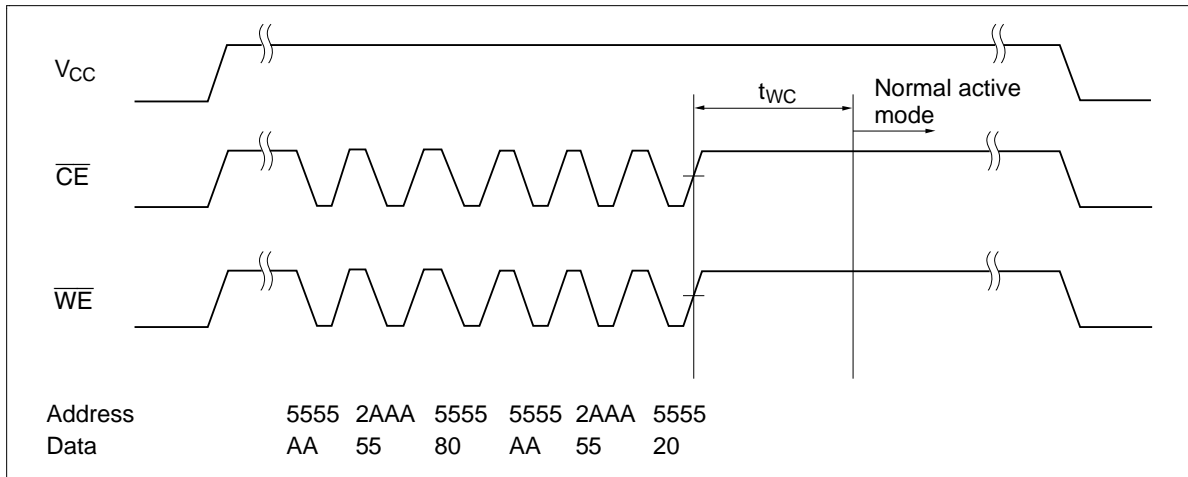


HN58V256A Series, HN58V257A Series

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



HN58V256A Series HN58V257A Series

Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μ s from the preceding falling edge of \overline{WE} or \overline{CE} . When \overline{CE} or \overline{WE} is high for 100 μ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

\overline{RDY} Polling

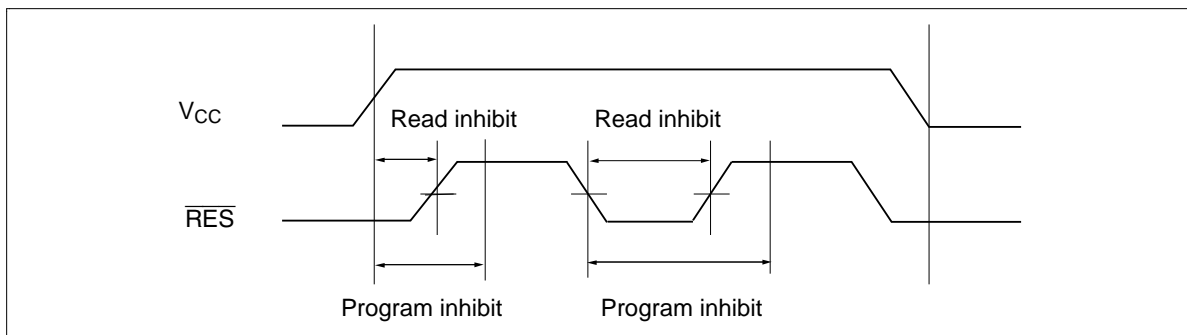
Data polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

$\overline{RDY/Busy}$ Signal (only the HN58V257A series)

$\overline{RDY/Busy}$ signal also allows the status of the EEPROM to be determined. The $\overline{RDY/Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the $\overline{RDY/Busy}$ signal changes state to high impedance.

\overline{RES} Signal (only the HN58V257A series)

When \overline{RES} is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping \overline{RES} low when V_{CC} is switched. \overline{RES} should be high during read and programming because it doesn't provide a latch function.



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\overline{WE} , \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

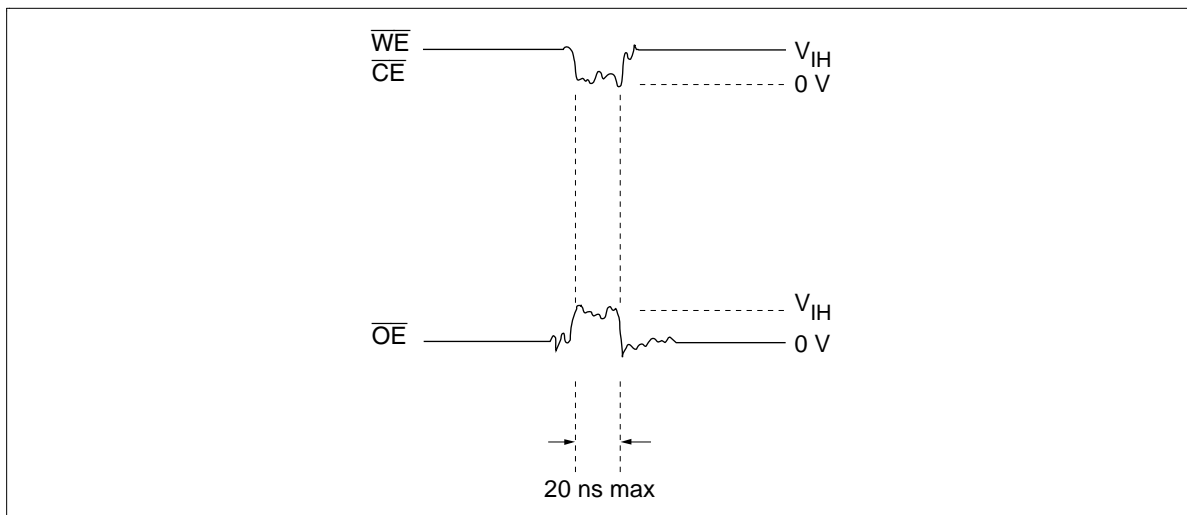
Data Protection

1. Data Protection against Noise on Control Pins (\overline{CE} , \overline{OE} , \overline{WE}) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less.

Be careful not to allow noise of a width of more than 20 ns on the control pins.

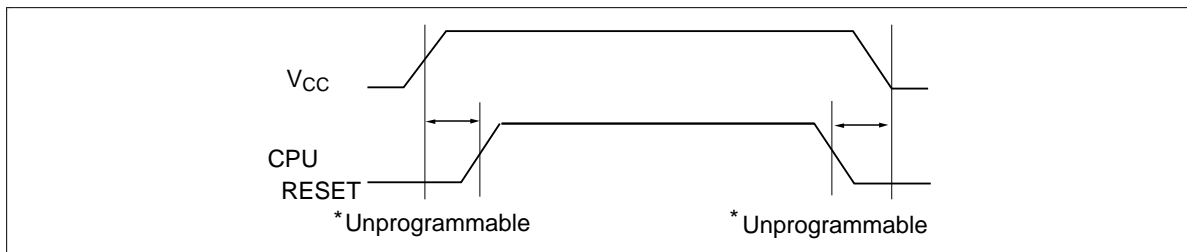


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2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



(1) Protection by \overline{CE} , \overline{OE} , \overline{WE}

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

\overline{CE}	V_{CC}	x	x
\overline{OE}	x	V_{SS}	x
\overline{WE}	x	x	V_{CC}

x: Don't care.

V_{CC} : Pull-up to V_{CC} level.

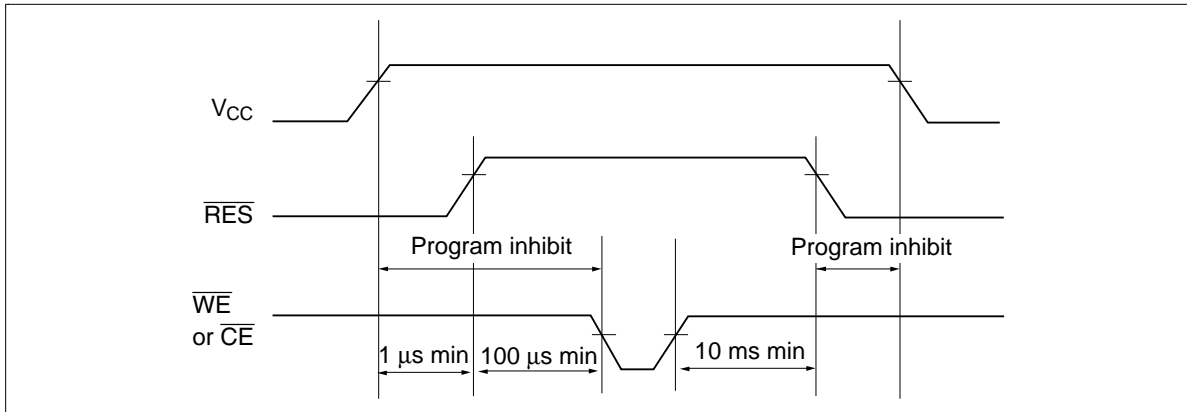
V_{SS} : Pull-down to V_{SS} level.

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(2) Protection by $\overline{\text{RES}}$ (only the HN58V257A series)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{\text{RES}}$ pin. $\overline{\text{RES}}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM breaks off programming operation when $\overline{\text{RES}}$ becomes low, programming operation doesn't finish correctly in case that $\overline{\text{RES}}$ falls low during programming operation. $\overline{\text{RES}}$ should be kept high for 10 ms after the last data input.



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3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.

Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	A0
↓	↓
Write address	Write data } Normal data input

The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.

Address	Data
5555	AA
↓	↓
2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
2AAA	55
↓	↓
5555	20

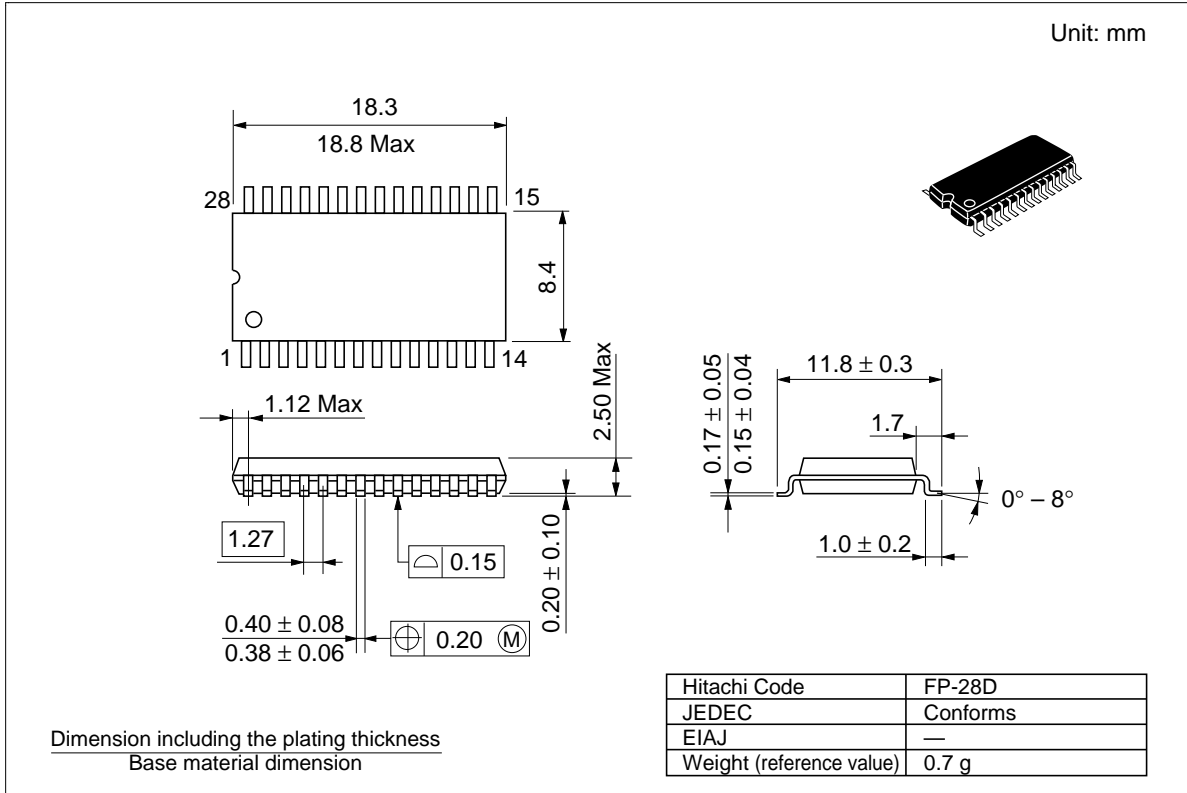
The software data protection is not enabled at the shipment.

Note: There are some differences between Hitachi's and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Hitachi sales offices.

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Package Dimensions

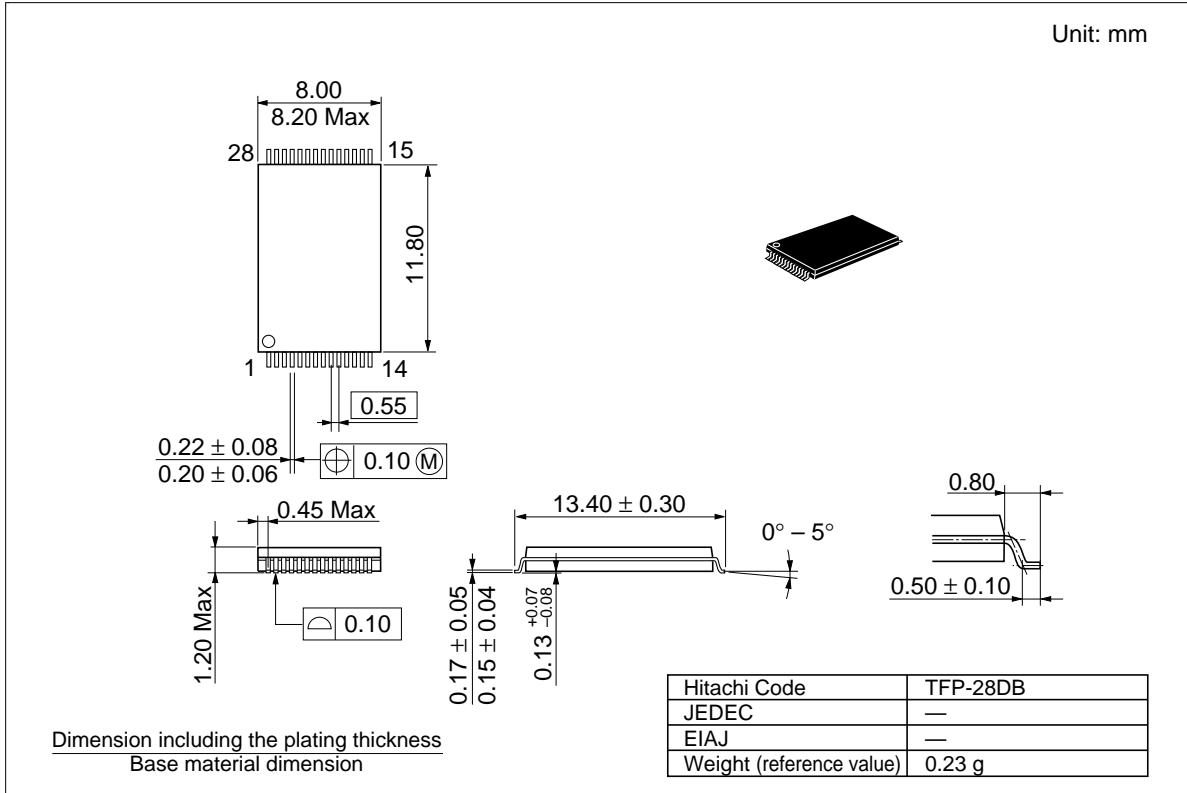
HN58V256AFP Series (FP-28D)



HN58V256A Series HN58V257A Series

Package Dimensions (cont.)

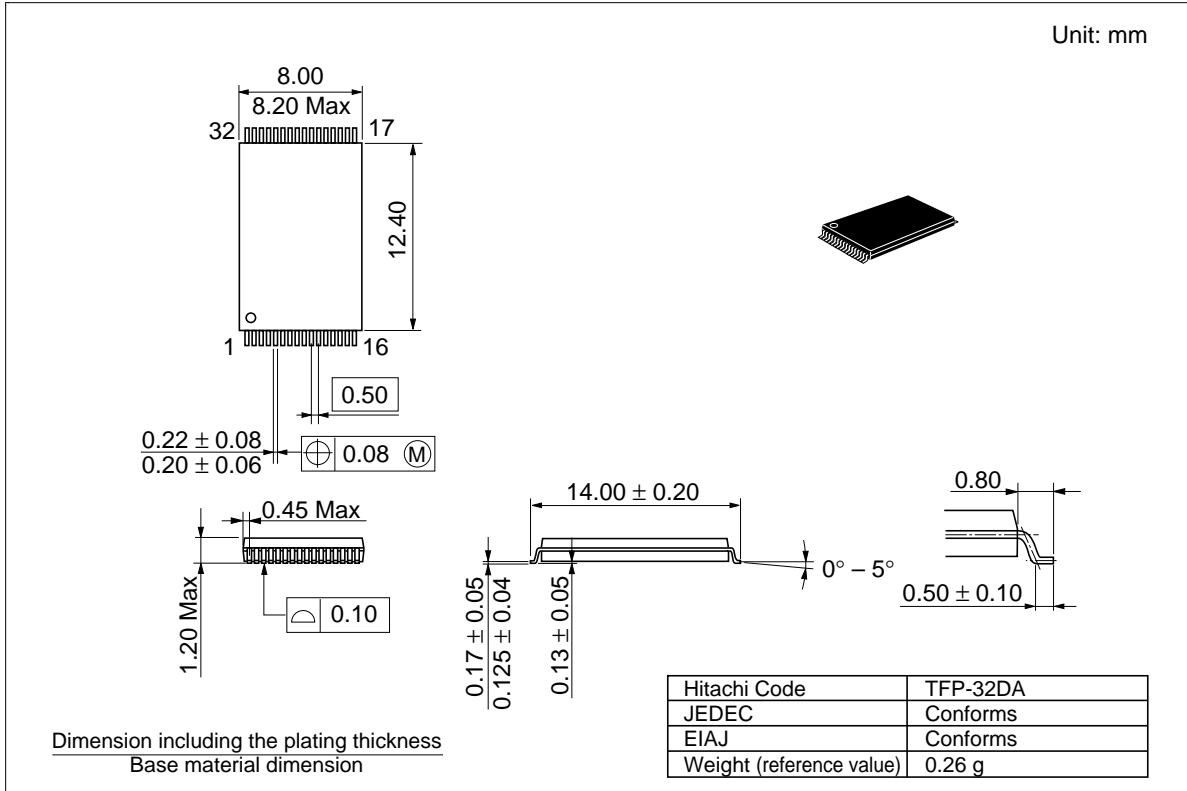
HN58V256AT Series (TFP-28DB)



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Package Dimensions (cont.)

HN58V257AT Series (TFP-32DA)



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Mar. 15, 1995	Initial issue	M. Terasawa	T. Muto
0.1	Aug. 7, 1995	Determination of package type: HN58V256AT series (TFP-28DB) Deletion of HN58V256AP series (DP-28) Deletion of HN58V256AFPI-12/15 Deletion of HN58V256AT-12SR/15SR Deletion of HN58V257AT-12SR/15SR Absolute Maximum Rating Deletion of Device Group Deletion of Operating temperature range – 20 to + 85°C and – 40 to +85°C Recommended DC Operating Conditions Deletion of Device Group Deletion of Operating temperature range –20/—/85°C and –40/—/85°C Deletion of note 4 Change order of notes	M. Terasawa	T. Muto
1.0	Apr. 12, 1995	Change of format Operating Information Deletion of HN58V256A-15 and HN58V257A-15 Deletion of note 1 Deletion of Compatible type No. Deletion of Operating temperature range Pin Description Addition of note 1 Block Diagram Addition of note 1 Mode Selection Addition of note 3 Absolute Maximum Ratings Addition of note 4 Recommended DC operating Condition V _{IH} (min) 2.4 V to 1.9 V Addition of note 4 DC Characteristics I _{CC3} (max): 8/12/20/30 mA to 8/12/15/30 mA AC Characteristics Test condition: Input pulse levels: 0 V to 3.0 V to 0.4 V to 2.4 V (V _{CC} ≤ 3.6 V), 0.4 V to 3.0 V (V _{CC} > 3.6V) Addition of note 2 Read Timing Waveform: Addition of note 1 Write Cycle: t _{DS} (min): 50 ns to 70 ns Addition of note 4, 5 Byte Write Timing Waveform (1) and (2): Addition of note 1 Page Write Timing Waveform (1) and (2): Addition of note 2	M. Terasawa	T. Wada

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Revision Record (cont.)

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Apr. 12, 1995	AC Characteristics Data Polling Timing Waveform: Addition of note 1 Toggle bit Waveform: Addition of note 4 Functional Description Data Protection 2-(2) Addition of figure	M. Terasawa	T. Wada
2.0	Mar. 4, 1997	Functional Description Data protection 3: Addition of note	Y. Nagai	K. Furusawa
3.0	May. 20, 1997	Functional Description Data protection 3: Change of Description	M. Terasawa	K. Furusawa
4.0	Oct. 24, 1997	Timing Waveforms Read Timing Waveform: Correct error		
