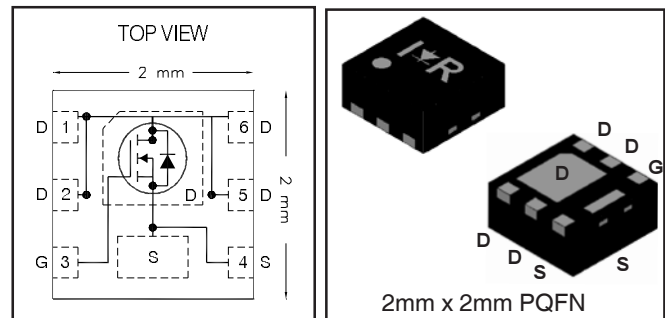


IRLHS6242PbF

HEXFET® Power MOSFET

V_{DS}	20	V
V_{GS}	±12	V
$R_{DS(on) \max}$ (@ $V_{GS} = 4.5V$)	11.7	mΩ
$R_{DS(on) \max}$ (@ $V_{GS} = 2.5V$)	15.5	mΩ
I_D (@ $T_{C(Bottom)} = 25^\circ C$)	12 Ⓣ	A



Applications

- Charge and discharge switch for battery application
- System/Load Switch

Features and Benefits

Features

Low $R_{DS(on)}$ ($\leq 11.7m\Omega$)
Low Thermal Resistance to PCB ($\leq 13^\circ C/W$)
Low Profile ($\leq 1.0mm$)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen

results in

⇒

Resulting Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLHS6242TRPBF	PQFN 2mm x 2mm	Tape and Reel	4000	
IRLHS6242TR2PBF	PQFN 2mm x 2mm	Tape and Reel	400	

Absolute Maximum Ratings

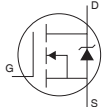
	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±12	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	10	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	8.3	
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ Ⓣ	22	
$I_D @ T_{C(Bottom)} = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ Ⓣ	18	
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ (Package Limited)	12	
I_{DM}	Pulsed Drain Current ①	88	
$P_D @ T_A = 25^\circ C$	Power Dissipation ②	1.98	W
$P_D @ T_{C(Bottom)} = 25^\circ C$	Power Dissipation ②	9.6	
	Linear Derating Factor ③	0.016	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Notes ① through ③ are on page 2

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	6.8	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	9.4	11.7	m Ω	$V_{GS} = 4.5V, I_D = 8.5A$ ③②
		—	12.4	15.5		$V_{GS} = 2.5V, I_D = 8.5A$ ③②
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.8	1.1	V	$V_{DS} = V_{GS}, I_D = 10\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-4.2	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$
g_{fs}	Forward Transconductance	36	—	—	S	$V_{DS} = 10V, I_D = 8.5A$ ②
Q_g	Total Gate Charge ⑥	—	14	—	nC	$V_{DS} = 10V$
Q_{gs}	Gate-to-Source Charge ⑥	—	1.5	—		$V_{GS} = 4.5V$
Q_{gd}	Gate-to-Drain Charge ⑥	—	6.3	—		$I_D = 8.5A$ ② (See Fig.17 & 18)
R_G	Gate Resistance	—	2.1	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	5.8	—	ns	$V_{DD} = 10V, V_{GS} = 4.5V$ ③ $I_D = 8.5A$ ② $R_G = 1.8\Omega$ See Fig.15
t_r	Rise Time	—	15	—		
$t_{d(off)}$	Turn-Off Delay Time	—	19	—		
t_f	Fall Time	—	13	—		
C_{iss}	Input Capacitance	—	1110	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = 10V$
C_{rss}	Reverse Transfer Capacitance	—	180	—		$f = 1.0MHz$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	22	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	88		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 8.5A$ ②, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	15	23	ns	$T_J = 25^\circ\text{C}, I_F = 8.5A$ ②, $V_{DD} = 10V$
Q_{rr}	Reverse Recovery Charge	—	12	18	nC	$di/dt = 210A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑤	—	13	$^\circ\text{C}/W$
$R_{\theta JC}$ (Top)	Junction-to-Case ⑤	—	94	
$R_{\theta JA}$	Junction-to-Ambient ④	—	63	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ④	—	46	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Package is limited to 12A by die-source to lead-frame bonding technology.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ R_{θ} is measured at T_J of approximately 90°C .
- ⑥ For DESIGN AID ONLY, not subject to production testing.
- ⑦ Calculated continuous current based on maximum allowable junction temperature.

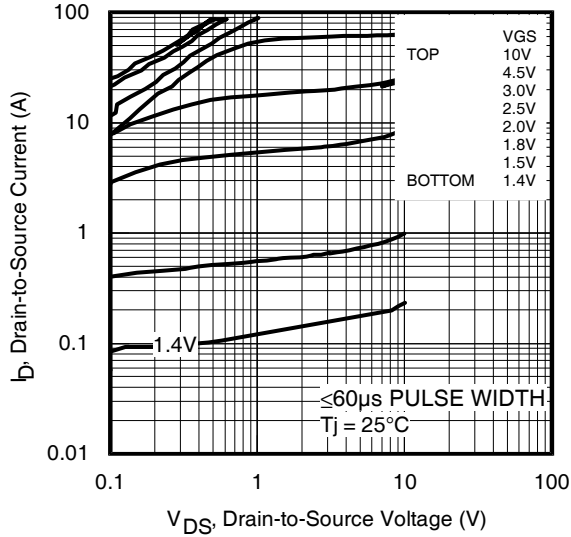


Fig 1. Typical Output Characteristics

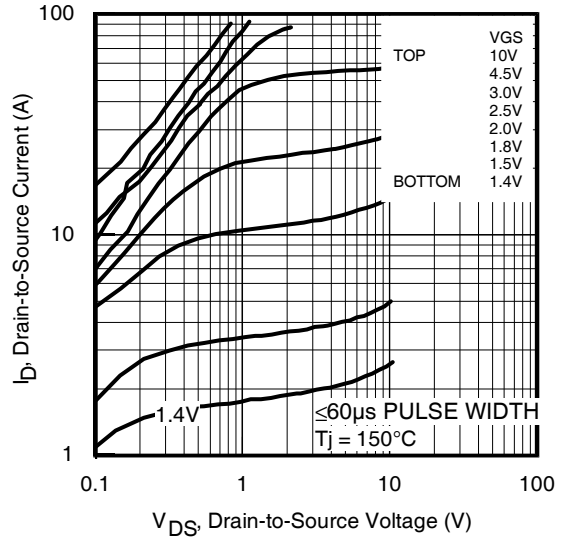


Fig 2. Typical Output Characteristics

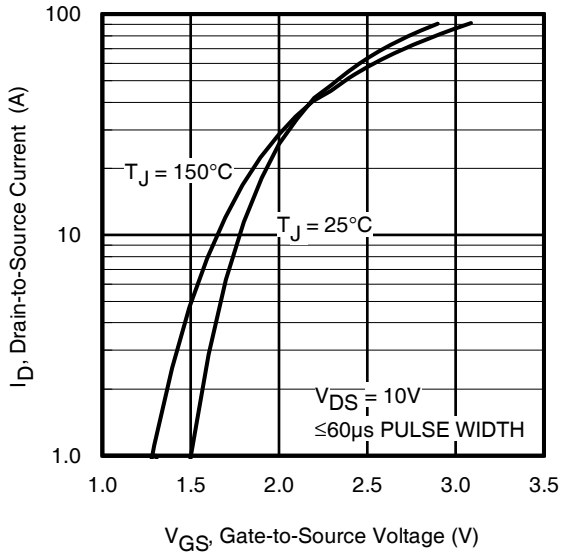


Fig 3. Typical Transfer Characteristics

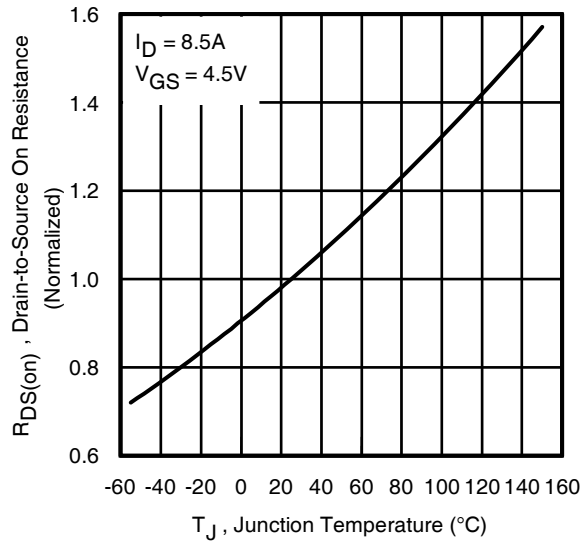


Fig 4. Normalized On-Resistance vs. Temperature

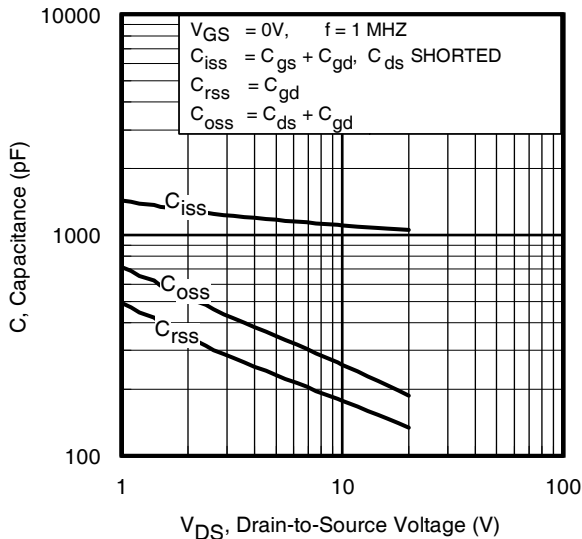


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
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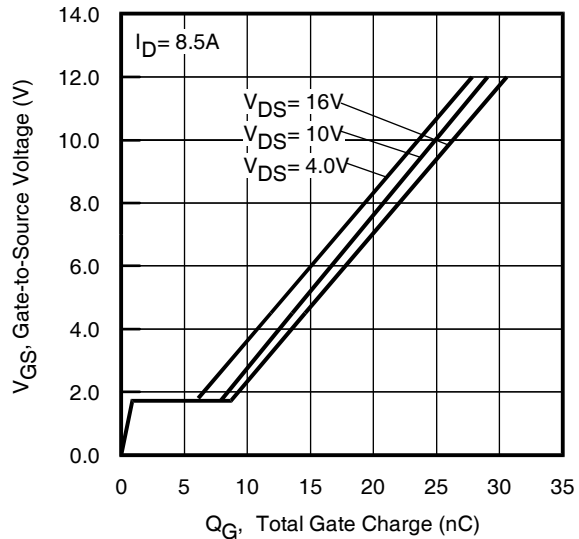


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

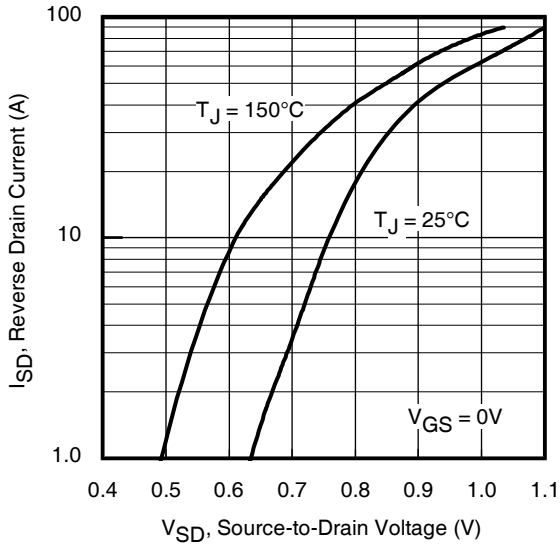


Fig 7. Typical Source-Drain Diode Forward Voltage

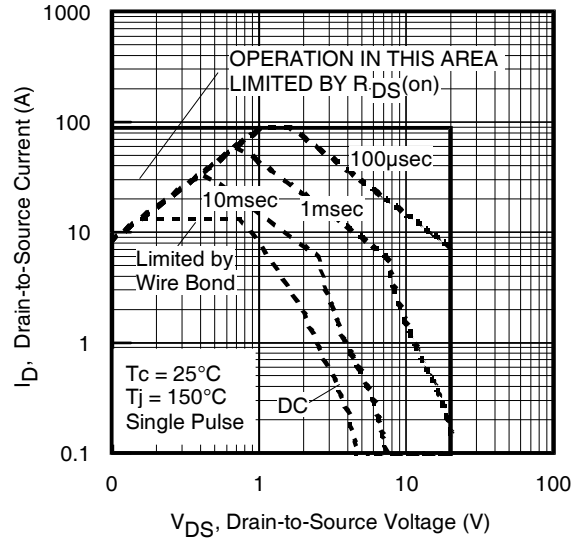


Fig 8. Maximum Safe Operating Area

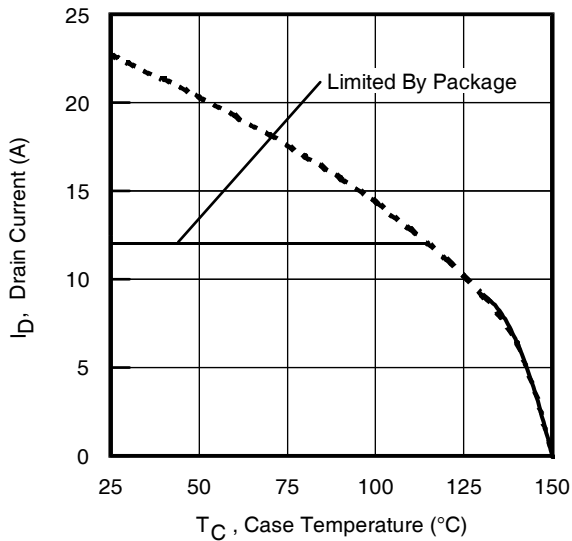


Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

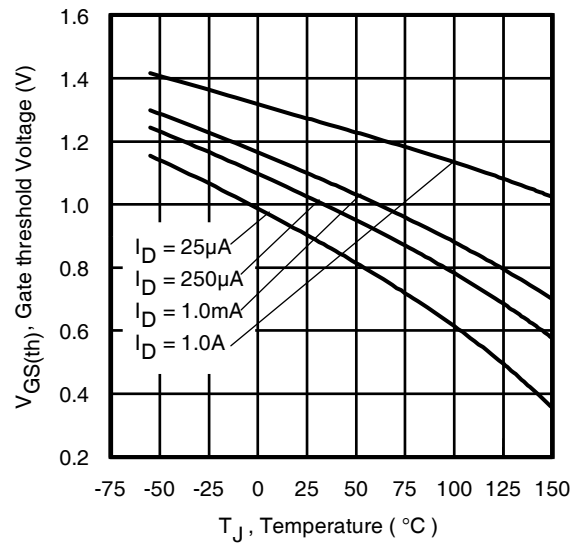


Fig 10. Threshold Voltage vs. Temperature

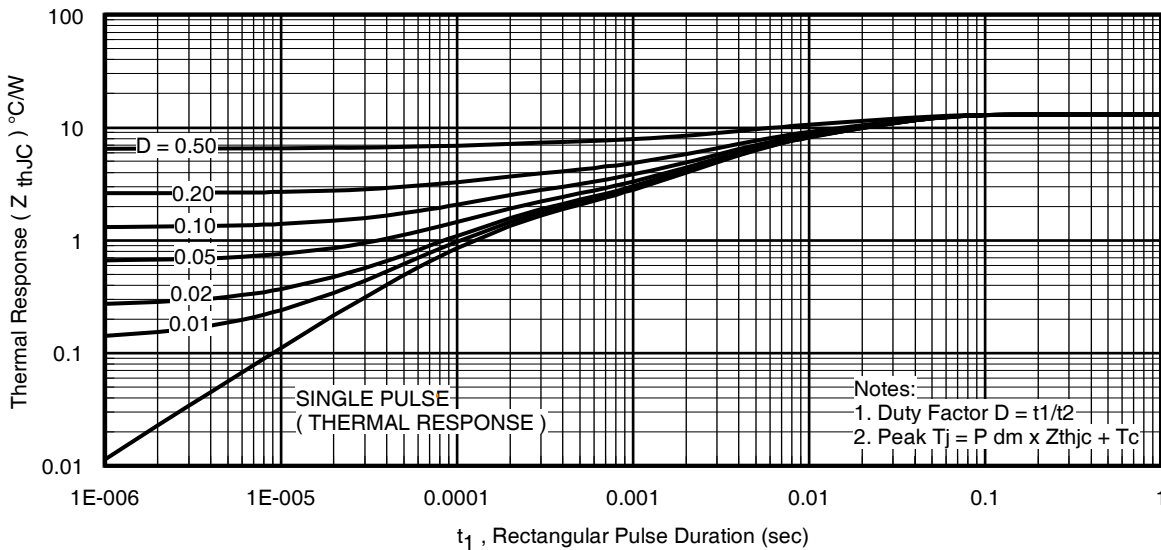


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

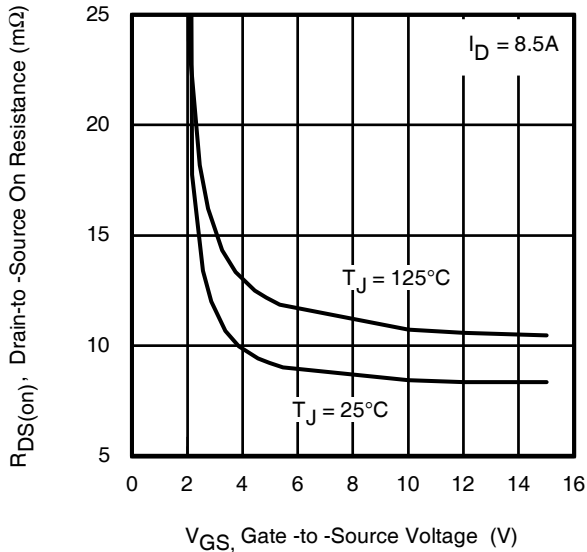


Fig 12. On-Resistance vs. Gate Voltage

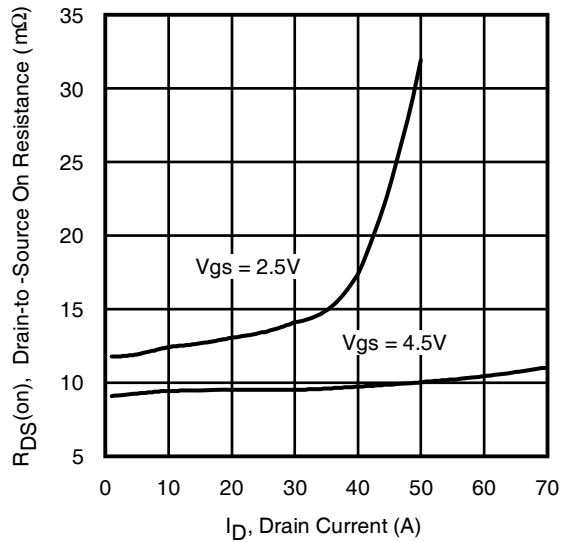


Fig 13. Typical On-Resistance vs. Drain Current

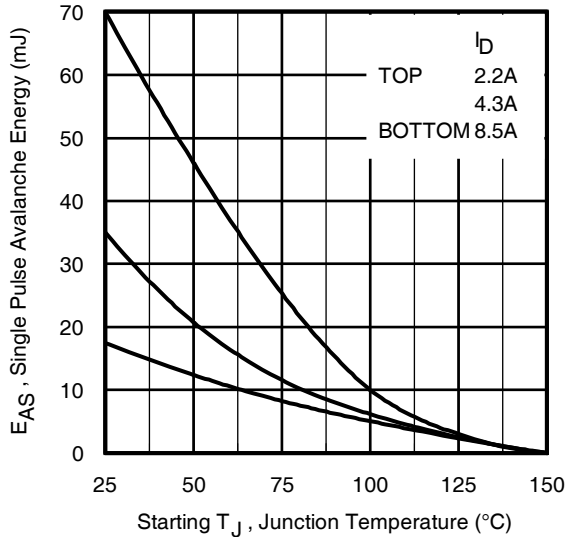


Fig 14. Maximum Avalanche Energy vs. Drain Current

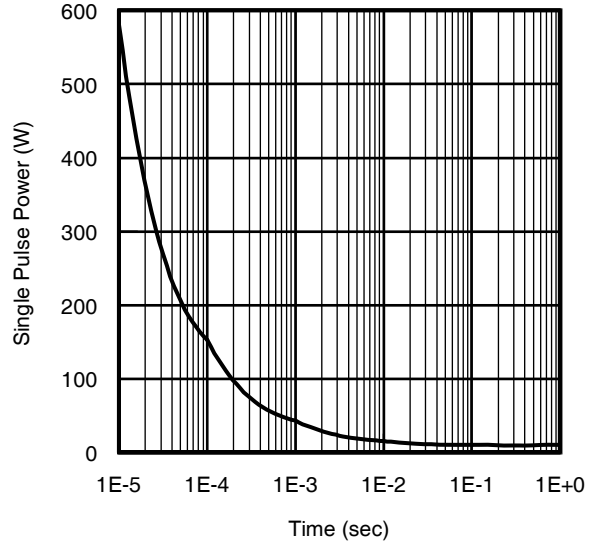


Fig 15. Typical Power vs. Time

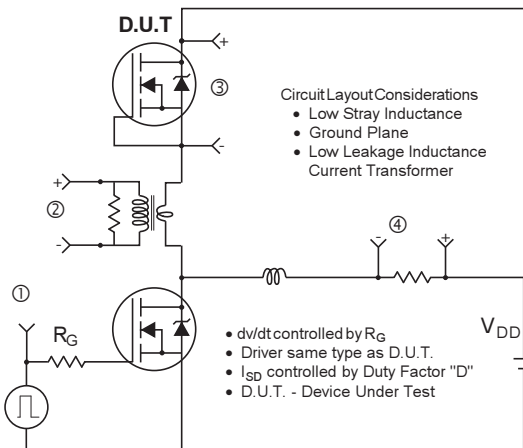
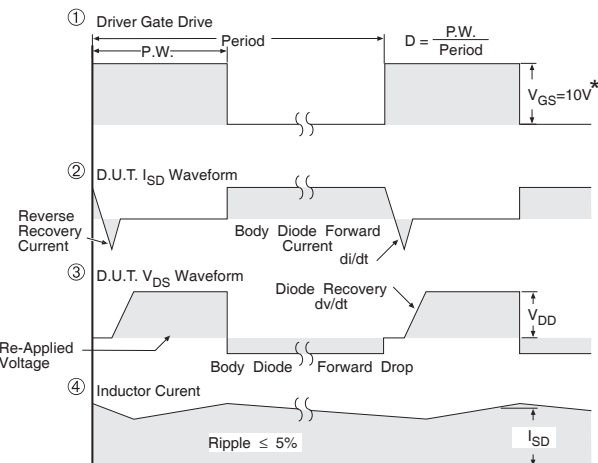


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET[®] Power MOSFETs



* $V_{GS} = 5V$ for Logic Level Devices

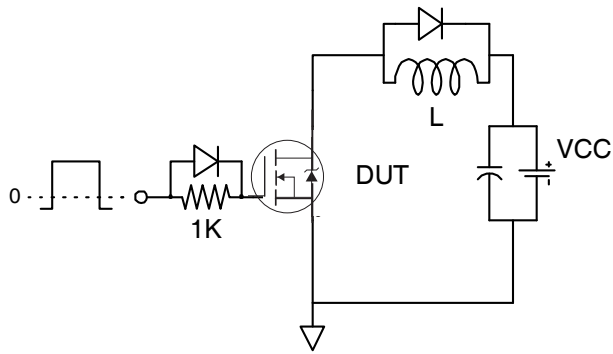


Fig 17a. Gate Charge Test Circuit

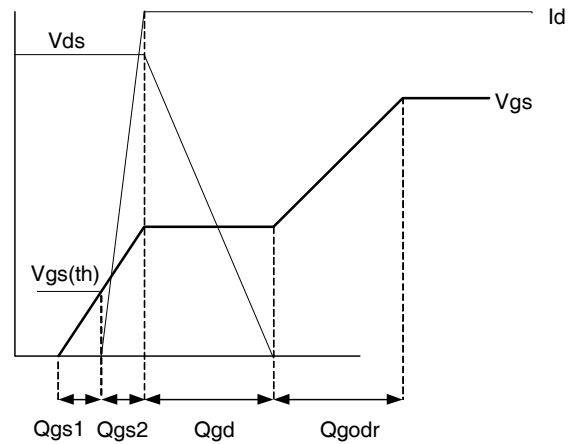


Fig 17b. Gate Charge Waveform

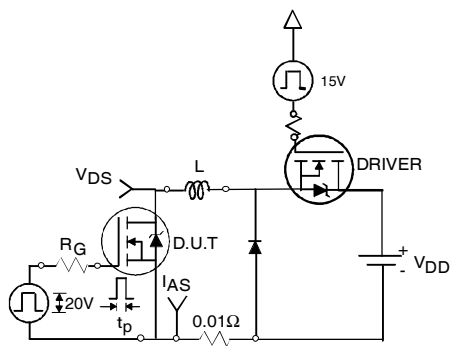


Fig 18a. Unclamped Inductive Test Circuit

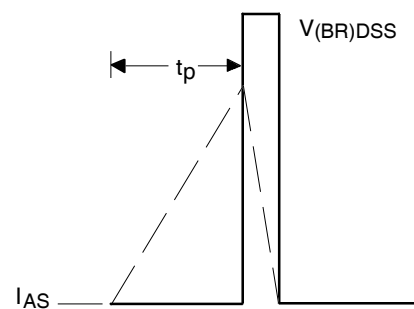


Fig 18b. Unclamped Inductive Waveforms

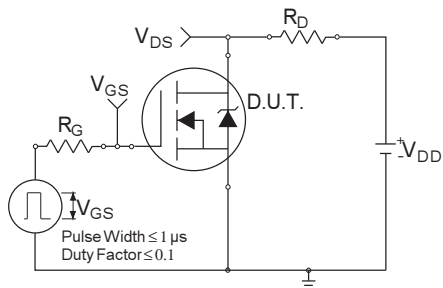


Fig 19a. Switching Time Test Circuit

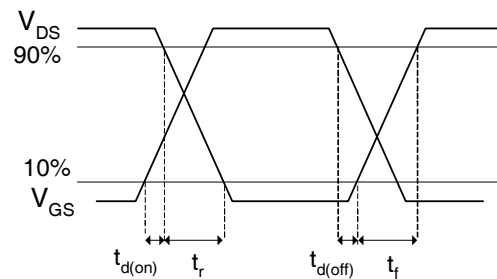
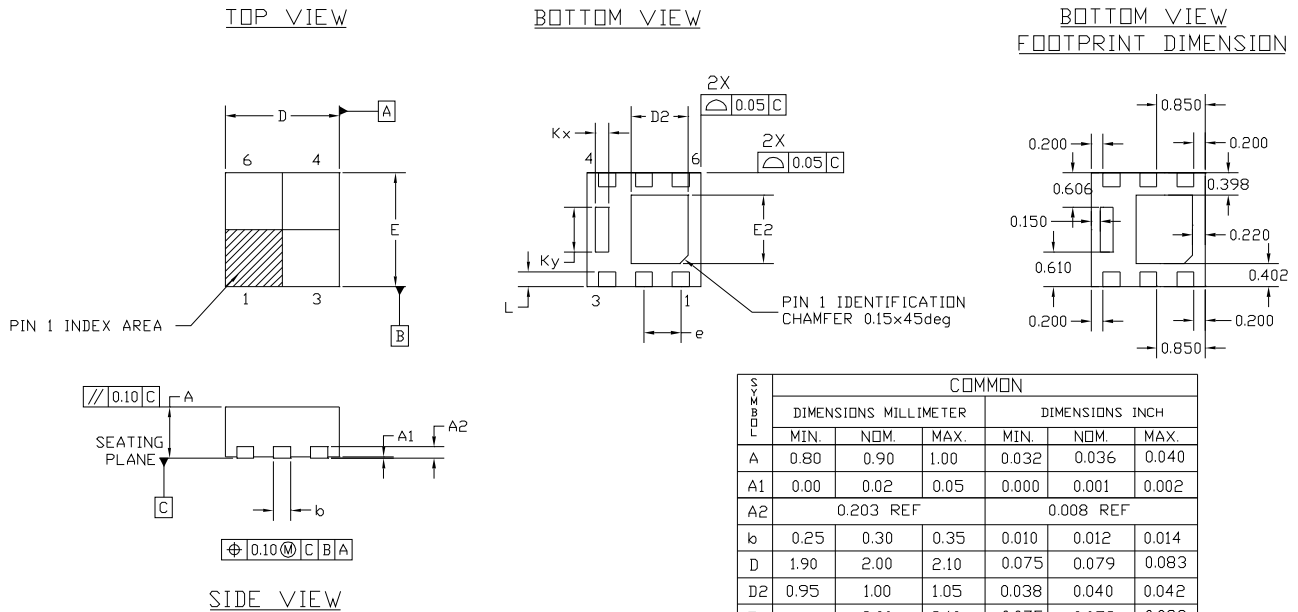


Fig 19b. Switching Time Waveforms

PQFN 2x2 Outline Package Details

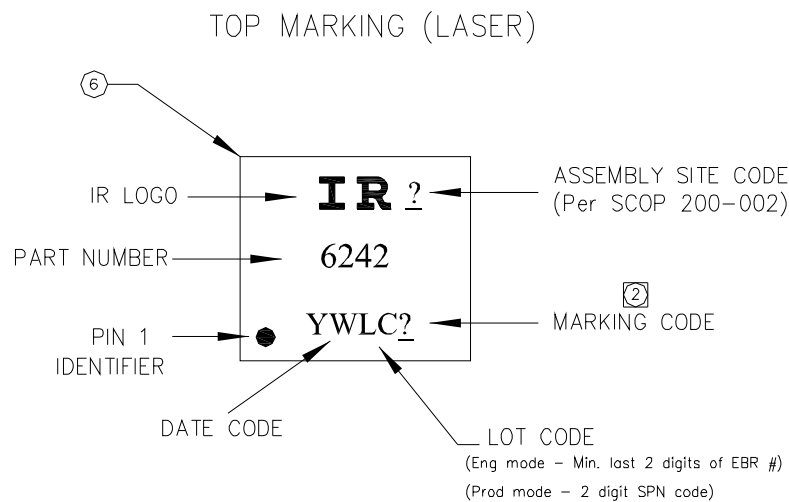


NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm. FROM TERMINAL TIP.

For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 2x2 Outline Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 2x2 Outline Tape and Reel

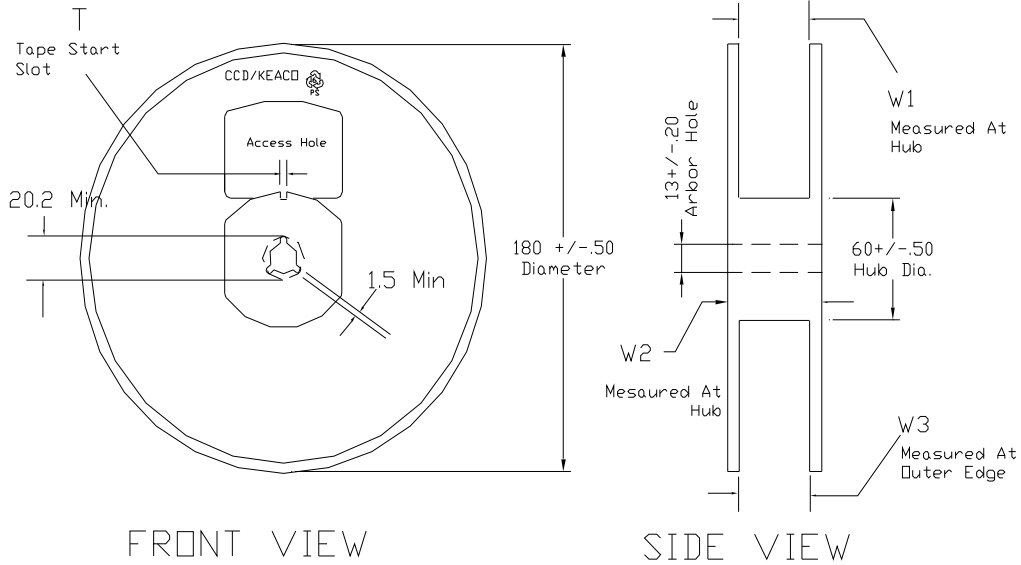
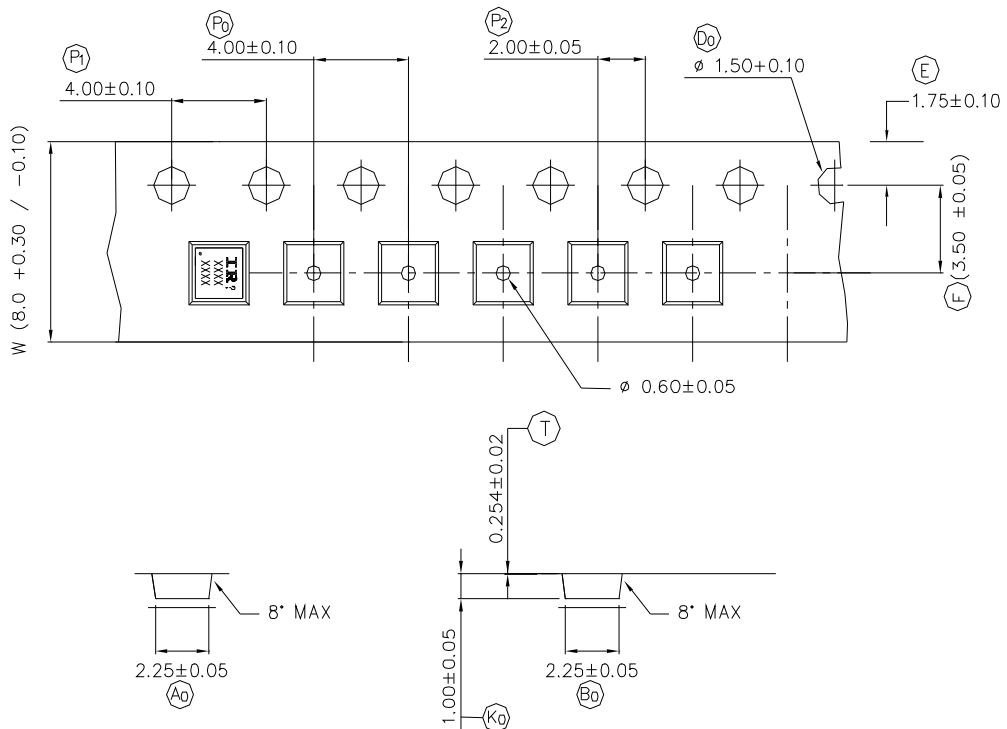


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 ^{+1.5} _{-0.0}	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 ^{+2.0} _{-0.0}	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is $\geq 1 \times 10^5$ but $< 1 \times 10^{12}$ ohm/sq.



NOTE: The Surface Resistivity is $10^4 - 10^8$ OHM/SQ

Qualification information[†]

Qualification level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 2mm x 2mm	MSL 1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.
 Please contact your International Rectifier sales representative for further information:
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

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