TMPZ80C47P

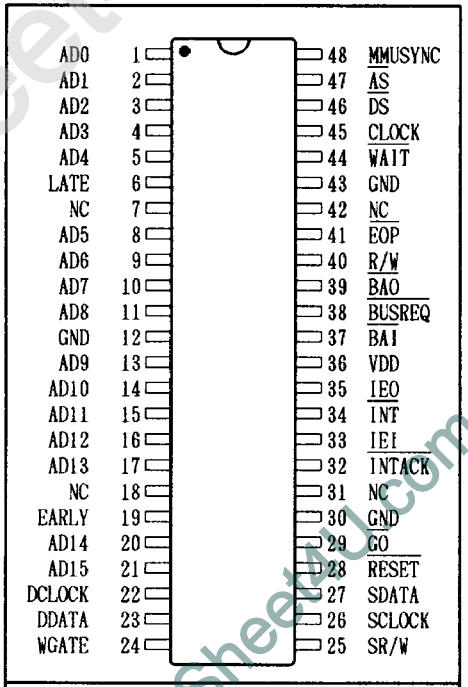
(Hard Disk Controller)

1. GENERAL DESCRIPTION

The TMPZ80C47P is a high efficiency hard disk controller (HDC) with the built-in DMA function.
Commands are issued in such a manner that when a command list called CCW (Channel control Word) is provided on a memory and a GO signal is given to HDC, CCW is automatically taken in and executed by HDC. In addition, since CCW can be chained automatically, multiple commands can be issued by only one time GO signal and complicated operations are easily realized.
The ST506 type interface has been adopted as the DISK interface, realizing max.10Mbit/sec transfer rate by MFM signal.
A 16 bit bus compatible with Z8000 has been adopted at HOST side.

FEATURES

- o Si-gate CMOS Technology
- o 5V single power supply
- o Built-in DMA function
- o Z bus compatible
- o CCW system
- o ST506 interface
- o Built-in ECC auto correction function (11bit burst error correction)
- o Max. 4 disk drives Connective
- o Max. 16 heads/drive
- o Built-in buffer RAM (256 bytes)
- o 48-pin DIP package



TMPZ80C47P PIN ARRANGEMENT

2. PIN DESCRIPTION

Pin No.	Name	Input/Output	Contents
1-5, 8-11, 13-17, 20, 21	AD0-AD15	I/O	Multiplex address data bus
48	MMUSYNC	OUTPUT	Sync. signal to MMU (Memory Management Unit, Z8010, Z8015)
47	AS/	3-STATE	Address strobe
46	DS/	I/O	Data strobe
45	CLOCK	INPUT	Clock at Host Block
44	WAIT/	INPUT	WAIT Input
41	EOP/	INPUT	Warning signal for irregular DMA (normally, connected to MMU SUP/)
40	R/W	I/O	Read/Write switching signal
39	BAO/	Output	Bus Control daisy chain output
38	BUSREQ/	OPEN DRAIN	Bus Control request signal
37	BAI/	INPUT	Bus Control daisy chain input
35	IEO	OUTPUT	Interrupt daisy chain output
34	INT/	OPEN DRAIN	Interrupt request signal
33	IEI	INPUT	Interrupt daisy chain input
32	INTACK/	INPUT	Interrupt acknowledge signal
29	GO/	INPUT	HDC start signal
28	RESET/	INPUT	RESET signal
27	SDATA	I/O	SERIAL DATA Input/Output
26	SCLOCK	OUTPUT	SERIAL DATA CLOCK
25	SR/W	OUTPUT	SERIAL DATA Read/Write
24	WGATE	OUTPUT	WRITE GATE Signal
23	DDATA	I/O	I/O terminal of Disk MFM data

Pin No.	Name	Input/Output	Contents
22	DCLOCK	INPUT	Disk block main clock. When reading, input 2 times clock pulse of transfer rate from VFO. When writing, input the crystal oscillator.
19	EARLY	OUTPUT	Signal for precompensation of Disk data
6	LATE	OUTPUT	Signal for precompensation of Disk data
36	VDD		Supply Voltage (+5V)
12,30,43	GND		Ground
7, 18, '31 42	NC		NO CONNECTION

3. INTERNAL STRUCTURE AND INTERFACE

3-1 Internal Blocks

The TMPZ80C47P consists of 5 functional blocks (CPU block, host block, buffer block, disk block and serial block). These blocks are connected each other by 16-bit internal bus.

(1) CPU Block

A CPU equipped with a 16-bit ALU. Command code is 8 bit wide. This CPU has a built-in 2K byte firmware ROM and controls the entire HDC operation.

CPU reads and analyzes CCW, outputs control signals to all blocks, inputs status signals, carries out execution of CCW, error detection, etc.

(2) Host block

The host block is a block that performs input/output of data to/from a host memory through the external bus of HDC. The host block consists of the bus control circuit, interrupt control circuit, DMA controller, etc. The external bus is compatible with Zilog's Z-bus.

(3) Buffer block

This block consists of a 16-bit x 128-word sector buffer RAM and its control circuit.

When used for data input/output between a disk and the host memory, this buffer block operates as FIFO and therefore, it is possible that both the disk block and the host block operate at the same time.

As it can be accessed from the CPU block, this block is also used for CCW read and STATUS write.

(4) Disk block

This block performs data transfer and formatting of disks. This block consists of the sequencer for disk track formatting, 16-bit serial-parallel converter, MFM encoder/decoder, CRC-ECC circuit, etc.

The disk interface adopted is of ST506 type.

(5) Serial block

This is a block that inputs or outputs low speed interface signal as serial data.

This block controls the external shift registers through three control lines and inputs/outputs 8 input signals and 32 output signals, thereby realizing all disk signals and 32 bit DMA address capability through the 48-pin DIP.

BLOCK DIAGRAM

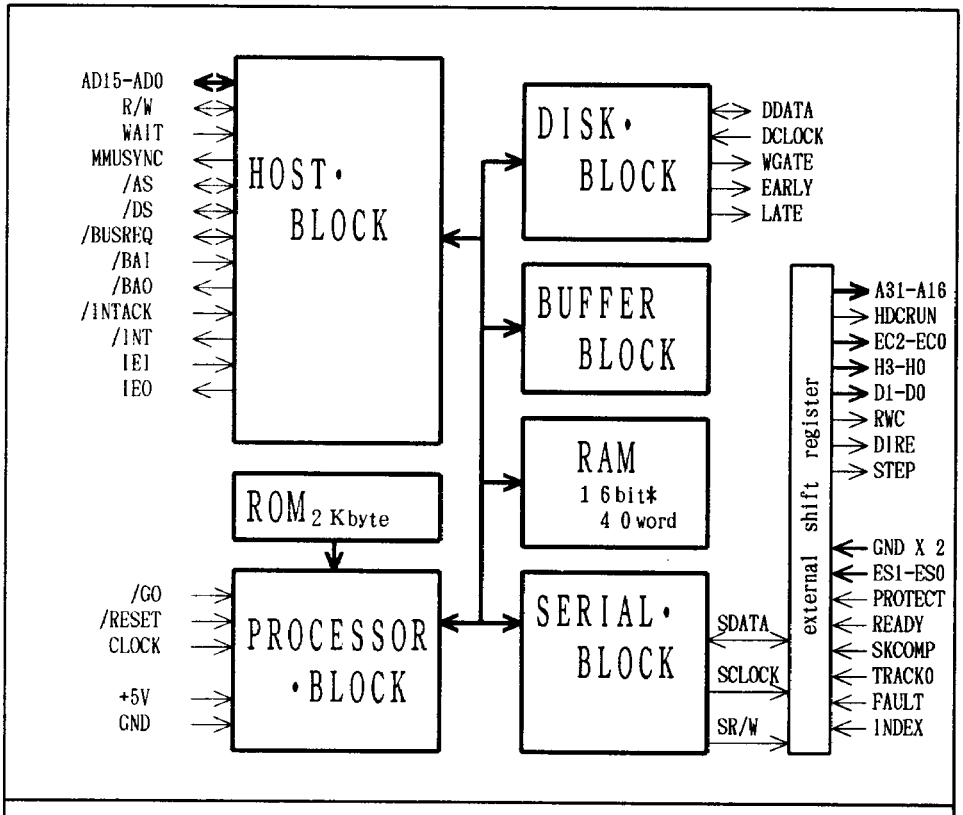


FIG1. HDC LSI BLOCK DIAGRAM

3-2 Host Interface

The Host interface supports the daisy-chain type bus control and interrupt for the Zilog's Z-bus compatible 16-bit bus.
Data transfer is carried out by the built-in DMA controller. DMA Address is 32 bits (4G byte).
DMA transfer is carried out for every 8 words (16 bytes) through the burst transfer and the bus control is returned to CPU side for every 8 words transfer. It is possible to connect the HOST interface to MMU (Z8010, Z8015) using MMUSYNC, a sync signal with MMU. One time (1 word) DMA transfer requires 3 clocks and when MMU is used, requires 4 clocks.
After completion of execution, HDC is enabled to generate an interrupt and supports both vector and non-vector.

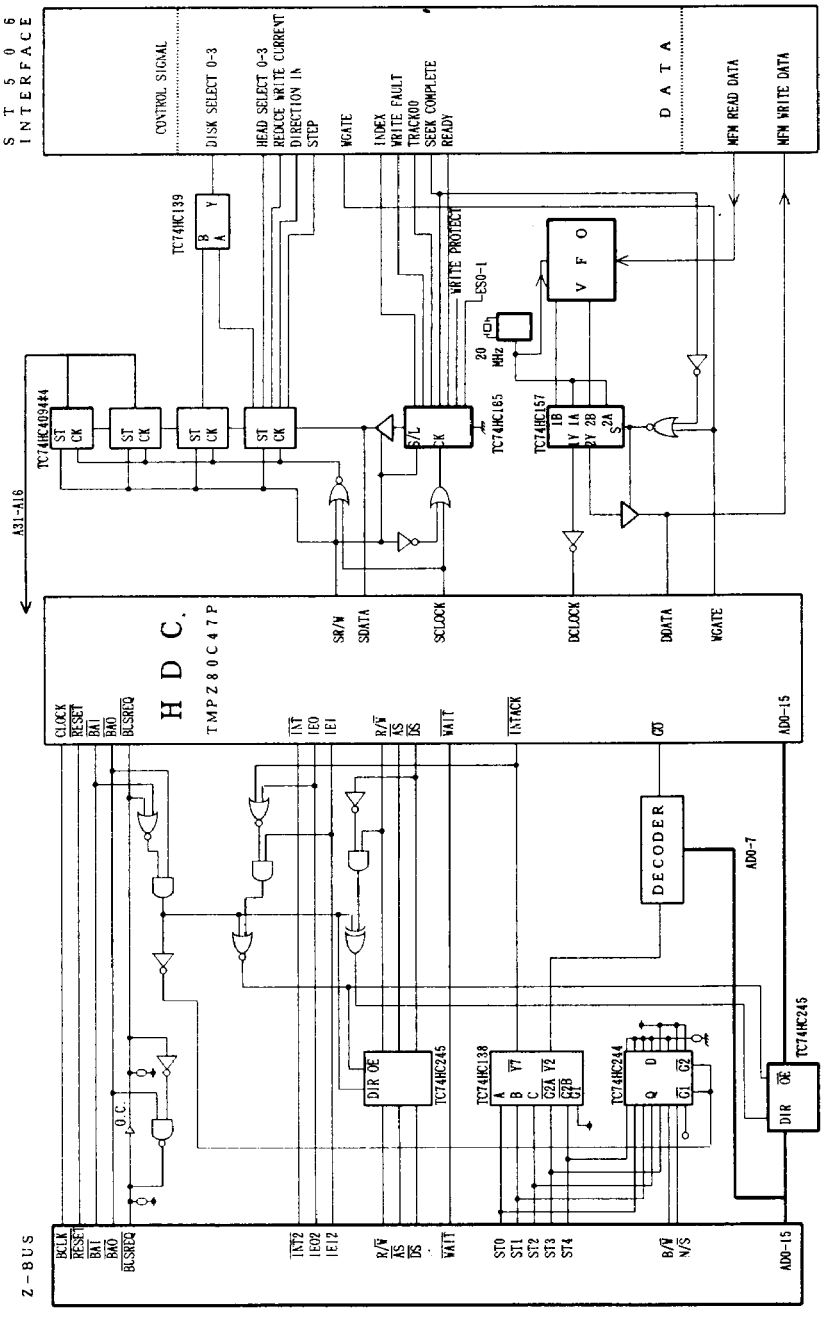
3-3 DISK Interface

The DISK side interface of the TMPZ80C47P has adopted ST506 type interface that is a standard interface of Winchester type drive.
TMPZ80C47P can control up to 4 drives and supports 16 heads and 1023 cylinders for each drive. Physical sector size is fixed at 256 bytes, but since the disk read/write are carried out on logical address (32 bits), data transfer can be carried out almost in the same manner as in the transfer between memories.
On one CCW, transfer of data in any size (for every 1 word) at max. 64K bytes and min. 2 bytes is possible.
When formatting the disk drive, alternate sector processing is automatically carried out in HDC and therefore, a disk can be handled externally as a faultless disk. (For details refer to 4-6 Alternate Sector Processing.)
Since HDC has the built-in MFM decoder/encoder, sink detection circuit and missing clock circuit, externally it requires a VFO circuit and data switching circuit only.

3-4 SERIAL Interface

The SERIAL interface performs serial data input/output through three signal lines (SR/W, SCLOCK and SDATA).
The input signals are 8 disk interface signals and user status signal (ES1, ES0).
Output signals are total 32 disk interface signals and high order 16 bits of DMA address.
Circuit examples are shown in 3-5. When high order 16 bits of DMA address are not used and number of disk drives is restricted to 2 units, no high order shift register is required.

3-5 Example of Circuit



3-6 Track Format

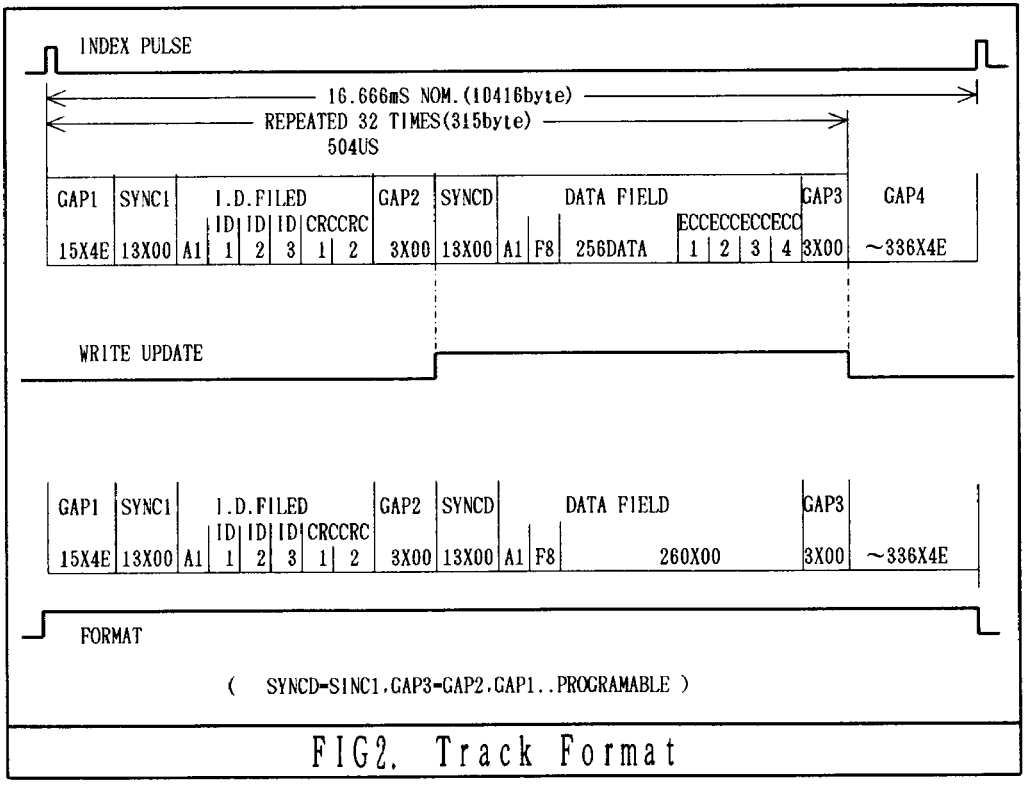


FIG2. Track Format

4. FUNCTIONS

4-1 Functional Description

Table of HDC Commands

FORMAT	Disk drive format command
READ	Command to transfer data from disk to memory. The seek operation is included.
WRITE	Command to transfer data from memory to disk. Similar to READ, the seek operation is included.
VERIFY	Command to compare disk data with memory data.
RTZ	Command to move the head to Track 0.
SET	Command to change CCW's root address
REPORT	Command to get error information from HDC
BOOT	Special command for Boot

[Features]

- o One FORMAT command can cover the formatting of the entire disk drive.
- o READ/WRITE/VERIFY commands used the physical sector, and seek, positioning at cylinder and head,retry, etc. which are all automatically carried out by HDC. Further, if the alternate sector processing is performed when formatting the disk drive, the alternate sector search is carried out automatically at time of command execution.
- o As disk read/write and DMA transfer are carried out in parallel using a buffer, multi-sector read (write) can be executed without sector interleaving. (However, when disk transfer rate is 5Mbps,system clock must be more than 4MHz, and when 10Mbps, it must be more than 6MHz.)
- o Multiple CCWs can be executed consecutively by indicating next CCW address.

4-2 Format of CCW

CCW consists of 8 words (16 bytes). The basic format is as follows.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	GO	0	ES 1	ES 0	STATUS (4 bit)				0	COMMAND			0	EC 2	EC 1	EC 0
1	BASE															
2	COUNT															
3	CHAIN															END
4	HOSTSH															
5	HOSTSL															
6	DISKSH															
7	DISKSL															

GO : GO bit. This bit should be set at "1" when a command is issued. After completion of CCW, "0" is written by HDC. Polling of this bit allows HDC to operate without interrupt interruption.

STATUS : STATUS information (4 bits) that is written by HDC after execution of CCW.

COMMAND : Command operation code in 3 bits. 8 commands (READ, WRITE, FORMAT, VERIFY, RTZ, SET, REPORT, BOOT)

BASE : Indicates low order 16 bits of memory address storing the CCW parameter list.

(Note) For the parameter list, refer to the explanation in 4-5.

COUNT : Basically, indicates number of transfer bytes.

CHAIN : Indicates CCW's chain address.

END : END bit. When this bit is set to "1", it indicates that the CCW chain ends at that CCW.

HOSTSH : Indicates high order 16 bits of DMA transfer address.

HOSTSL : Indicates low order 16 bits of DMA transfer address.

DISKSH : Indicates high order 16 bits of DISK logical address.

DISKSL : Indicates low order 16 bits of DISK logical address.

ES1,ES0 : Extra status. After execution of CCW, serial interface signals ES1 and ES0 are written by HDC. User can define as desired.

EC2,1,0 : Extra command. This value of CCW is output to EC2, EC1 or EC0 of the external shift register through output by HDC when CCW is executed. This signal is defined by user.

The 14th, 7th and 3rd bit of the first word of CCW must always be set to 0.

4-3 Explanation of All CCWs

4-3-1 FORMAT CCW

This is a command used to format the hard disk drive.
It is possible to format either the entire disk drive or a part of disk drive for every track.

	1	0	X	X	0	0	0	0	0	0	1	0	0	X	X	X
1	BASE															
2	COUNT															
3	CHAIN															
4	HOSTSH															
5	HOSTSL															
6	DISKSH															
7	DISKSL															

COUNT : Specifies number of tracks to be formatted.

HOSTSH : Address of main memory storing the format ID information.
HOSTSL

DISKSH : Logical address of a disk of which formatting begins.
DISKSL

[Function]

Basically, the formatting is made for every track and therefore, it is possible to change the sector interleaving method by track. For the track format, refer to 3-6.

The format ID data (sector interleaving data) shall be made available in the format shown in next page and set in memory addressed by HOSTSH and HOSTSL

Here, Cylinder No. is written into "WCYLIND." Normally, however, if WCYLIND is left 0, the same cylinder number as the physical cylinder number is automatically written. "SECTOR" shows Sector No.

When the sector interleave is common to all tracks, all tracks can be formatted at one time with WCYLIND=0, COUNT=number of cylinders x number of heads, and DISKSH/SL=0.
Whenever formatting the tracks, the physical cylinders and logical

cylinders must be always match. Only exception is when an alternate track for the alternate sector processing is formatted. (For the alternate sector processing, refer to 4-6.)

ID Data

HOSTSH,SL ---

10 bit	6 bit
WCYLIND	SECTOR
WCYLIND	SECTOR
WCYLIND	SECTOR
.	.
.	.
.	.
WCYLIND	SECTOR

WCYLIND 10 bits, max. 1023 cylinders (as 3FF is used for the alternate sector designation).
SECTOR 6 bit, max. 64 sectors.

4-3-2 READ CCW

This is a command used to transfer data (COUNT shows the total bytes) from the logical address of a disk to the main memory address shown by HOST/HOSTSL.

1	0	X	X	0	0	0	0	0	0	0	1	0	X	X	X
BASE															
COUNT															
CHAIN															
HOSTSH															
HOSTSL															
DISKSH															
DISKSL															

COUNT : Indicates number of read data transfer bytes. When "0" is input, number of transfer bytes is regarded to be 64K bytes.

HOSTSH : Read data transfer destination address
HOSTSL

DISKSH : Read data disk logical address
DISKSL

[Function]

This command includes the seek operation. As the present head location is stored in the register in HDC, HDC calculates a physical address from the logical address of this time, compares it with the present location, and seeks the head as necessary. The automatic retry function (including a recalibration) is available for erroneous reading. (Refer to the retry in the explanation of parameters in 4-5.)

4-3-3 WRITE CCW

A command to transfer number of bytes shown by COUNT to the logical address of a disk from the main memory address shown by HOSTSH/ HOSTSL.

1	0	X	X	0	0	0	0	0	0	1	1	0	X	X	X
BASE															
COUNT															
CHAIN															
HOSTSH															
HOSTSL															
DISKSH															
DISKSL															

COUNT : Indicates number of write data transfer bytes.
When "0" is set, number of transfer bytes is regarded to be 64K bytes.

HOSTSH : Write data transfer destination address
HOSTSL

DISKSH : Write data disk logical address
DISKSL

[Function]

Basically, the function of this command is nearly the same as READ command except the transfer direction. In writing smaller data than the physical sector, making a judgment automatically, HDC reads that sector in the internal buffer, modifies the write data on the buffer, and writes it on the original sector.

4-3-4 VERIFY CCW

This command compares data of number of bytes shown by COUNT from the disk logical address shown by DISKSH/DISKSL with data on the main memory shown by HOSTSH/HOSTSL. If there are unmatched data, status=2 (DATA ERROR) is returned.

1	0	X	X	0	0	0	0	0	1	0	0	0	X	X	X
BASE															
COUNT															
CHAIN															
HOSTSH															
HOSTSL															
DISKSH															
DISKSL															

[Function]

This is a command to compare disk data with memory data. This command is used to check if data is properly written onto a disk. In addition, in finding a defective sector at time of formatting, use of this command is more effective rather than use of a method to search ECC error using READ command.

4-3-5 RTZ CCW

This command brings the disk drive head to track 0 position.

1	0	X	X	0	0	0	0	0	1	1	0	0	X	X	X
BASE															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CHAIN															
- - -															
- - -															
- - -															
- - -															

[Function]

This command brings the disk drive head to track 0 position.
At time of power ON, the register contents of the head position in HDC is in out of accord with the actual head position, and it is therefore necessary to issue RTZ command (to all disk drives).

At time of normal read/write, the calibration is carried out automatically at time of retry if RETRY 2 is set to other than 0 by a parameter and therefore, it is not necessary to issue RTZ command.

4-3-6 SET CCW

This CCW is used to change ROOT address of a CCW (the top address where the CCW is positioned).

* : LOCK

1	0	X	X	0	0	0	0	0	1	0	1	*	X	X	X
BASE															
ROOTH															
ROOTL															
- - -															
- - -															
- - -															
- - -															

LOCK : When "1" is set, change of ROOT address is inhibited on and after this CCW.

ROOTH : High order 16 bits of ROOT address.
ROOTL : Low order 16 bits of ROOT address.

(Note) ROOT address after reset has been set at 0000 FFF0.

[Function]

This is a CCW used to change ROOT address of a CCW (the top address where that CCW is positioned.)
If CCWs are erroneously chained, HDC runs away. Root address must be changed, ROOT address will become indistinct unless it is reset. Therefore, after power ON, issue SET command with LOCK=1.

4-3-7 REPORT CCW

This is a command used to transfer values of the register in HDC to a main memory shown by HOSTSH/HOSTSL.

1	0	X	X	0	0	0	0	0	1	1	1	0	X	X	X
BASE															
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
CHAIN															
HOSTSH															
HOSTSL															
- - -															
- - -															

Data is output in the format shown below.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R_C_O_U_N_T															
1	ECCHD						ECCCYL									
2	ECCCNT						ECCDIV		ECCSEC							
3	CYLIND															
4	HEAD															
5	SECTOR															
6	SCYL															
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	CPOS0															
9	CPOS1															
10	CPOS2															
11	CPOS3															

RCOUNT : In case of READ/WRITE, indicates number of remaining transfer bytes.
ECCHD : Indicates Head No. of the head that caused ECC error lastly.
ECCCYL : Indicates Cylinder No. of the cylinder that caused ECC error lastly.
ECCSEC : Indicates Sector No. of the sector that caused ECC error lastly.
ECCDV : Indicates Drive No. of the drive that caused ECC error lastly.
ECCNT : Number of ECC errors taken place.

CYLIND/HEAD/SECTOR : Value of the cylinder, head/sector being accessed by HDC.

SCYL : Cylinder No. of the cylinder that was (or tried to be) seeked lastly.
CPOSn : Cylinder no. at the position of the nth drive's head.

[Function]

REPORT command is a command that is used to output register data in HDC. Register data is used for error analysis, etc. This command is principally used for detecting any defective sector or a place at where an error was caused at time of the formatting.

4-3-8 BOOT CCW

This is a special CCW and is only executed after reset. This command transfers 0 cylinder, 0 head or 0 sector data at address 0000 FF00 unconditionally, and executes a CCW from ROOT address (0000 FFF0).

ALL 1 OR ALL 0
- - -
- - -
- - -
- - -
- - -
- - -
- - -
- - -

[Function]

This is a special CCW and is valid time only after reset. This command reads out 0 cylinder, 0 track or 0 sector data at address 0000 FF00 and executes a CCW from ROOT address (0000 FFF0).

If a CCW to transfer a BOOT program to a memory is loaded in 0 cylinder, 0 track or 0 sector, a system that is able to start up without BOOT ROM can be constructed.

4-4 Explanation of STATUS

Results of the execution of CCW are written into the first word of CCW by HDC as status data. Status data is in 4 bits and contains 15 data. If status data is more than 2, it is regarded as the fatal error and execution of CCW is stopped even when there is the chain designation.

(1) status 0 : NO ERROR
Indicates that CCW has been properly completed. Even when there was a retry at time of the disk read/write, if CCW was completed within specified number of times, it is regarded to have been properly completed.

(2) status 1 : ECC CORRECTED
Indicates there was ECC corrected data when CCW was being executed. It is regarded as the proper completion and if there is the chain designation, CCW is continuously executed.

(3) status 2 : DATA ERROR
a) Indicates that data without ECC error (or ECC correctable data) could not be read within specified number of retrys during the disk read.
b) When data did not match on VERIFY CCW.
In both cases, HDC suspends execution of the CCW at that point of time and returns this status.

(4) status 3 : ID NOT FOUND
Indicates that applicable ID (cylinder, sector, head) could not be found when read/write executes. (CRC error is also included.)

(5) status 4 : DATA AM NOT FOUND
Indicates that the data address mark A1F8 pattern which must exist in the data field could not be found.

(6) status 5 : FORMAT OVER FLOW
Indicates that no index signal was received within 3ms after completion of the formatting of one track when the formatting was executed.
Number of sectors of one track is erroneously designated mostly and re-formatting is necessary in these cases.

(7) status 6 : NOT READY
indicates there was no disk READY signal when CCW except for SET and REPORT commands was executed. The process will ends without execution of CCW. However, in case of BOOT CCW, it is waited infinitely till READY becomes 1.

(8) status 7 : WRITE PROTECT
Indicates that it was tried to write into the write inhibit area using WRITE command.
a) When there was a write protect signal.
b) When it was tried to write in the write inhibit area designated by the parameter list.

(9) status 8 : CCW ERROR
Indicates there is violation of the format of CCW.
a) In SEG mode, the transfer was specified just like to stride across the segment boundary.
b) When any one of BASE, COUNT (except FORMAT), HOSTSL, DISKSL, or ROOTL is an odd number.
c) When SET command is newly issued after LOCK by previous SET command.
d) BOOT command other than all 0 or all 1.
e) When a value of BASE is in FFF1 - FFFF.

(10) status 9 : EOP ERROR
Indicates that HDC accepted EOP/signal during DMA transfer of data. HDC stops DMA transfer.

(11) status A : ABORT
Indicates that GO/signal has been accepted after HDC has been started and before completion of execution by HDC. HDC stops the execution at an appropriate phase.

(12) status B : WRITE FAULT
Indicates the possibility that the disk contents have been destructed.
a) When write fault signal is output from the drive.
b) When the drive is not ready when execution of CCW was completed.

(13) status C : TRACK0 OVER
Indicates that track 0 isn't detected even when step pulses have been output by 1,023 times.

(14) status D : SKCOMP OVER
Indicates that after transmitting step pulses, HDC had not been accepted Seek Complete signal within the specified time. (The specified time is approx. 400 ms at CLOCK-10 MHz and more than 400ms at CLOCK-below 10 MHz.)

(15) status E : INDEX OVER
Indicates that index signal could not been detected under formatting.

(NOTE)
HDC has a built-in timer and has been so designed that Hunging up isn't caused by abnormality of the disk drive. In the following cases, however, no response or runaway may be caused:
(1) No response
- o When system bus request cannot be taken over infinitely.
- o When no response signal to interrupt request is received infinitely.
- o When CCW, PARAMETER, ID data, and REPORT transfer are in the illegal address space.
- o When CCWs are erroneously chained.

(2) Runaway
- o When data transfer address shown by CCW and another CCW overlap each other.
- o When CCWs are erroneously chained.

4-5 Explanation of Parameters

The parameter list specifies attribute for each disk drive by 8 word data from address shown by CCW's BASE.

0	0	0	0	0	0	0	0	0	PX	E	S	I	NV	D1	DO
TK								VECTOR							
0	BIAS			HEADC				0	0	SECT					
0	0	0	0	RETRY1				RETRY2		STEPT					
GAP1				SYNC				GAP2			0	0	0		
0	0	0	0	0	0	R W C C									
0	0	0	0	0	0	PCOMPC									
0	0	0	0	PROTA											

PX : This parameter makes pre-compensation signals EARLY and LATE valid (PX=1).

E : Performs the automatic ECC correction (E=1)

S : Outputs sync. signal for MMU when S=1. Further, under this mode, data transfer having a carry to high order address is inhibited.

I : Makes HDC interrupt valid (I=1)

NV : Makes the vector interrupt valid (NV=0)

D1/D0 : Coded disk drive number

TK : Time constant. A value to decide the timer unit used in HDC. Input a value calculated according to the following equation:

CLOCK = F (MHz)

A value calculated by TK = 1000* F/64 (raise to a unit)

VECTOR : Output vector value

BIAS : Specifies number of alternate tracks (For alternate track refer to 4-6.)

HEADC : (No. of heads of one drive) - 1

SECT : (No. of sectors of one track) - 1

RETRY1 : A value of retries on the track when read/write is executed.

RETRY2 : HDC has been so designed that retry is executed once more after recalibration following one retry. This is a value of recalibration to be carried out.

STEP : Sets up stepping pulse cycle.

Cycle T = STEPT*0.25ms

However, when STEPT=0, it is about 280* (CLOCK cycle), making the buffer seek possible. (About 70us at 4 MHz)

GAP1	:	Value of GAG1 in case of formatting.
GAP2	:	Value of GAG2 in case of formatting.
SYNC	:	Value of SYNC in case of formatting. * Refer to the track format.
RWCC	:	This parameter sets the disk interface signal RWC to "1" at cylinder with a value above this value. (Reduce write current)
PCOMPC	:	Carries out the precompensation at cylinders with a value above this value.
PROTA	:	When this value is n, writing to disk addresses lower than $n*2^{16}$ is inhibited.

Functions provided by Parameters

Precompensation : PX = 1

In writing a kind of pattern when data is written onto a disk, a writing position and reading position may shift each other for nature of magnetic substance. To compensate this shift, a process called the precompensation is performed. EARLY and LATE signals required for this process are output.

ECC Correction : E = 1

HDC has the built-in ECC circuit to allow detection and correction of burst error in 11 bits or less. If ECC error occurs when E = 1, ECC error correction is automatically carried out using the internal buffer data and corrected data is re-transferred.

Connection of MMU : S = 1

It is possible to connect HDC directly to Z8000 System MMU (Z8010, Z8015). Under this mode, DMA transfer cycle will become 4 clocks. Further, such a transfer that a carry is caused on high order 16 bits of DMA address by one time transfer is inhibited.

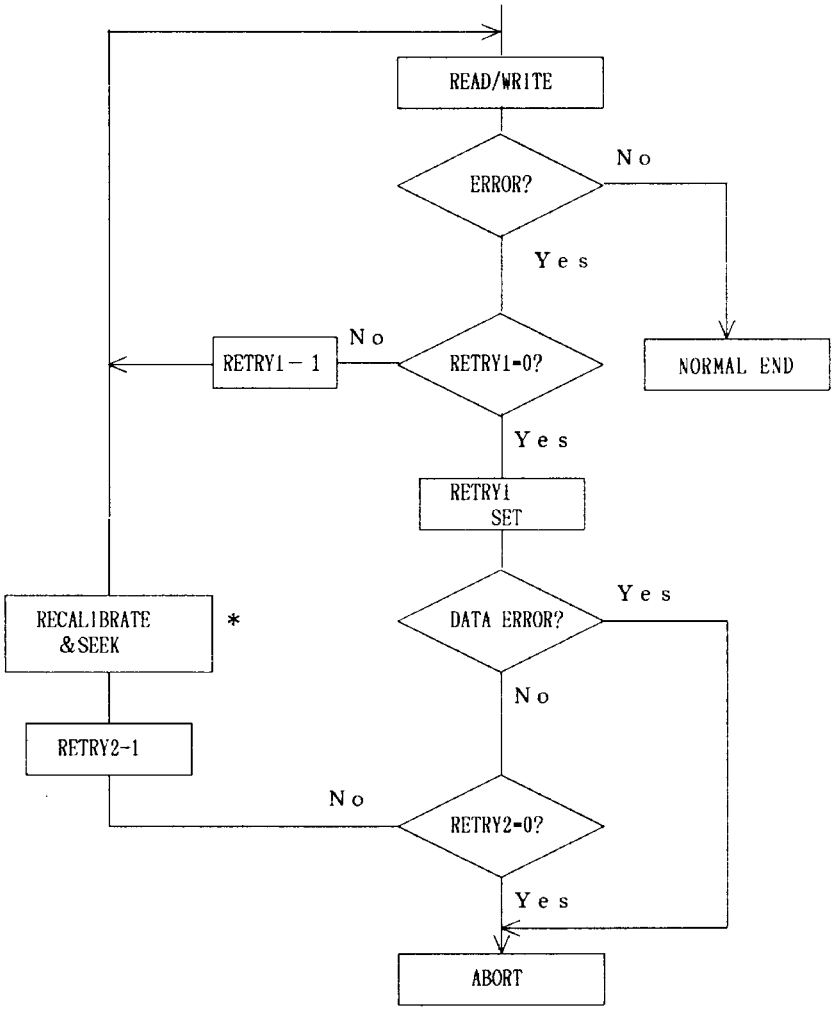
Interrupt : I, NV

When I = 1, HDC generates interrupt request. The interrupt protocol is in accordance with the Z-bus protocol. When NV = 0, the vector interrupt is generated and the VECTOR contents are output into the bus. After receiving the interrupt acknowledge, HDC performs the postprocess for about 100 clocks during when GO signal cannot be accepted. (When used in the polling, about 200 clocks after GO bit becomes 0.)

Retry Function : RETRY 1, RETRY 2

When RETRY1 or RETRY2 is set, HDC performs retry automatically. The retry is performed only when E = 0 and no ID could be found or when ECC error occurred and no ID could be found at E = 1.

The flowchart for executing RETRY1/2 is shown below.



*Including alternate sector processing

Step Rate : STEPT

Step rate is programmable and cycle can be set at intervals of 2.5ms (STEP*0.25ms). When STEPT=0, the buffer seek mode results.

Write Protection Function : PROTA

The function to inhibit write operation into disk drive from logical address 0 for every 64K bytes. When PROTA=1, write operation into the logical addresses 0 through FFFF of a disk is inhibited.

4-6 Alternate Sector Process

Whenever the disk drive is used, it is always necessary to take a defective sector into consideration. It is a normal practice to search defective sectors when formatting and take some measures not to use those defective sectors. There are various measures; one measure is that a host CPU stores information on defective sectors in a memory and avoids to use such sectors, and another measure is to provide alternate sectors (tracks). The TMPZ80C47P has the function to perform the alternate sector process automatically and therefore, a host CPU is not burdened.

If the alternate sector process is performed when Format CCW is executed, the alternate sector process is automatically carried out as read/write operation and therefore, a disk can be treated as a complete disk from the host CPU side.

The automatic alternate sector processing method is to,

1) format the entire area of disk drive.
2) find out defective sectors using such commands as READ, WRITE, VERIFY, etc.
3) reformat a track having defective sectors with defective sector format information put in FFFF (non-existing ID No.).
4) format the 0th cylinder on the side (same head) having defective sectors using defective sector's ID.
5) if there are many defective sectors, use the 1st, 2nd ... cylinders.
6) set the same value as the used cylinder as bias.

Thus, HDC cannot find ID when tried to read/write a defective sector and returning to the 0 cylinder, searches that defective sector from the 0 cylinder to the cylinder that has been set with BIAS.

4-7 Example of CCW Execution

Command issue , HDC starting and execution status are explained using a definite example.

[Example]

To read 200H bytes from the disk logical address 1234 of Disk Drive 1 at address 400H of a memory and write this data into address 4500H of Disk Drive 2.

[Creation of Command List]

First, a list of commands that are desirable to be executed is created at CCW's ROOT address. If the list consists of more than two commands, commands must be chained successively. In this case, ROOT address is FF00H and CCW will become as shown in Fig. 4-7-1.

* Execution of CCW always starts from ROOT address. Even when previous CCW stopped the execution as errors occurred on the middle of chaining, if CCW is started by GO signal, CCW is executed from ROOT address instead of next of the chain.

[Starting HDC]

When a command list has been created, a GO signal is given to HDC. HDC takes in and executes CCW quite independently of a host CPU and therefore, after giving the GO signal, the host CPU waits an interrupt from HDC while performing other jobs.

(Taking CCW by HDC)

When received the GO signal, HDC takes in the first CCW from ROOT address by DMA. If no format violation is found on CCW, CCW is analyzed and executed. In this case, READ command is first executed.

(Executing and Chaining by HDC)

HDC calculates physical address from the disk logical address given by CCW, and transfers data to a memory via the internal buffer.

When CCW has been properly executed, HDC returns the status to the CCW and if chain is specified, reads next CCW from the chain address.

* If the status is more than "2", it is regarded as the fatal error and after returning the status, HDC carries out the end process (if I=1, the interrupt request is generated.)

* If the host CPU confirms the proper end while polling GO bit and the status, it is possible to use data transferred by CCW before the chaining of all CCWs ends and the interrupt request signal is received.

(Taking Parameters)

HDC performs read/write according to the disk's attribute shown on the parameter list. Since it is useless to read the parameter list every time when CCW is taken in, the parameter list should be re-read only when CCW's Base is changed from the previous time. In this case, before execution of the second CCW, the parameter list must be always read.

* The above indicates that re-writing of parameters on the list does

not necessarily assure change of parameters in actual execution.

(Ending HDC)

After performing the chaining and executing CCW with END bit "1", HDC begins the end operation.

HDC returns the status to the last CCW and when I=1 has been set, generates an interrupt signal. In the case of this example, an interrupt signal is generated after executing WRITE command.

[Starting HOST CPU]

The host CPU knows end of CCW execution by receiving the interrupt signal from HDC or by polling GO bit of CCW. The host CPU makes a judgment the execution has been properly completed or not by checking the status of each CCW.

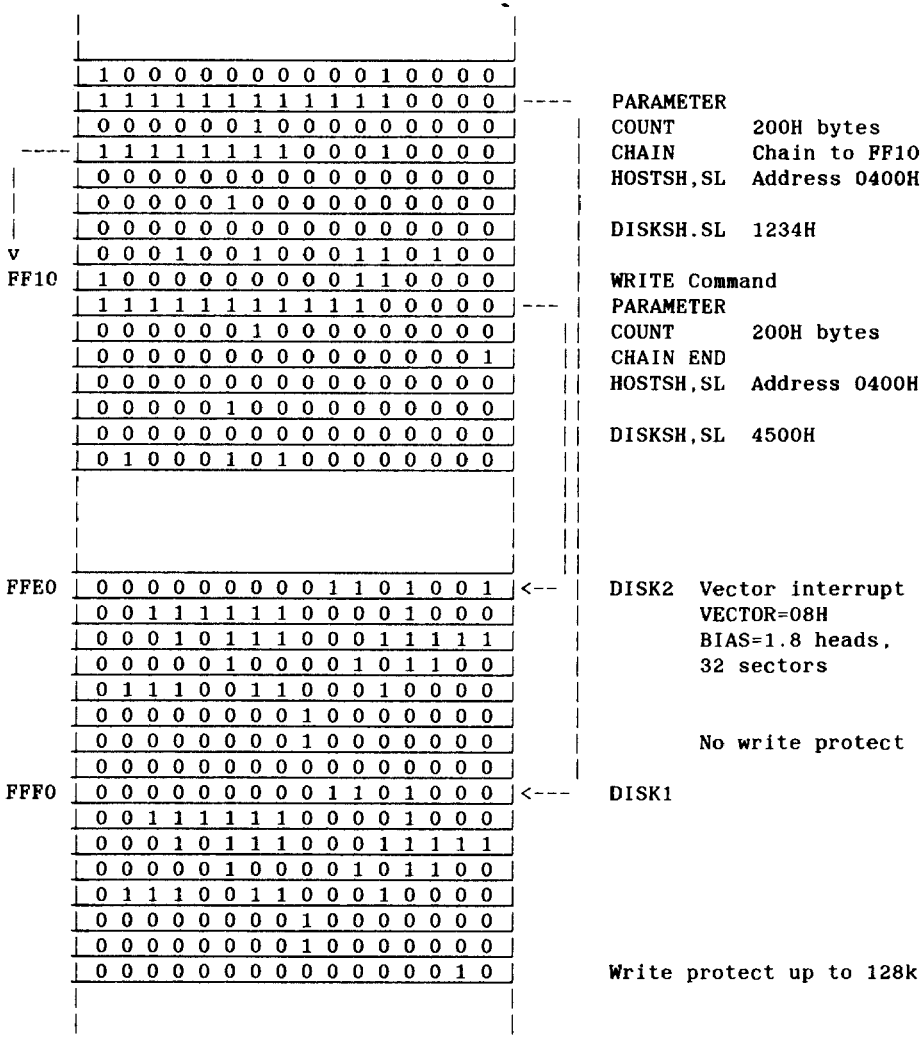


Fig. 4-7-1 CCW and Parameters

5. Electrical Characteristics

5-1 Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT
Supply Voltage Range	VDD	-0.5 to +7.0	V
Input Voltage Range	VIN	-0.5 to +7.0	V
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Tstg	-65 to +125	°C

5-2 DC Characteristics (Ta = 25°C VDD = +5V)

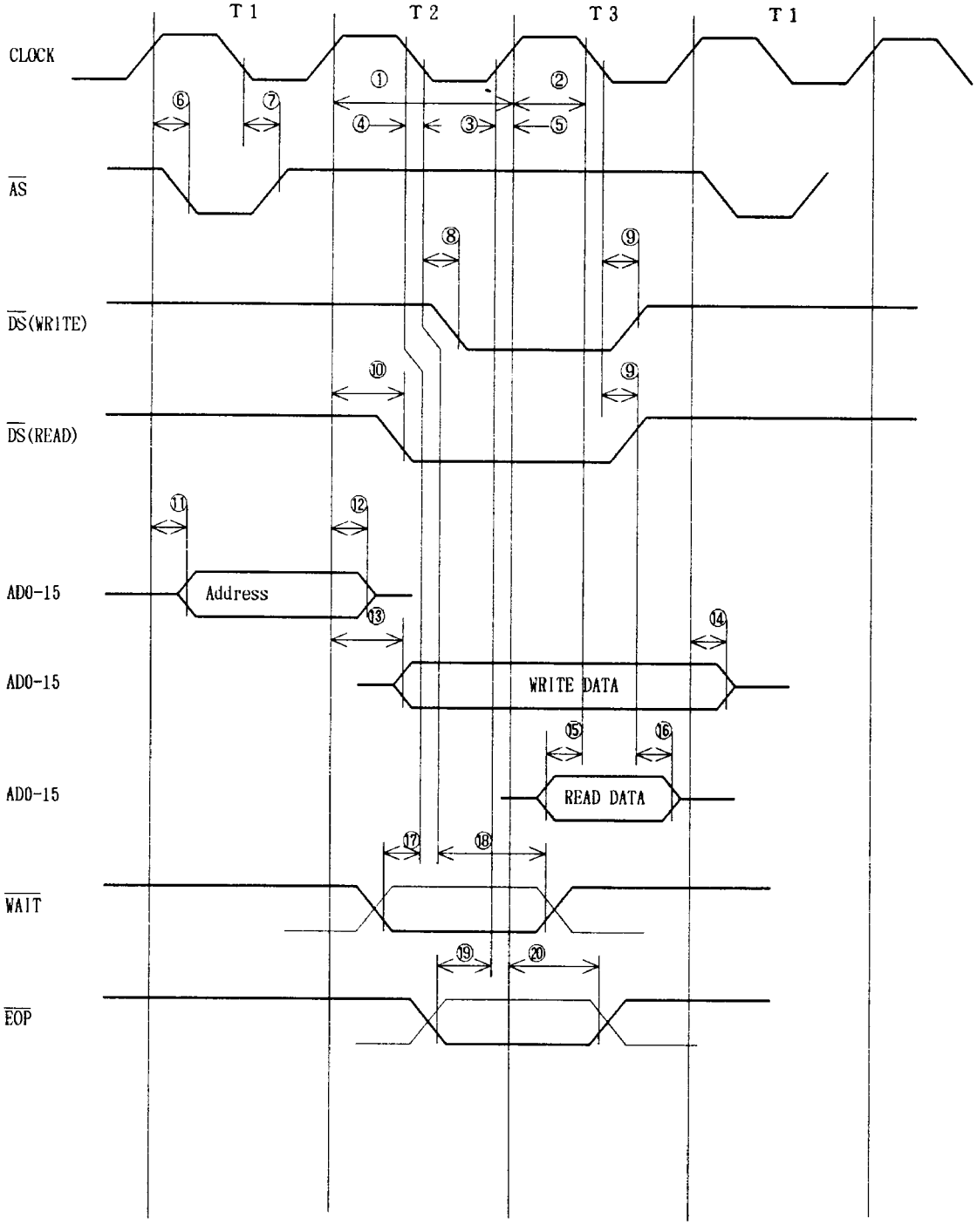
ITEM	SYMBOL	CONDITION	Min.	Max.	UNIT
Input Voltage 1	VIHc	Only CLOCK	VDD-0.4	VDD+0.3	V
Input Voltage 2	VILc	Only CLOCK	-0.3	0.45	V
Input Voltage 3	VIH	Except CLOCK	2.2		V
Input Voltage 4	VIL	Except CLOCK		0.8	V
Output Voltage	VOH		2.4		V
Output Voltage	VOL			0.4	V
Output Current	IOH	VOH = 2.4 V		-250	uA
Output Current	IOL	VOL = 0.4 V	2.0		mA
Power Consumption	IDD	10 MHz	30 Typ.		mA

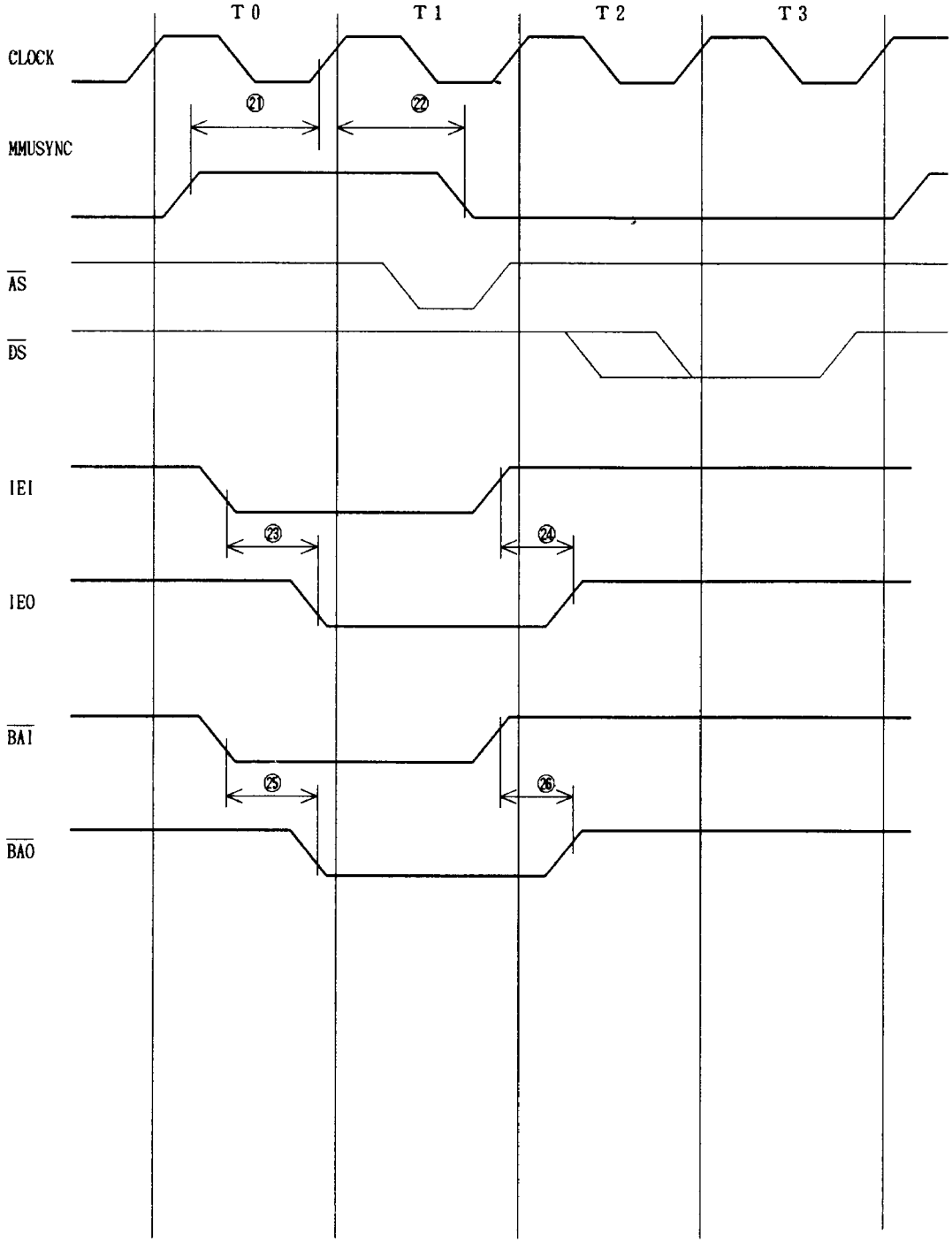
5-3 AC Characteristics

UNIT: (nS)

NO.	SYMBOL	ITEM	6MHz 1)		10MHz 2)	
			MIN	MAX	MIN	MAX
1	TcC	Clock cycle time	165		100	
2	TwCh	Clock pulse width (HIGH)	70		40	
3	TwCl	Clock pulse width (LOW)	70		40	
4	TfC	Clock falling time		10		10
5	TrC	Clock rising time		15		10
6	TdC(ASf)	Clock rise to AS/ fall time		60		40
7	TdC(ASr)	Clock fall to AS/ rise time		80		40
8	Tdc(DSw)	Clock fall to DS/ fall time(write)		80		60
9	Tdc(DSr)	Clock fall to DS/ rise time		65		45
10	TdC(DSR)	Clock rise to DS/ fall time (read)		85		60
11	TdC(A)	address valid		75		50
12	TdC(AZ)	address invalid		55		40
13	TdC(DW)	data valid		75		50
14	TdC(Bz)	data bus invalid		55		40
15	TsDR(C)	read data setuptime	20		10	
16	ThDR(DS)	read data hold time	0		0	
17	TsW(C)	wait pulse setup time	30		20	
18	ThW(C)	wait pulse hold time	10		5	
19	TsEOP(C)	EOP/ pulse setup time	30		20	
20	ThEOP(C)	EOP/ Pulse hold time	10		5	
21	TdMMU(C)	MMUSYNC rise to Clock rise time	70			
22	TdC(MMU)	Clock rise to MMUSYNC fall time	70			
23	TdE1(EOf)	IEI fall to IEO fall time		100		100
24	TdE1(EOr)	IEI rise to IEO rise time		100		100
25	TdB1(BOf)	BAI/ fall to BAO/ fall time		100		100
26	TdB1(BOr)	BAI/ rise to BAO/ rise time		100		100
27	TdDSf(V)	DS/ fall to VECTOR data valid		180		160
28	TdDSr(Vz)	DS/ rise to VECTOR data invalid	0		0	
29	TdDSr(INT)	DS/ rise to INT/ rise time		180		160
30	TdIAK(IEO)	INTACK/ fall to IEO fall time		100		160

1) TMPZ80C47P
2) TMPZ80C47P-10 (Preliminary)


T 1
T 2
T 3
T 1
CLOCK
AS
DS(WRITE)
DS(READ)
AD0-15
Address
AD0-15
WRITE DATA
AD0-15
READ DATA
WAIT
EOP

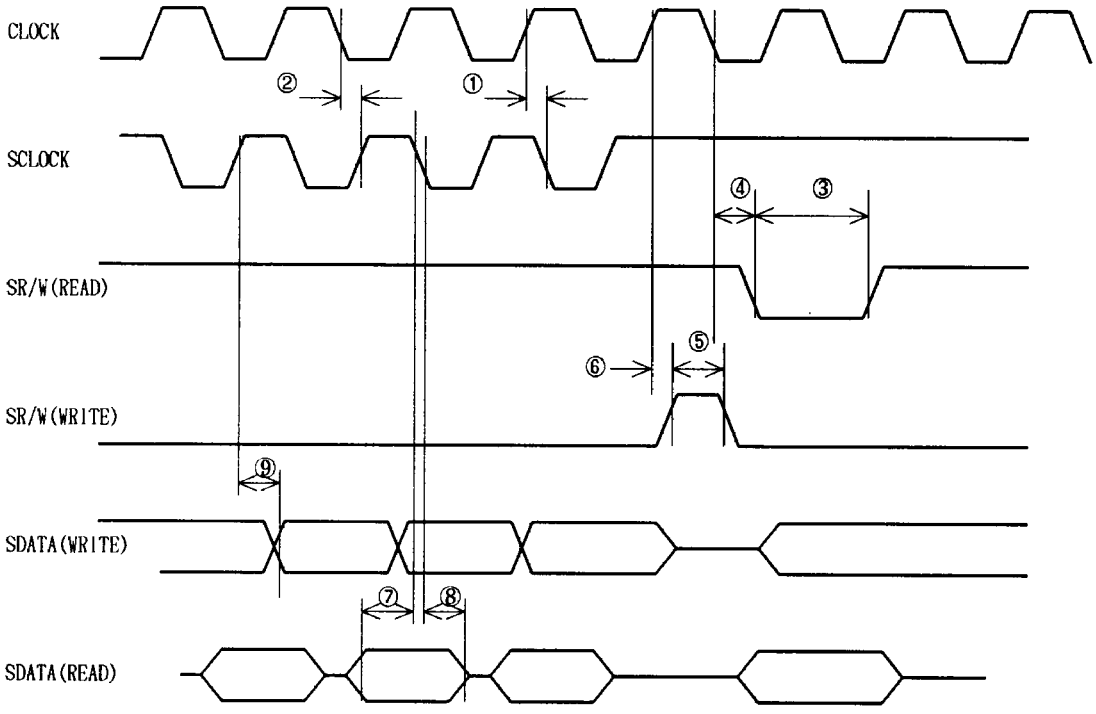

T 0
T 1
T 2
T 3
CLOCK
㉑
㉒
MMUSYNC
AS
DS
IEI
㉓
㉔
IEO
BAI
㉕
㉖
BAO

AC Characteristics (2)

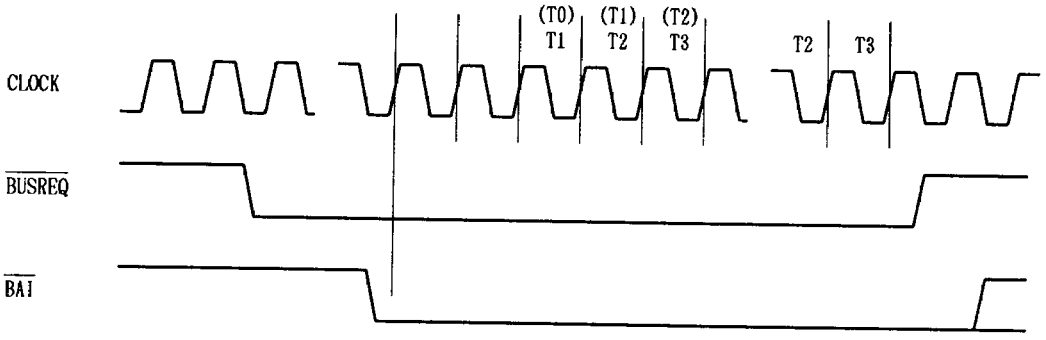
UNIT: (nS)

NO.	SYMBOL	ITEM	6MHz 1)		10MHz 2)	
			MIN	MAX	MIN	MAX
1	TdC(SCf)	Clock fall to SCLOCK rise time	60			40
2	TdC(SCr)	Clock rise to SCLOCK fall time	60			40
3	TwSR/W1	SR/W pulse width (LOW)	100		80	
4	TdC(SR/W)	Clock fall to SR/W fall time		80		40
5	TwSR/Wh	SR/W pulse width (HIGH)	60		30	
6	TdC(SR/Wr)	Clock rise to SR/W rise time		80		60
7	TsSD(SC)	SDATA set up time	50		30	
8	ThSD(SC)	SDATA hold time	0		0	
9	TdSC(SD)	SDATA valid delay time	0		0	

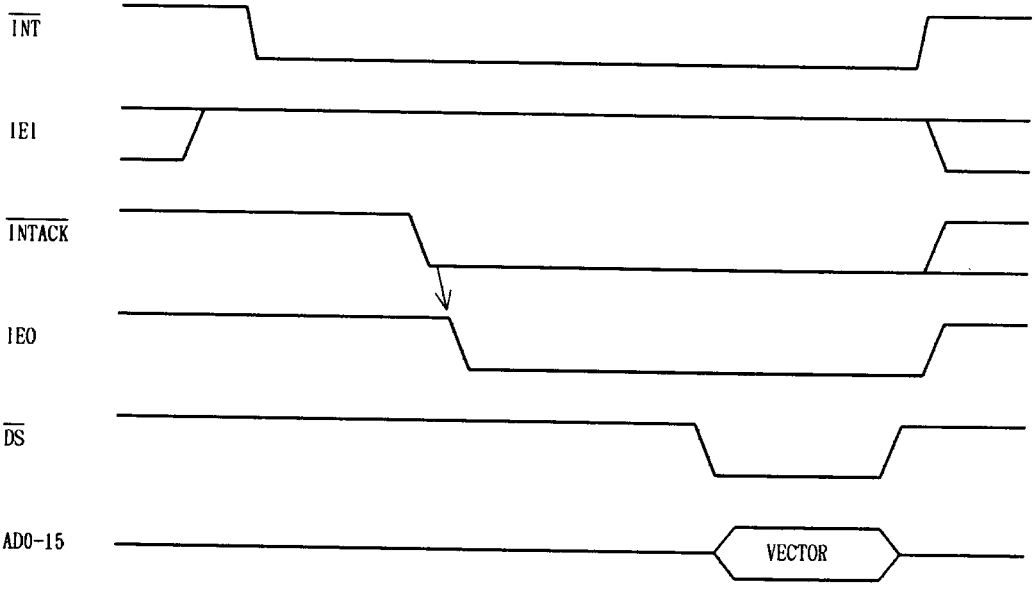
1) TMPZ80C47P
2) TMPZ80C47P-10 (Preliminary)


CLOCK
SCLOCK
SR/W(READ)
SR/W(WRITE)
SDATA(WRITE)
SDATA(READ)
①
②
③
④
⑤
⑥
⑦
⑧
⑨

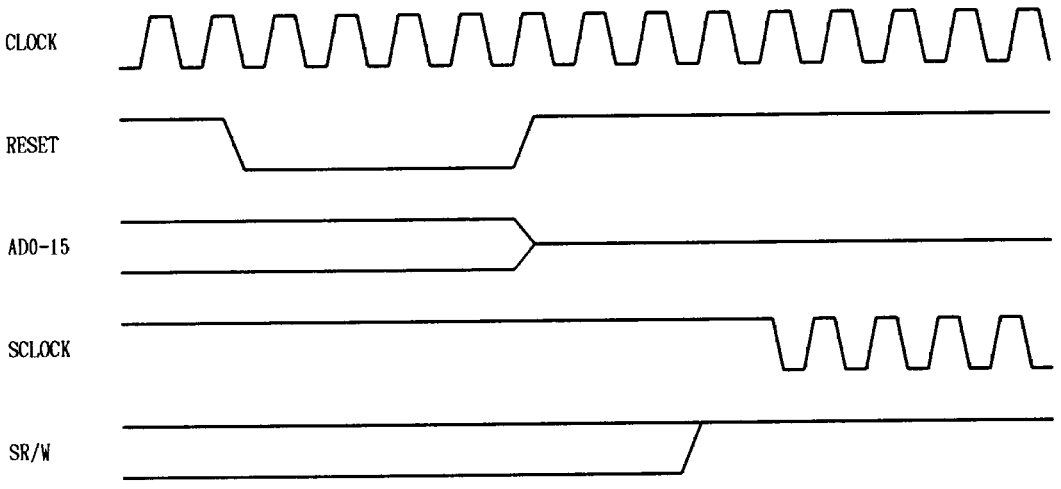
BUS TIMING



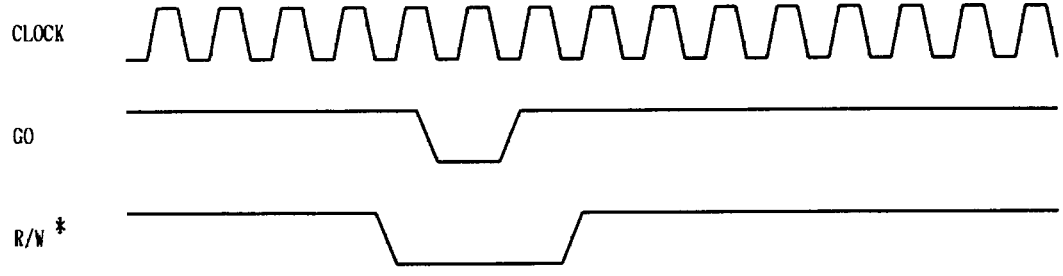
INTERRUPT TIMING



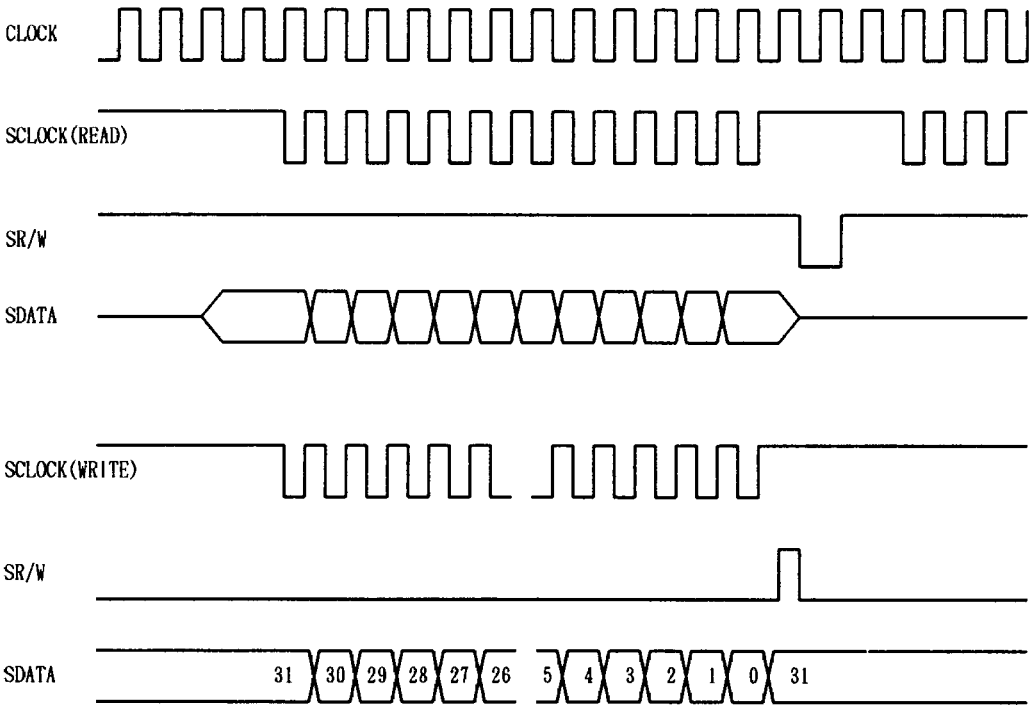
RESET TIMING



GO TIMING



SERIAL I/O TIMING



6. PACKAGE OUTLINE

DIP48PIN (PLASTIC PACKAGE)

Unit: mm