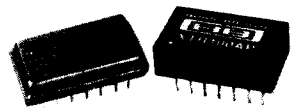
BURR-BROWN®

XTR100



Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 25μV max
  - Low Voltage Drift, 0.5μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- -40°C TO +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE

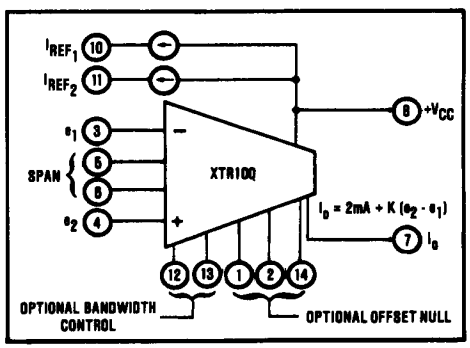
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR100 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage controlled output current source, and dual-matched precision current references. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTD's, thermistors, and strain gauge bridges. State-of-the art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR100 is generally very useful for low noise, current-mode signal transmission.



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PDS-467C

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, +V_{CC} = 24VDC, R_L = 100Ω unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR100AM/AP MIN	XTR100AM/AP TYP	XTR100AM/AP MAX	XTR100BM/BP MIN	XTR100BM/BP TYP	XTR100BM/BP MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS								
Current	Linear Operating Region	4		20	*		*	mA
Current	Derated Performance	3.8		22	*		*	mA
Current Limit	Io min		28	38		*	*	mA
Offset Current Error	Ios, Io = 4mA		±1.5	±4		*	*	µA
Offset Current Error vs Temp.	ΔIos/ΔT		±5	±10		*	*	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA			±20			*	µA
Power Supply Rejection		110	135		*	*		dB
Power Supply Voltage	Vcc, pins 7 & 8, compliance(1)	+11.6		+40	*		*	VDC
Load Resistance	At Vcc = +24V, Io = 20mA			600			*	Ω
	At Vcc = +40V, Io = 20mA			1400			*	Ω
SPAN								
Equation	Rs in Ω, e_1 and e_2 in V	$I_O = 4mA + [0.016U + (40/R_S)](e_2 - e_1)$						
Untrimmed Error(2)	εSPAN	-5	-2.5	0	*	*	*	%
Nonlinearity	εNONLINEARITY			0.01			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
Temperature Effects			30	±100		*	*	ppm %/°C
INPUT CHARACTERISTICS								
Impedance								
Differential			0.4 || 0.047			*		GΩ || µF
Common-Mode			10 || 180			*		GΩ || pF
Voltage Range, Full Scale	Δe = (e_2 - e_1)(3)	0		1	*		*	V
Offset Voltage	Vos			±50			±25	µV
vs Temperature	ΔVos/ΔT		±0.7	±1		±0.25	±0.5	µV/°C
Bias Current	Ib		60	150		*	*	nA
vs Temperature	ΔIb/ΔT		0.30	1		*	*	nA/°C
Offset Current	Ios		10	±30		*	±20	nA
vs Temperature	ΔIos/ΔT		0.1	0.3		*	*	nA/°C
Common-Mode Rejection(4)	DC	90	100		*	*	*	dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	V
CURRENT SOURCES								
Magnitude			1			*		mA
Accuracy	Vcc = 24V, $V_{PIN\ 8}$ - $V_{PIN\ 10, 11}$ = 19V, R_s = 5kΩ, Fig. 3		±0.03	±0.1		±0.015	±0.05	%
vs Temperature				±30			*	ppm/°C
vs Time			±8			*		ppm/mo.
Ratio Match	Tracking							
Accuracy	1 - I_{REF1}/I_{REF2}		±0.006	±0.02			*	%
vs Temperature				±15			10	ppm/°C
vs Time			±1			*		ppm/mo.
Output Impedance		10	20		*			MΩ
TEMPERATURE RANGE								
Specification		-40		+85	*		*	°C
Operating (AM, BM)		-55		+125	*		*	°C
(AP, BP)		-40		+85	*		*	°C
Storage (AM, BM)		-55		+165	*		*	°C
(AP, BP)		-40		+85	*		*	°C

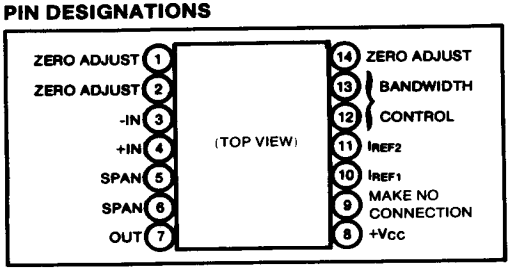
*Same as XTR100AM/AP.

NOTES:
1. See Typical Performance Curves.
2. Span error shown is untrimmed and may be adjusted to zero.
3. e_1 and e_2 are signals on the -IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR100A and XTR100B grades respectively. 2mV FS is also possible with the B grade; but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise.
4. Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

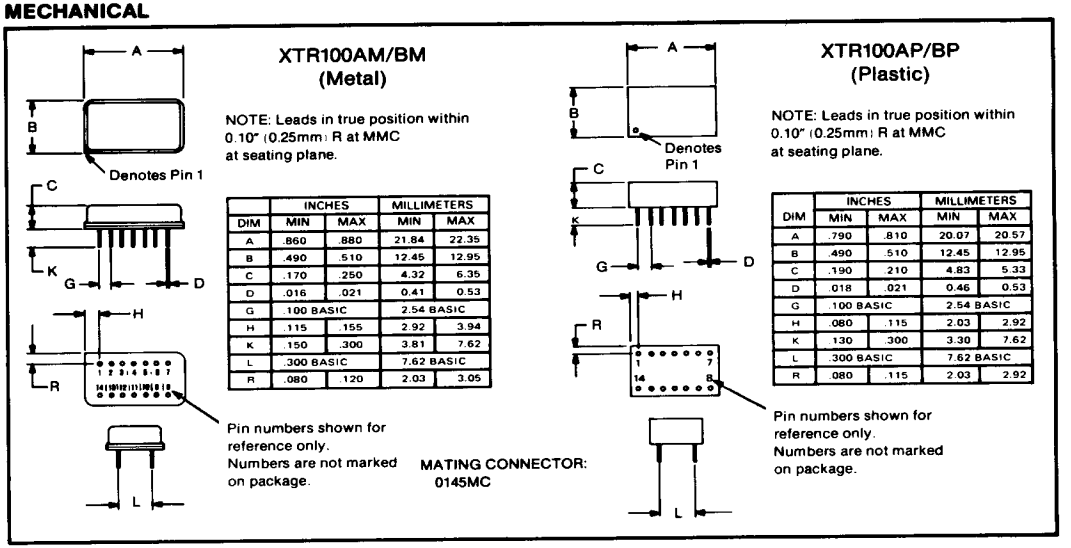
ABSOLUTE MAXIMUM RATINGS

Power Supply, Vcc	40V
Input Voltage, e_1, or e_2	≥ VOUT, ≤ +Vcc
Storage Temperature Range, metal	-55°C to +165°C
Storage Temperature Range, plastic	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	+165°C

PIN DESIGNATIONS



MECHANICAL



XTR100AM/BM (Metal)

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

MATING CONNECTOR: 0145MC

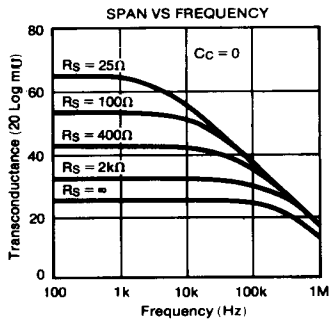
XTR100AP/BP (Plastic)

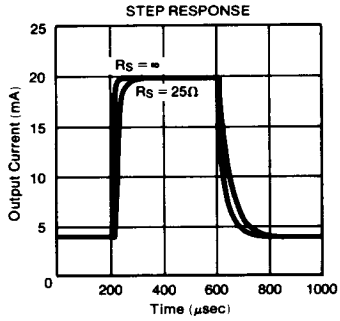
NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

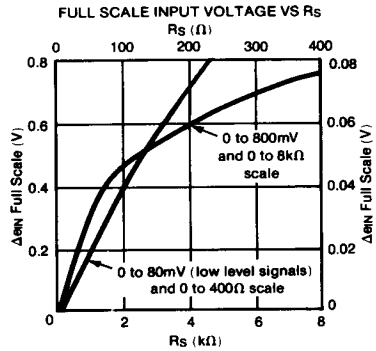
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

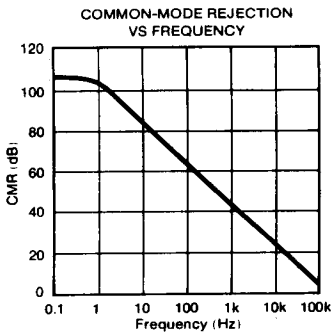
TYPICAL PERFORMANCE CURVES

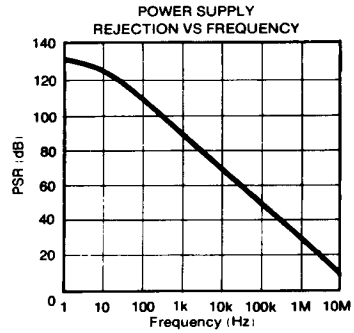
(T_A = +25°C, +Vcc = 24VDC unless otherwise noted)

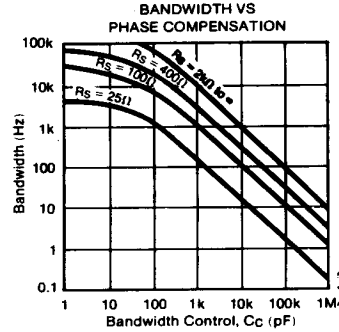


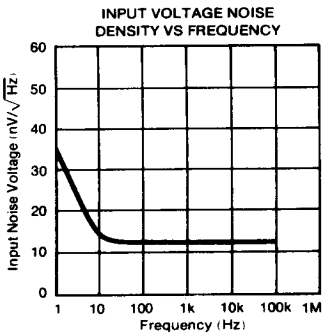


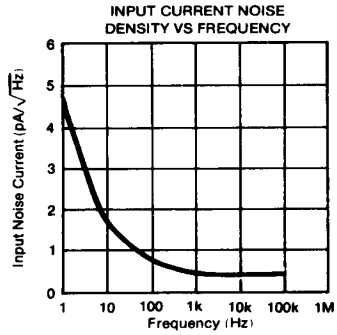


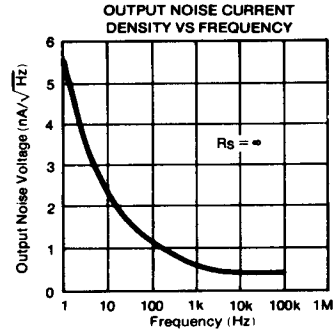












THEORY OF OPERATION

A simplified schematic of the XTR100 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as an instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\Omega + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

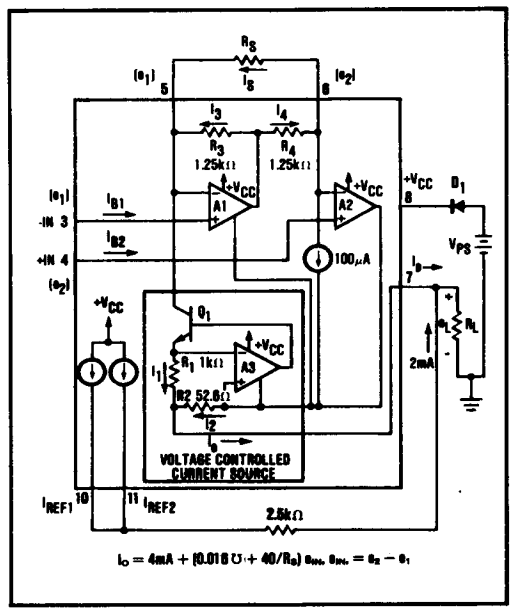


FIGURE 1. Simplified Schematic of the XTR100.

INSTALLATION AND OPERATING INSTRUCTIONS

Major points to consider when designing with the XTR100:

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a $0.01\mu F$ capacitor as close to the unit at possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation
$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$
(e_1 and e_2 measured with respect to pin 7).
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation connect them together and through a $1k\Omega$ resistor to pin 7. Each reference must have between +1V and $+(V_{CC} - 4V)$ with respect to pin 7. Filter with one $0.01\mu F$ or two $0.0047\mu F$ capacitors.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 2).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR100 caused by momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.
8. When the XTR100 is in high gain, use a compensation capacitor, pins 12 and 13, and consider PC board layout which minimizes parasitic capacitance.

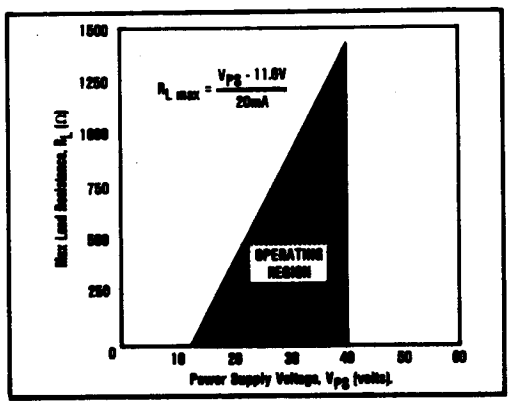


FIGURE 2. Power Supply Operating Range.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of ΔI_{OFS}, $[(0.016\text{Ω}) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16mA$.

Solving for R_S;

$$R_S = \frac{40}{\Delta I_O/\Delta e - 0.016\text{Ω}} \quad (1)$$

For example, if $\Delta e_{IN_{FS}} = 100mV$ for $\Delta I_{O_{FS}} = 16mA$

$$R_S = \frac{40}{(16mA/100mV)} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

The internal circuitry of the XTR100 is such that both e_1 and e_2 must be kept approximately 5V above the voltage at pin 7. This is easily done by using one or both current sources and an external resistor R_2. Figure 3 shows the simplest case - a floating voltage source e'_2. The 2mA from the current sources flows through the $2.5k\Omega$ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$

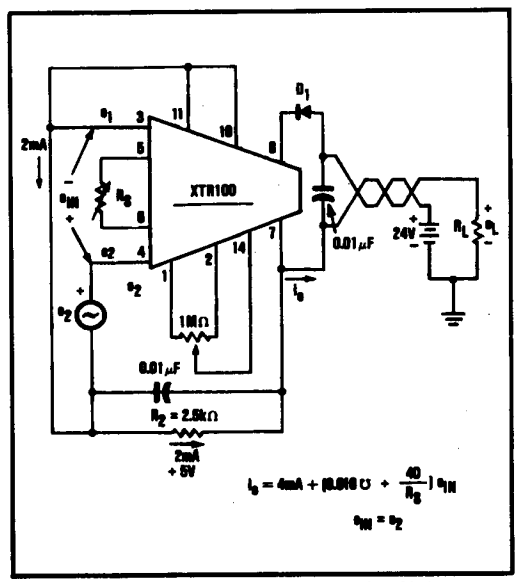


FIGURE 3. Basic Connection for Floating Voltage Source.

Figure 4 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources.

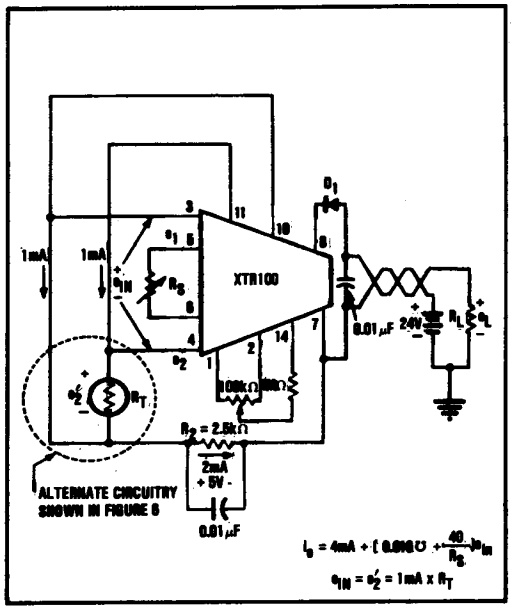


FIGURE 4. Basic Connection for Resistive Source.

CMV AND CMR

Thus the XTR100 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications. If the inputs are biased at some other CMV then an input offset error term is (CMV - 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 5 and 6(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20µV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3µV/°C per 100µV of induced offset.

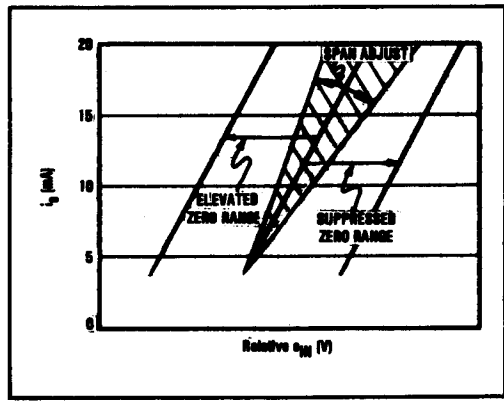


FIGURE 5. Elevation and Suppression Graph.

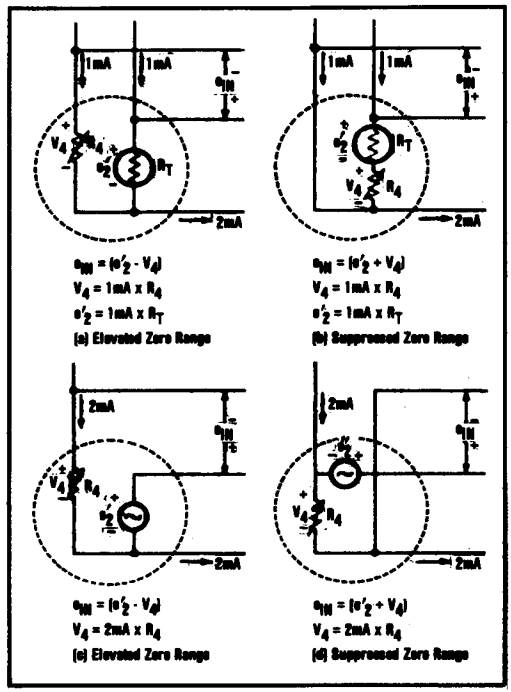


FIGURE 6. Elevation and Suppression Circuits.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR100 ideal for a variety of two-wire transmitter applications. It can be used by OEM's producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise

interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR100 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1 - RTD Transducer shown in Figure 7. **Given a process with temperature limits of +25°C and +150°C, configure the XTR100 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.**

Computing R_S.

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span) the span of e_{IN} is 1mA x $(100\Omega/266°C)$ x 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{in}} - 0.016\,\mho}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - 0.016\,\mho} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

Computing R_4:

$$\text{At 25°C, } e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$$
$$= 1mA \times 109.4\Omega$$
$$= 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA the input circuitry shown in Figure 7 is used.

e_{IN} is made 0 at 25°C
or $e'_{2\,25°C} - V_4 = 0$
thus, $V_4 = e'_{2\,25°C} = 109.4mV$

$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

Computing R_2 and checking CMV:

At 25°C, $e'_2 = 109.4mV$

$$\text{At 150°C, } e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$
$$= 156.4mV$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage they may be ignored in computing R_2 as long as the CMV is met.

$R_2 = 5V/2mA = 2.5k\Omega$

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

The +4V to +6V CMV requirement is met.

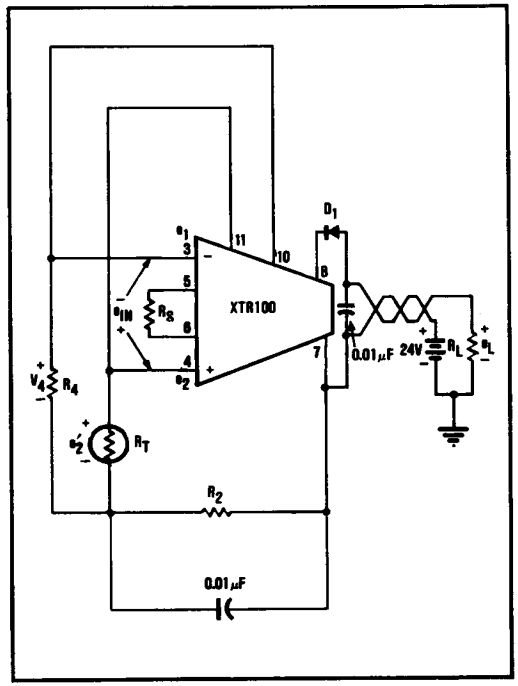


FIGURE 7. Circuit for Example 1.

EXAMPLE 2 - Thermocouple Transducer shown in Figure 8. **Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR100 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C, this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.**

Establishing R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}} = 58mV$).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\,\mho}$$

$$= \frac{40}{\frac{16mA}{58mV} - 0.016\,\mho} = \frac{40}{0.2599}$$

$R_S = 153.9\Omega$

Selecting R_4:

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ ($V_{TC} = -1.28mV$) and $T_D = 25°C$ ($V_D = 0.6V$). A circuit is shown in Figure 8.

V_{TC} will be -1.28mV when $T_{TC} = 0°C$ and the reference junction is at +25°C. e_1 must be computed for the condition of $T_D = +25°C$ to make $e_{IN} = 0V$.

$V_{D_{25°C}}$ = 600mV.
$e_{1_{25°C}}$ = 600mV x 51/2051 = 14.9mV
e_{IN} = $e_2 - e_1 = + V_{TC} + V_4 - e_1$
with e_{IN} = 0 and $V_{TC} = -1.28mV$
V_4 = $e'_1 + e_{IN} - V_{TC} = 14.9mV + 0V - (-1.28mV)$
1mA x R_4 = 16.18mV
R_4 = 16.18Ω

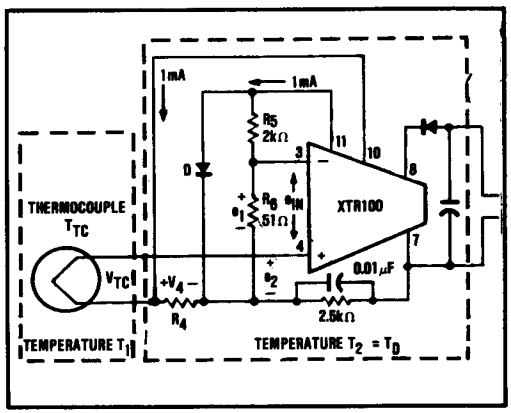


FIGURE 8. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

Cold Junction Compensation:

The temperature reference circuit is shown in Figure 9.

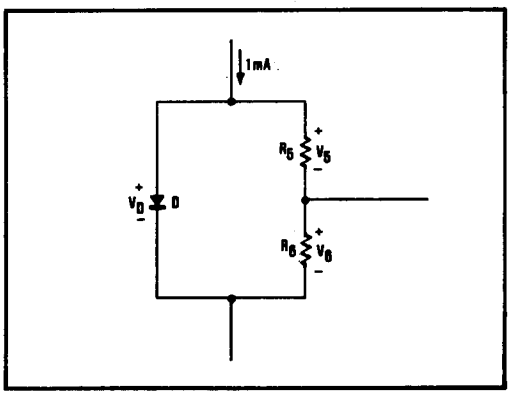


FIGURE 9. Cold Junction Compensation Circuit.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ell n \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = 25°C$, $V_D = 0.6V$ and $\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At 25°C this is approximately 52μV/°C (obtained from standard thermocouple table) therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right) \quad (2)$$

$$52\mu V/°C = 2000\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right)$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 14 and 15 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the +input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 16 should be used. When the TC opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR100 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltage (25μV max for the B grade, 50μV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 3 and 4. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommmended where possible and can be done by either one of two techniques shown in Figure 10. C_2 connect to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{1.59 \times 10}{(R_1 + R_2 + R_3 + R_4)(C_2 + 0.047\mu F)}$$

with f_{CO} in Hz, all R_S in Ω and C_2 in μF. This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1 will use smaller values of capacitance and is not a function of the input resistors. It is however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

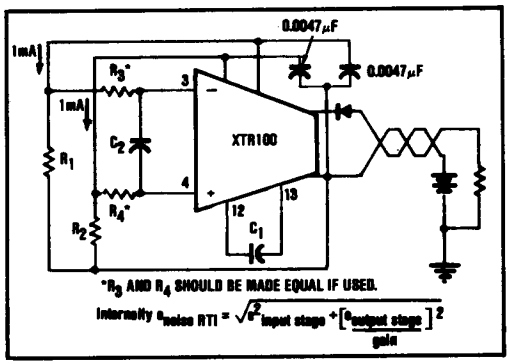


FIGURE 10. Optional Filtering.

APPLICATION CIRCUITS

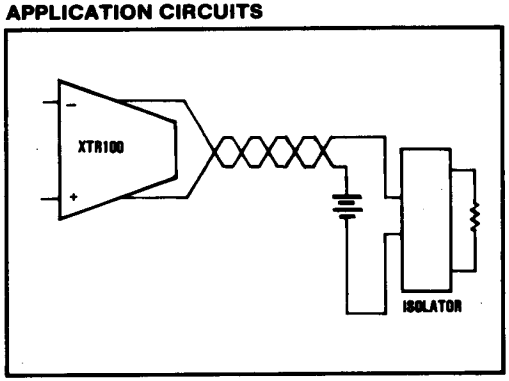


FIGURE 11. XTR100 with Loop-powered Isolation.

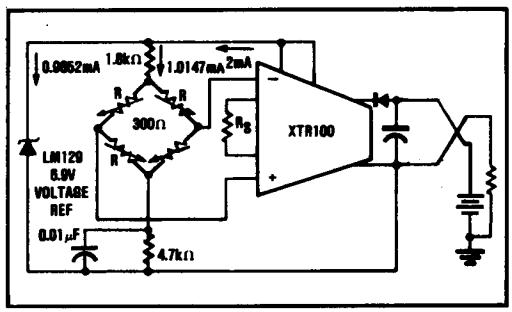


FIGURE 12. Bridge Input, Voltage Excitation.

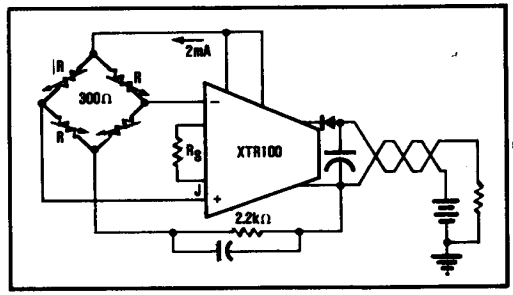


FIGURE 13. Bridge Input, Current Excitation.

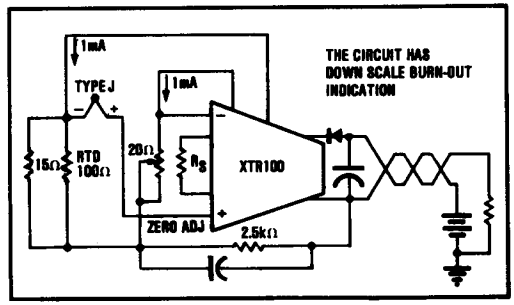


FIGURE 14. Thermocouple Input with RTD Cold Junction Compensation.

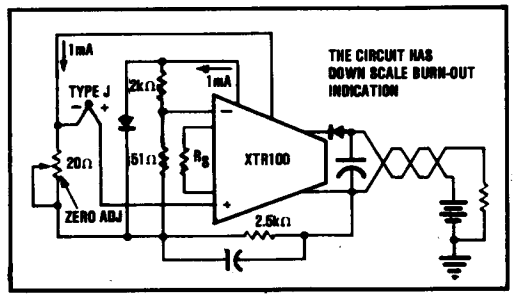


FIGURE 15. Thermocouple Input with Diode Cold Junction Compensation.

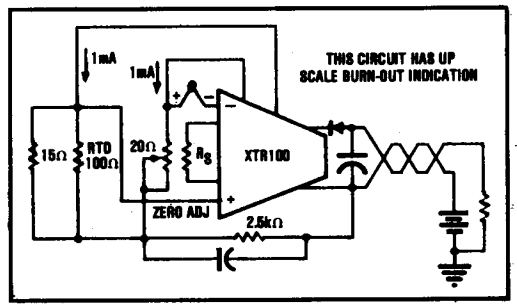


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

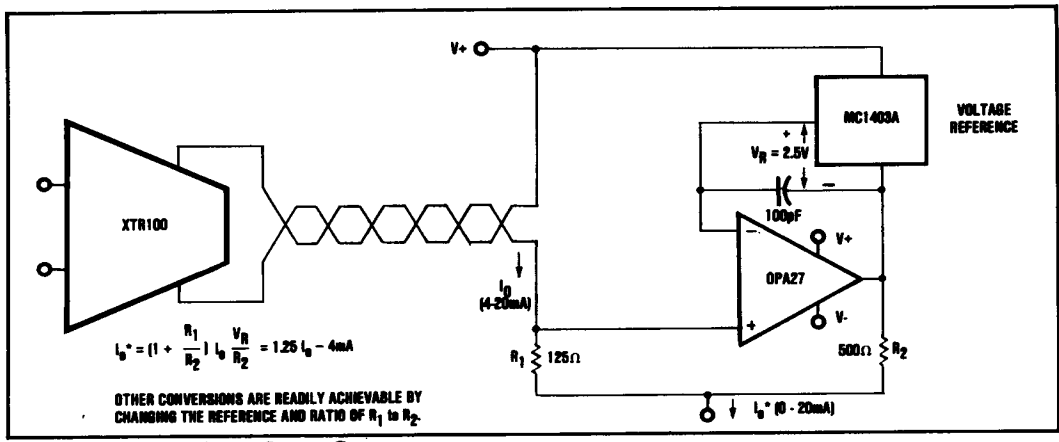


FIGURE 17. 0mA to 20mA Output Converter.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN} \quad (3)$$

K is the span (gain) term, (0.016mA/mV) + (40/R_S)

The nature of the XTR100 circuit is such that there are three major components of error

σ_O = error associated with the output stage.
σ_S = errors associated with span adjustment.
σ_I = errors associated with input stage.

The transfer function including these errors is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms (σ_S σ_I) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} + K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_S + K\ \sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR100 and the particular circuit in which it is applied. The circuit of Figure 7 will be used to illustrate the principles.

$$\sigma_O = Ios_{RTO} \quad (7)$$

Ios_{RTO}* = the output offset error current.

For the circuit of Figure 7,

$$\sigma_I = V_{OSI} + [I_{B1}\ R_T - I_{B2}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR} \quad (8)$$

The term in brackets maybe written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + Ios' R_4$.

V_{OSI}* = input offset voltage
I_{B1},* I_{B2}* = input bias current
I_{OSI}* = input offset current
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nomimal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio
$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
ϵ_{NONLIN}* = span nonlinearity
ϵ_{SPAN}* = span equation error. Untrimmed error = 3% max. May be trimmed to zero.

*Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

Given the circuit in Figure 7 with the XTR100B specifications and the following conditions: R_T = 109.4Ω at 25°C, R_T = 156.4Ω at 150°C, I_o = 4mA at 25°C, I_o = 20mA at 150°C, R_S = 123.3Ω, R_4 = 109Ω, R_L = 250Ω, R_{LINE} = 100Ω, V_{D1} = 0.6V, V_{PS} = 24V ±0.5%. Determine the % error at the upper and lower range values.

A. At the lower range value (T = 25°C).

$\sigma_O = Ios_{RTO} = \pm 4\mu A$

$$\sigma_I = V_{OSI} + [I_{B1}\ \Delta R + I_{OSI}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5}{CMRR}$$

$\Delta R = R_{T_{25°C}} - R_4 = 109.4 - 109 \approx 0$

$\Delta V_{CC} = 24 \times 0.005 + 4mA\ (250\Omega + 100\Omega) + 0.6V$
$= 120mV + 1400mV + 600mV = 2120mV$

$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$

$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$

$(e_1 + e_2)/2 - 5 \approx 0$

$PSRR = 3.16 \times 10^5$ for 110dB

$CMRR = 31.6 \times 10^3$ for 90dB

$$\sigma_I = 25\mu V + (150nA \times 0 + 30nA \times 109\Omega) \quad (9)$$

$$+ \frac{2120mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$$= 25\mu V + 3.27\mu V + 6.7\mu V + 0$$
$$= 34.97$$

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
$= 0.0001 + 0$ (assumes trim of R_S)
i_O error $= \sigma_O + K\,\sigma_I + K\,\sigma_S\,e_{IN}$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.341\,U$$

$e_{IN} = e_2 - V_4 = I_{REF1} R_{T_{25°C}} - I_{REF2} R_4$
since $R_{T\ 25°C} = R_4$
$e_{IN} = (I_{REF1} - I_{REF2}) R_4 = 0.1\mu A \times 109\Omega = 10.9\mu V$

Since the maximum mismatch of the current references is 0.01% of 1mA = 0.1μA

i_O error $= 4\mu A + (0.341\,U \times 34.97) + (0.341 \times 0.0001)$
$\times\ 10.9\mu V = 4\mu A + 11.89\mu A + 0.0004\mu A = 15.89\mu A$

$$\%\ \text{error} = \frac{15.89}{4mA} \times 100\% = 0.4\%$$ at lower range value.

B. At the upper range value (T = 150°C)

$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$
$\Delta V_{CC} = 24 \times 0.005 + 20mA\ (250\Omega + 100\Omega) + 0.6$
$= 7720mV$
$e_1 = 5.109V$
$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$
$(e_1\ e_2)/2 - 5V \approx 0$
$\Delta R = -R_{T\ 150°C} + R_4 = 156.4 - 109 = 47\Omega$
$\sigma_O = 4\mu A$
$\sigma_I = 25\mu V + (150nA \times 47\Omega + 30nA \times 109\Omega)$

$$+ \frac{7720mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$= 25\mu V + 10.33\mu V + 24\mu V$ F0 $= 59.33\mu V$
$\sigma_S = 0.0001$
$e_{IN} = e_2' - V_4 = I_{REF1} R_{T\ 150°C} - I_{REF2} R_4$
$= (1mA \times 156.4\Omega) - (1mA - 109\Omega)$
$= 47mV.$

$$i_{O\ ERROR} = \sigma_O + K\,\sigma_I + K\,\sigma_S \times e_{IN} \quad (10)$$
$$= 4\mu A + 0.341\,U \times 59.33\mu V + 0.341\,U \times$$
$$0.0001 \times 47000\mu V$$
$$= 4 \times 20.23 + 1.6 = 25.83\mu A$$

$$\%\ \text{error} = \frac{25.83\mu A}{20mA} \times 100\% = 0.13\%$$ at upper range value or % of FS.

CONCLUSIONS

From equation (9) it is observed that the predominant error term is the input offset voltage (25μV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 3 and 4. From equation (10), the predominant errors are $I_{OS\ RTI}$ (4μA), $V_{OS\ RTI}$ (25μV), and I_B (150nA), max, B grade.

A NOTE FOR HIGH GAIN APPLICATIONS

In applications where e_{in} full scale is small (<50mV) and R_{span} is small (<≈150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

In such applications, be sure to include the effect of the normal thermal feedback within the XTR100 package. Small additional errors occur from a change in input offset voltage and current due to a change in chip temperature resulting from a change in output current (4mA up to 20mA).

The XTR100 has two thermal resistance specifications:

$\theta_{JA} = 115°C$

This is the thermal resistance from output transistor to ambient. It is used for normal power dissipation considerations (see Figure 18).

$\theta_{JI} = 60°C/W$

This is the thermal resistance which describes the effect of output stage power dissipation in input stage temperature rise.

As an example of how θ_{JI} would be applied, we will calculate the limits with $V_{PS} = 40V$ and $R_L = 250\Omega$.

Power Dissipation:

at 20mA output: 20mA [40V−(20mA × 250Ω)] = 700mW
at 4mA output: 4mA [40V−(4mA × 250Ω)] = 156mW

Thermal Resistance: $\theta_{JI} = 60°C/W$

Input Stage Temperature Rise:

at 20mA output: 700mW × 60°C/W = 42°C
at 4mA output: 156mW × 60°C/W = 9.4°C

Thus under these conditions when the output changes from 4mA to 20mA the input stage temperature changes 42°C − 9.4°C = 32.6°C. The maximum input stage offset change will depend on the particular grade specification:

A Grade (1μV/°C max) = 32.6μV
B Grade (0.5μV/°C max) = 16.3μV

The amount of error that this offset voltage represents depends on how large the full scale input voltage is. It is worse, of course, for small input voltages. Table I shows the error as a percentage of full scale and in terms of output current (% FS error × 16mA FS output span).

TABLE I. Maximum Errors Due to Thermal Feedback
$V_{PS} = 40V$, $R_L = 250\Omega$.

	10mV FS	100mV FS	1V FS
A Grade	0.326% (52.2μA)	0.0326% (5.22μA)	0.0033% (0.522μA)
B Grade	0.163% (26.1μA)	0.0163% (2.61μA)	0.0016% (0.261μA)

HOW TO REDUCE ERRORS

Lower V_{PS}

The errors can be reduced by lowering the voltage at the XTR100 line terminals. The errors in the example above represent a fairly demanding condition of maximum voltage ($V_{PS} = 40V$) and minimum resistance ($R_L = 250\Omega$). If the voltage is lowered to 24V, then a 4mA to 20mA output change causes a change in input stage temperature of 17.3°C and the errors in Table I are reduced by a factor of 17.3°C/32.6°C = 0.53. (Note that this is different than the decrease in the voltage itself: 24/40 = 0.6.)

Raise Resistance

If the load or line resistance is raised the output power dissipation will also be reduced. If $R_L = 400\Omega$ (400/250 = 1.6), the change in output temperature is 29.2°C as the output changes from 4mA to 20mA (still with V_{PS} = 40V) and the errors in Table I are reduced by a factor of 29.2°C/32.6°C = 0.9.

Heat Sink

Heat sinking the package will reduce both θ_{JA} and θ_{J1}. The following is information on small-finned heat sinks that are attached with an epoxy heat sink adhesive (AHAM-985). The three models are 0.75" × 0.4" × 0.21".

Model 141
AHAM
27901 Front St.
Rancho, CA 92390
(714) 676-4151

Models 141 and 142
Heat Sink Plus
28715 Via Montezuma
Temecula, CA 92390
(714) 676-3031

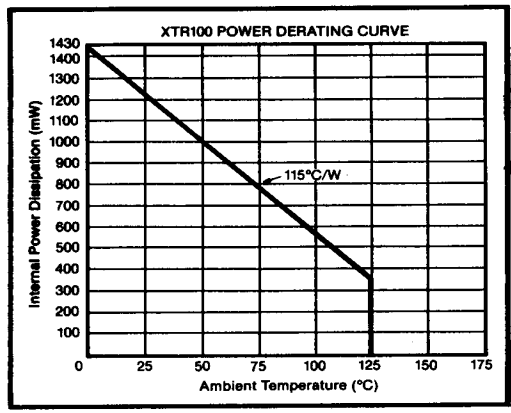


FIGURE 18. Power Derating Curve.

GENERAL RECOMMENDATIONS HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).