AN1231
APPLICATION NOTE

VIPower: VIPer50
FOR USB SELF-POWERED HUB

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1 SCOPE

This document presents the results obtained from a USB off-line power supply designed with VIPer50.

This design is a complete solution for powering Self-powered 4-ports hubs.

It supplies the USB HUB-controller by delivering up to 15W (this is more than enough to meet the USB requirements), 500mA each port. In the case that a 3.3V is needed, a voltage regulator can be added.

2 SCHEMATIC

The USB power supply is based on the standard schematic RCD-snubber-TL431 suggested in the VIPer software.

The complete schematic is shown in figure 1.

This circuit operates from 85Vac to 275Vac, with an output current, on 5V, varying from 20mA to 3A.

The working frequency has been set to about 50KHz (47.6KHz) using R1=5.1KΩ and C5=8.2nF.
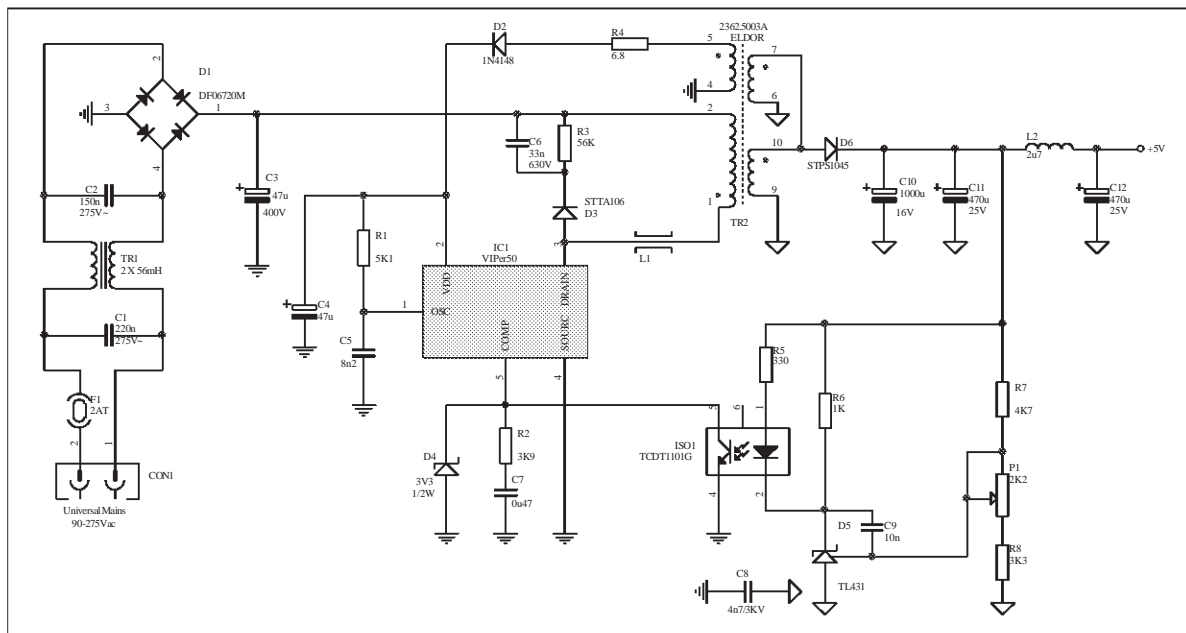
The potentiometer P1 could be removed, if output adjustment is not necessary to compensate voltage drops on the following stages (mainly on Power Distributors).

By removing P1 the value of R8 becomes the same of R7 (4K7) and a short-circuit must be placed between the ends of P1.

3.0 MEASUREMENTS

Unless otherwise noted, all measurements have been made with a high voltage DC source, ranging from 100V to 400V. This corresponds to an AC input voltage from 85Vac (considering the voltage ripple of the bulk capacitor) to 280Vac.

Figure 1: Schematic diagram

3.1 EFFICIENCY

Figure 2 gives the system efficiency measured for different output currents at 4 different values of input voltage. Figure 3 reports in detail the efficiency for low output current up to 150mA.
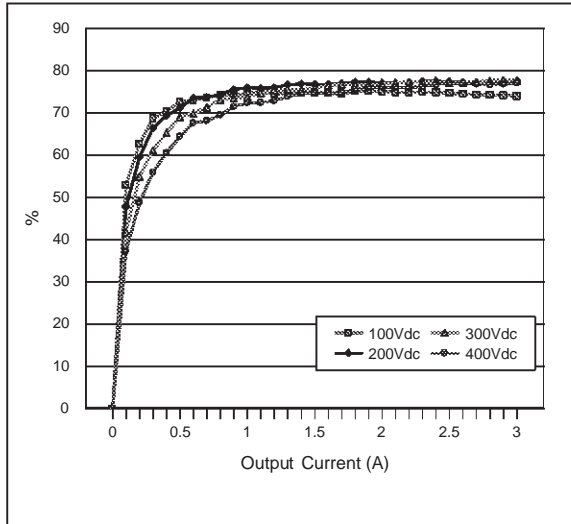
Figure 2: Efficiency
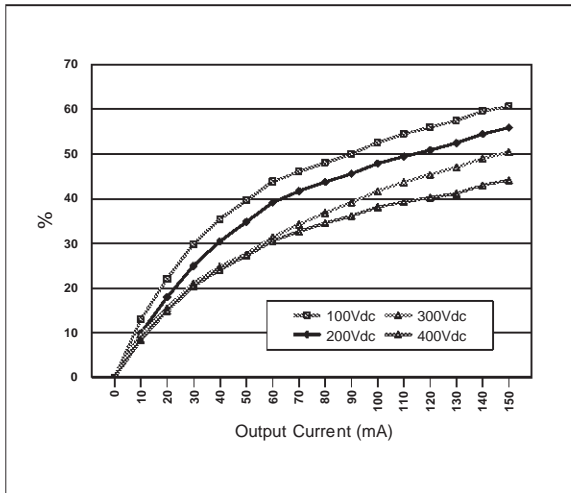

Figure 3: Efficiency at low current

Table 1: Numerical Values

| Input Voltage	Efficiency at 20mA	Efficiency at 1.5A	Efficiency at 3A
100V	22%	75%	74%
200V	18%	77%	77%
300V	16%	76%	77%
400V	15%	74%	77%

The behaviour of the previous curves gives the idea that the switching losses are preponderant versus conduction losses at a very low output current.

Using the mathematic capability of scope, it is possible to make an estimation of power losses. The measures have been done at 400Vdc and full load:

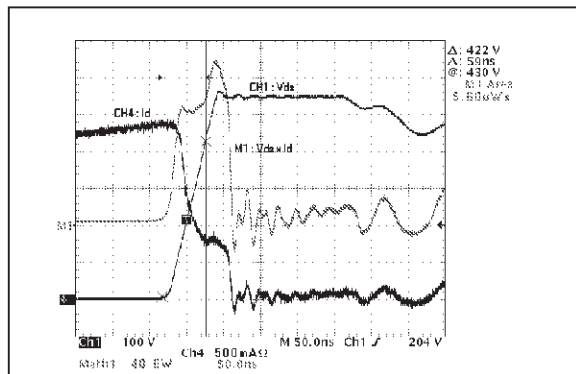Turn on losses:

$$P_{ON} = 3.92\mu J \cdot 47.6KHz = 0.186W$$

Figure 4: Turn on losses
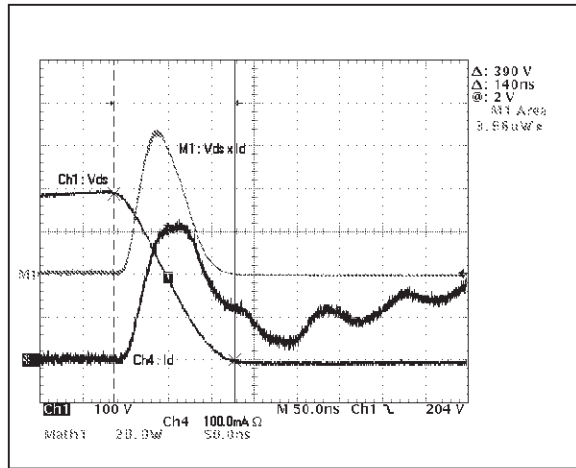
Turn off losses:
$$P_{OFF} = 5.60\mu J \cdot 47.6Hz = 0.266W$$

Figure 5: Turn off losses

Note that the right cursor has been set at about the same value as the turn on voltage.

This assumes that nothing is dissipated at turn off, because the cross over time is only due to charge of the drain capacitance and the internal turn off of the power MOSFET is sufficiently fast. The corresponding energy of this capacitor is dissipated at turn on, and this explains that only the part of voltage which is discharged at turn on is taken into account at turn off.

The conduction losses can be estimated as follows:

$$P_{CD} = t_{ON}/t_{SW} \cdot R_{dson} \cdot I_p^2/3 = 0.146W$$

Also the power dissipated by signal part and biasing resistor have to be considered (refer to AN947 for a deeper analysis) in order to have the complete power dissipated by VIPer50

Table 2. VIPer50 Power Dissipation

Parameter	Value
P_{ON}	0.186W
P_{OFF}	0.266W
P_{CD}	0.146W
P_{bias}	0.140W
P_{dd}	0.120W
P_{tot}	0.858W

The measured case temperature was 70.5°C for an ambient temperature of 23°C. This correspond to a dissipated power of about 0.8W with a thermal resistance of 60°C/W (free air, no heatsink) well in accordance with the above calculated losses.

The STPS1045 conduction power losses were calculated using the formula reported on the datasheet:

$$P = 0.42 \cdot I_{F(AV)} + 0.015 \cdot I_F^2{}_{(RMS)} = 1.53W$$

where, in the case of triangular waveform:

$$I_{F(AV)} = I_M \cdot \delta / 2$$

$$I_F^2{}_{(RMS)} = I_M^2 \cdot \delta / 3$$

The power losses in the diode are double than those in the VIPer50. Considering an ambient

temperature of 70°C and a thermal resistance of 60°C/W in free air the VIPer can work without any heatsink (T_{jmax} = 120°C), while for the diode the heatsink is required.

3.2 BURST MODE

When the output current is too low, the minimum duty-cycle fixed by the internal blanking time of the device is too high to control the output voltage. In such a case, the burst mode operation takes place automatically, thanks to the VIPer50 ability to maintain its power switch in the off state when the voltage on the compensation pin goes below 0.5V.

Figure 6: Good burst mode
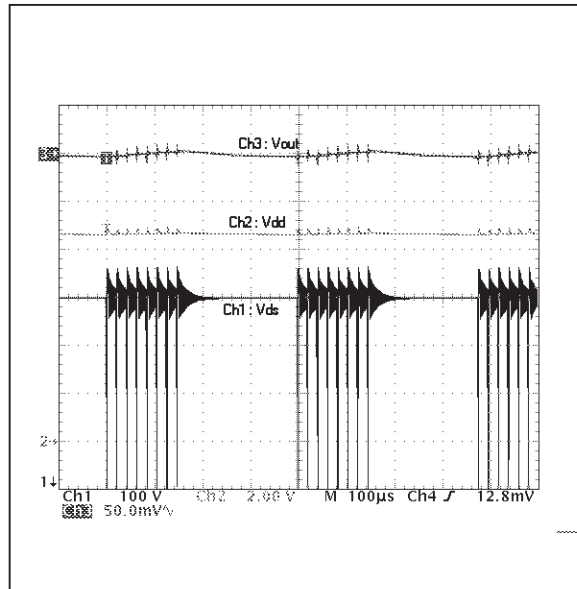
This results in missing cycles, as shown on the scope waveforms reported in figure 6 (Vin=400Vdc, Iout=30mA).

The burst mode has a recurring period of about 400µs, and 8 switching cycles take place each time. The output ripple is about 10mV and the Vdd voltage is stable, just above the low threshold voltage (8V) of the internal UVLO logic. This threshold can be reached by further reducing the output current, because it also reduces the Vdd voltage on the primary side (less and less energy from the auxiliary winding). When this occurs, another type of burst mode appears, which is controlled by the

Vdd voltage. This is called the "bad" burst mode. The following scope waveforms show what happens in this case (Vin=400Vdc, Iout=10mA).

Figure 7: Bad burst mode
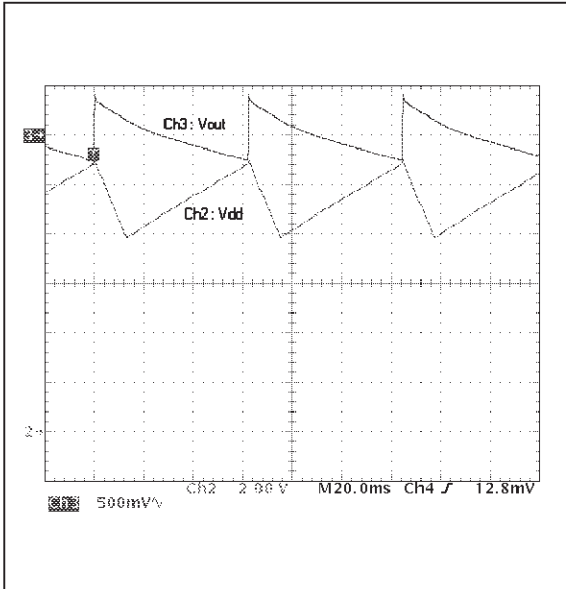
Each time that the Vdd voltage reaches the low threshold voltage of the UVLO logic the device is reset and the Vdd capacitor is charged back to the high threshold of the UVLO logic thanks to the start up current source that is turned on. The recurring period of this phenomenon is about 60ms. This behavior leads to the following drawbacks:

1. Since the start up current source is activated to supply the device from the high voltage rail, the efficiency decreases dramatically.

2. The recurring period is very high, leading to a large output ripple. In the above example, this ripple is about 700mV, which is not acceptable for an output voltage of 5V.

3. This mode has very poor dynamic behavior in the case of output current variation. If an increase of output current occurs during the recharging phase, the output capacitor will be discharged down to 0V and the normal output voltage will return only at the next starting phase.

In conclusion, the good burst mode has to be extended in the low output power range as much as possible, mainly optimizing the transformer.
The bad burst mode occupies a very low range of output current, in which the power supply doesn't have its nominal performance. But the output voltage is still under control (no overpassing the nominal voltage), and no stress is applied to the power supply.
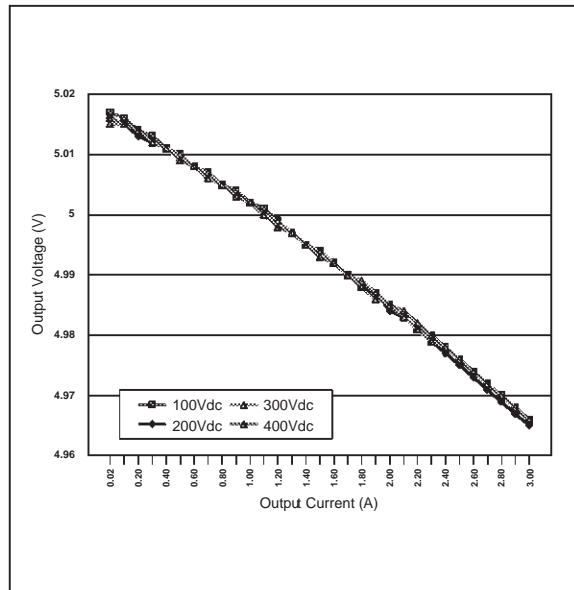
3.3. LOAD REGULATION

3.3.1. STATIC REGULATION
Figure 8 shows the output regulation for an output current ranging from 20mA to 3A.

The four curves have been done at different input voltages.

Figure 8: Static load regulation

The voltage drops from 20mA to 3A is about 50mV, this is mainly due to the resistance of the inductance (~20mΩ) used in the output filter.
Connecting the resistive bridge on TL431 after the output inductor the 50mV drop in load regulation will be avoided. We prefer to leave the feedback connected after the diode, because in some real applications the inductance is not present, or the

LC filter (L2, C12) is split and dedicated for each downstream port.

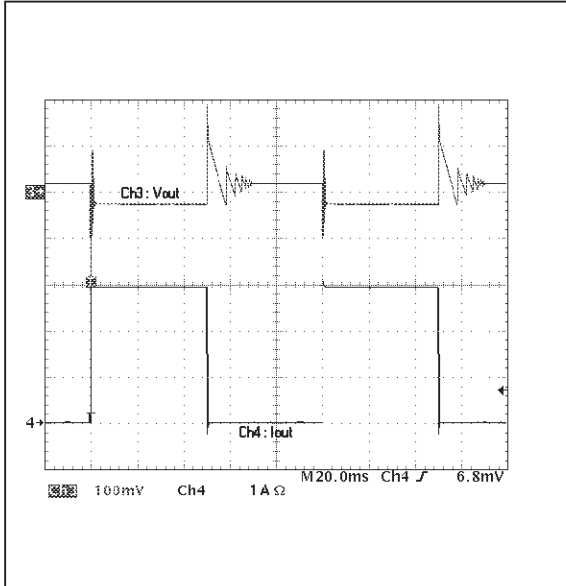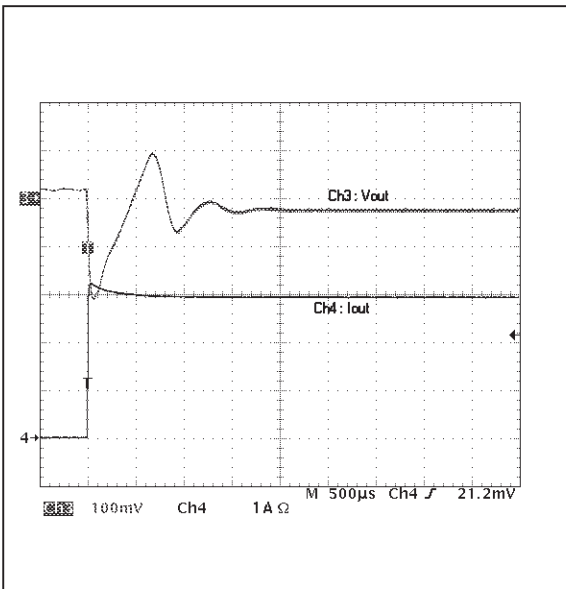**Figure 9: Dynamic behaviour for 0.66% to 100% of full load**

Figure 10: Dynamic behavior for 0.66% to 100% of full load

3.3.2. DYNAMIC REGULATION

The output current has been modulated by a square wave, from minimum load (20mA) to full load (3A), from minimum load to 50%, and from 50% to full load with an input voltage of 300Vdc.
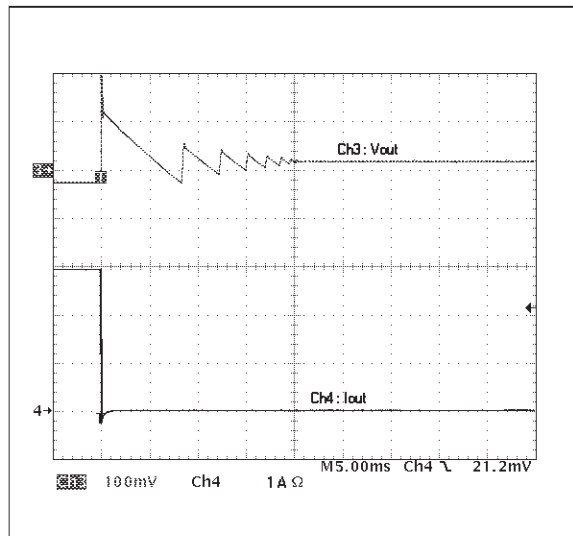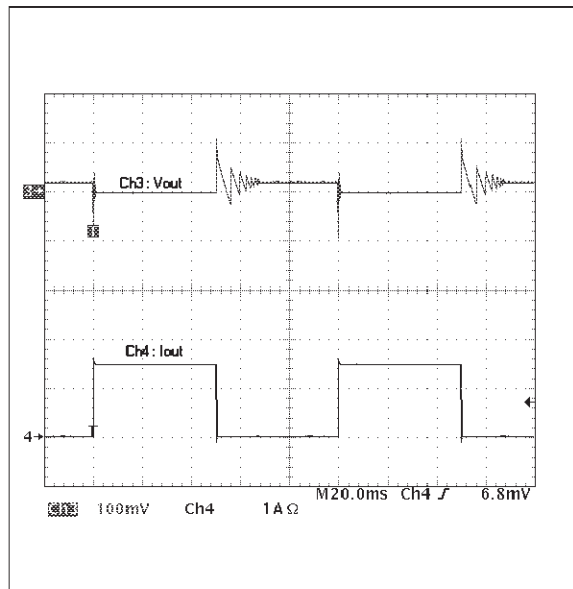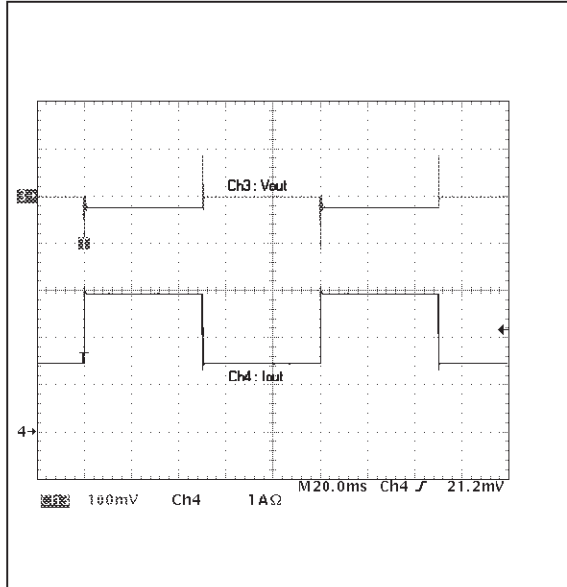
Figure 11: Dynamic behavior for 100% to 0.66% of full load

Figure 12: Dynamic behavior for 0.66% to 50% of full load

Figure 13: Dynamic behavior for 50% to 100% of full load

Ch3 : Vout

Ch4 : Iout

4→

100mV   Ch4   1AΩ   M20.0ms Ch4 ƒ 21.2mV

3.4. LINE REGULATION & SWITCHING NOISE

The power supply has been connected to 85Vac/ 50Hz main lines (worst case, not even real) to measure the line rejection on the output. Both the input voltage and the output voltage are reported in figure 14, with a full load operation.

Figure 14: Dynamic Line Regulation at 100Hz

C3 Pk–Pk
2.6mV

Ch3 : Vout

3→

C2 Pk–Pk
33.0 V

Ch2 : Vin

Ch3 10.0mVΩ   1=.0 V   M2.00ms Ch3 ƒ 400mV
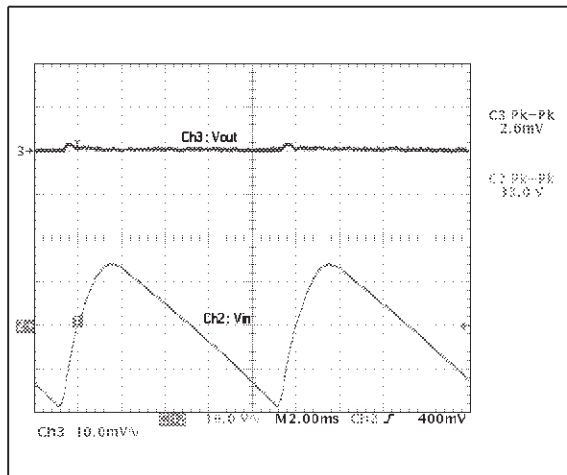
Thanks to the excellent input voltage disturbances rejection of the device, the 100Hz output ripple is 2.6mV against the 33V ripple on the bulk capacitor (-82dB).

The internal current control loop takes care of a good part of the input voltage variation, and the outer voltage loop makes the final improvements, thus reducing the output voltage variation to such levels.

Figure 15 shows the switching noise, at 47.6KHz, on the output. The waveform is related to 220Vac and an output current of 3A.
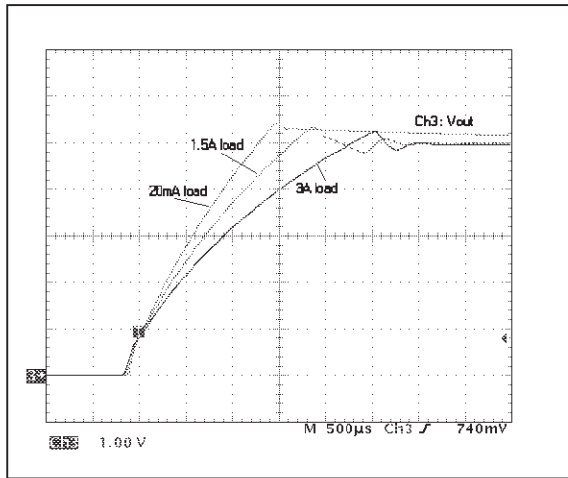
Figure 15: Switching Noise

C3 Pk–Pk
59.6mV

Ch3 : Vout

20.0mVΩ   M 20.0µs Ch3 ƒ 10.4mV
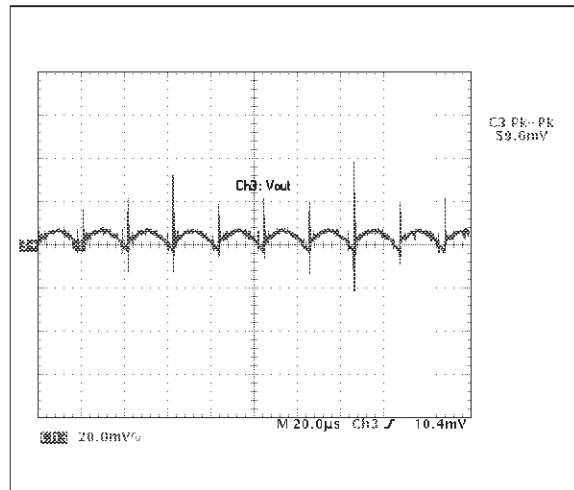
3.5. TURN ON

The input voltage of 300Vdc has suddenly been applied to the power supply, and the output voltage monitored for different load conditions. The results are reported in figure 16. The starting slope is due to the value of C7 which defines the soft start time of the power supply. This time can be adjusted by choosing the value of this capacitor, but take care that this capacitor enter also in the loop calculation. The value of C4 must be changed accordingly in order to maintain the Vdd voltage at a sufficient level during this soft start time.

Figure 16: Start up waveforms

Figure 18: Start up time at different Vin

The start up time has also been measured using mains. This is given in figure 17, where all the input, Vdd and output voltages are given at start up, for a full load condition. Different input voltage does not affect the start up time, because it is due to an internal current generator that charges C4. The device starts to work when the Vdd reaches 11V, as shown in figure 18 for 85Vac and 275Vac.

Figure 17: Start up time

3.6. TURN OFF

The behavior of the power supply at turn off is reported in figures 19 and 20, for both the output and input voltages. It can be seen that the output voltage decreases in a monotone way, with no restart after it reaches the zero level.

Figure 19: Turn off at 20mA load
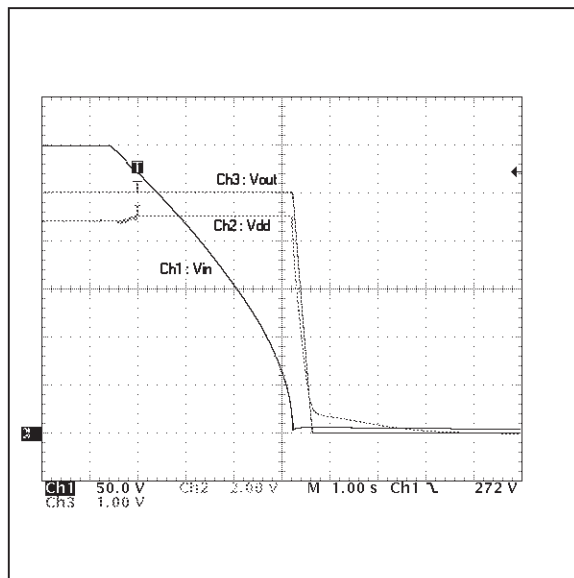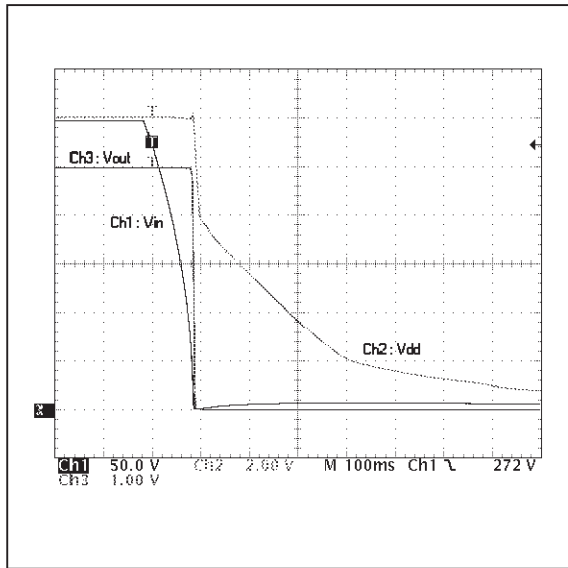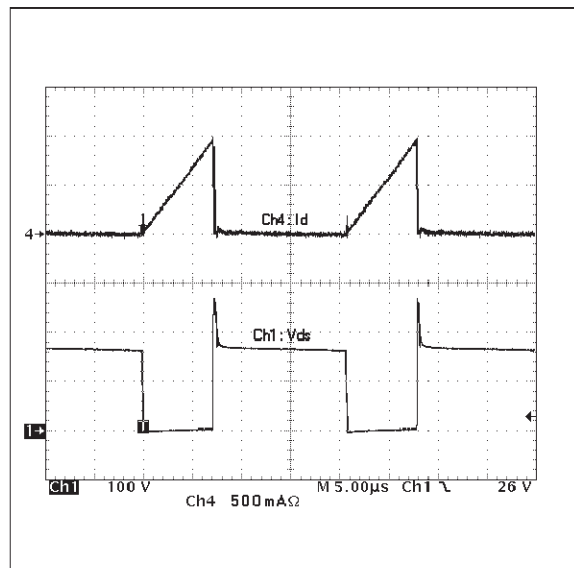
Figure 20: Turn off at 3A load

Figure 22: Normal operation 85Vac, 3A

3.7. NORMAL OPERATION

The following figures show the voltage and current on the Drain pin at different working conditions. With 85Vac as the input voltage and 3A as the load, the power supply is at the limit of continuous mode, but this is not a problem for the IC.
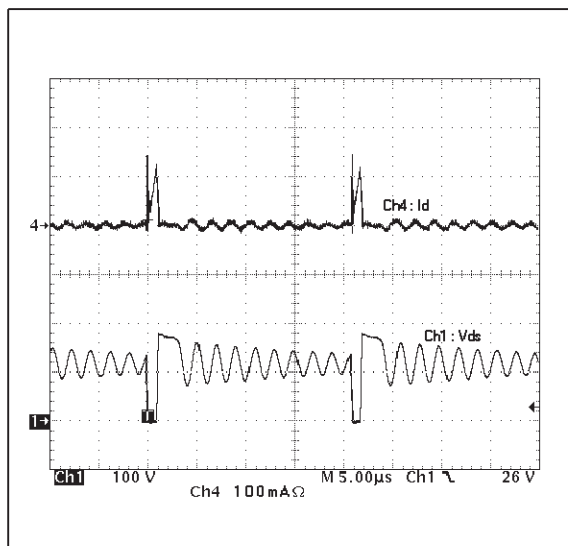
Figure 21: Normal operation 85Vac, 20mA
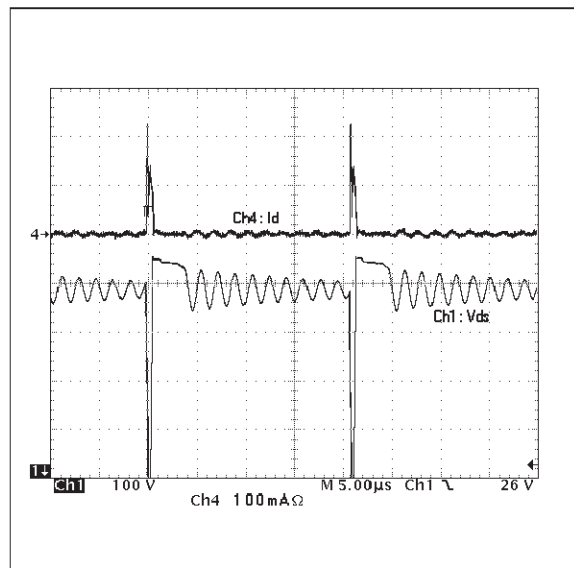

Figure 23: Normal operation 275Vac, 20mA

Figure 24: Normal operation 275Vac, 20mA
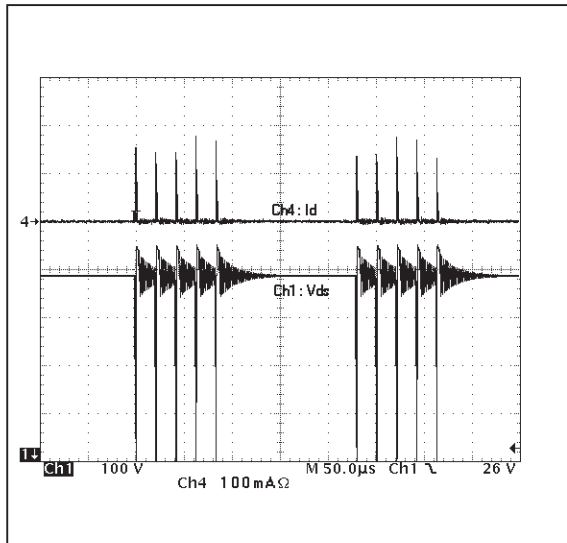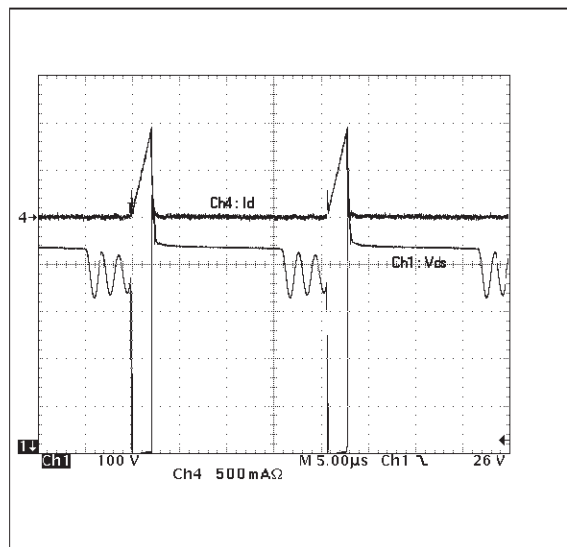

Figure 25: Normal operation 275Vac, 3A

3.8. OVERLOAD

When the output current exceeds a certain value the Vdd reaches 13V, the VIPer50 automatically passes into primary mode regulation. In the case that the overload increases together with limiting the current flowing inside the IC by the zener diode on the Comp pin, the output voltage decreases to maintain Vdd at 13V.

Figure 26: Overload
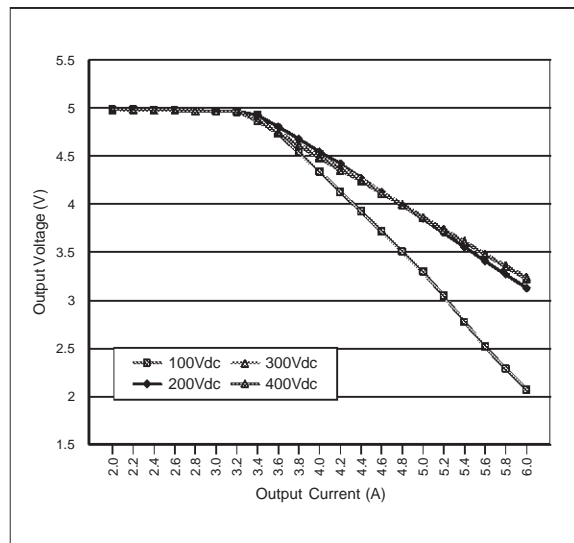
The output voltage at 100Vdc decreases quickly because the system is in continuous mode.

4. IMPROVEMENTS

Some modifications have been done on the design of Figure 1 in order to improve the behavior of the power supply.

In a real application where there are some protection devices between the output of the power supply and the downstream ports, user accessible, a short circuit will never be seen by the power supply, unless this happen due to a failure of the USB Hub control circuit/device.

4.1. SHORT CIRCUIT BEHAVIOR

With 400Vdc input voltage, a short circuit has been made on the output of the power supply. This results in a permanent average current of about 11A, well above the transformer capability. Figure 27 and 28 show Iout and Idiode in this condition.

The VIPer50 is controlled only by Thermal Protection, when the internal temperature overcomes the Ttds (see the datasheet) the device stops working.
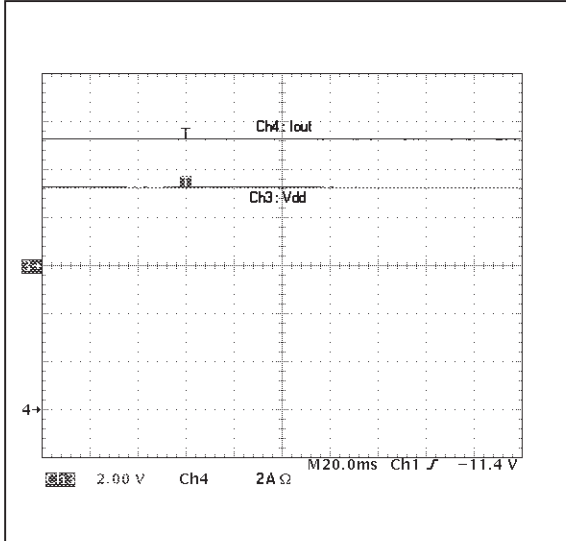
Figure 27: Vdd and Iout in short circuit
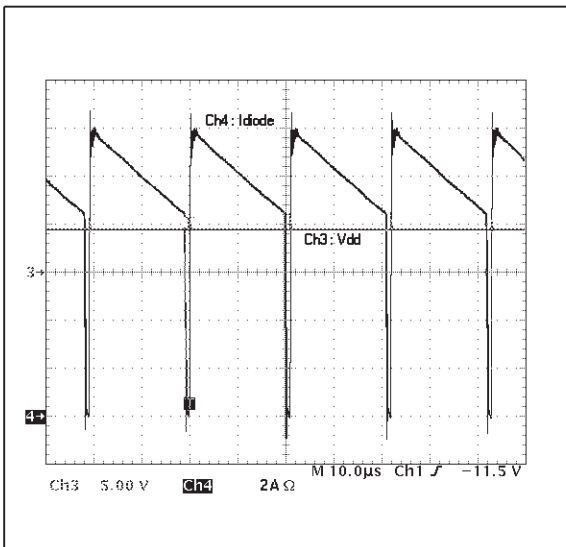

Figure 28: Vdd and Idiode in short circuit

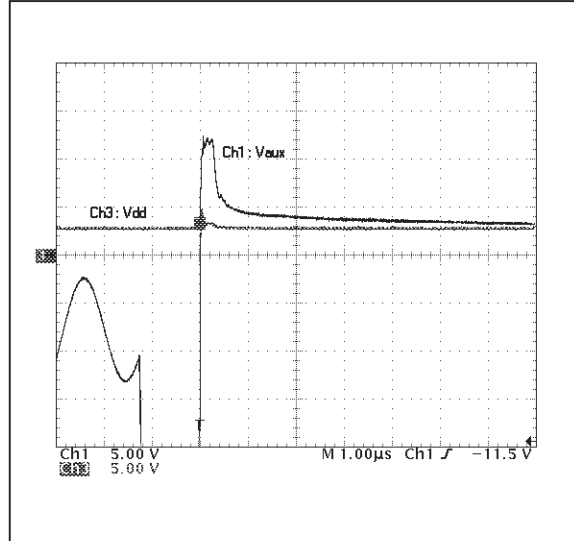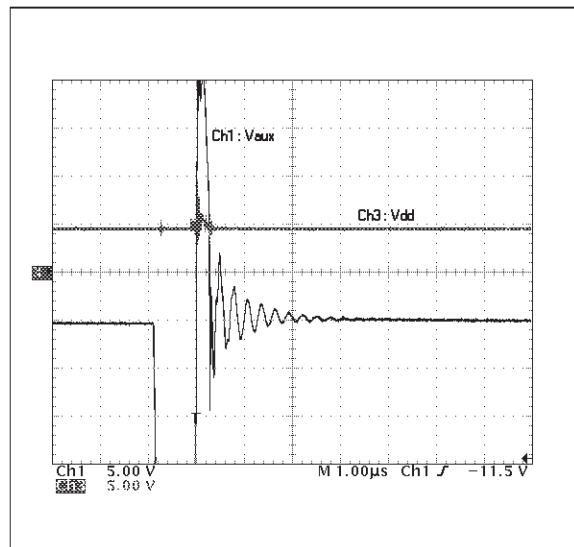**Figure 29: Vdd, Vaux in normal operation**


Figure 30: Vdd, Vaux in short circuit

The protection which is foreseen for the VIPer50 consists of the monitoring of the Vdd voltage and the switching off of the device when this voltage is below the low threshold voltage (8V) of the UVLO logic. This is done naturally when the output voltage is low (i.e. in short circuit), because the auxiliary winding is delivering a Vdd voltage which is proportional to the output voltage.

Unfortunately, the transformer delivers some voltage spikes at switch off on the auxiliary winding, as shown in figure 29 and 30.

This spike is sufficient to maintain a correct supply voltage to the device, and even to increase its voltage up to the internal reference (13V) where the device decreases the peak current. Actually the device is regulating its primary Vdd voltage through the auxiliary winding spike.

A solution to get rid of these spikes is to implement a filter just by increasing R4. But this leads to poor performances in regulation, especially for light loads, where the bad burst mode will appear for a higher output current than now.

Another solution consists of using an active switch instead of the R4. Figure 31 presents a possible schematic with the addition of two more components, compared with the former one.

Figure 31. Possible short circuit protection
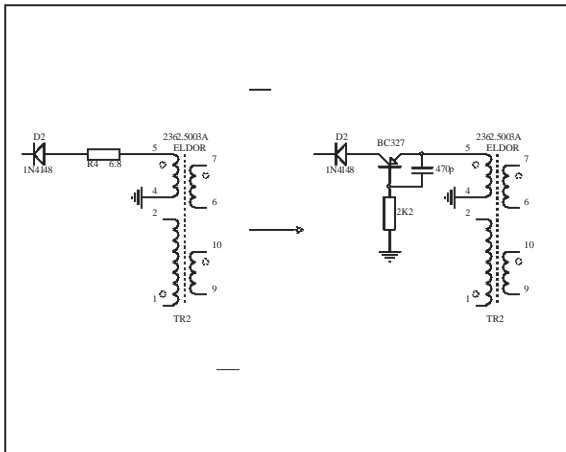
A bipolar transistor is inserted in series with the auxiliary winding and it is driven through an RC network. The RC delays the transistor turn on when the auxiliary winding begins to deliver positive voltage, thus skipping the first spikes, as shown in the following figures.

Therefore, the Vdd is more representative of what happens on the secondary side.

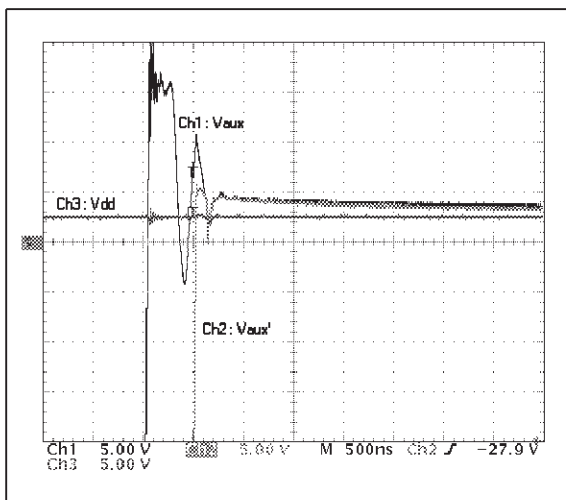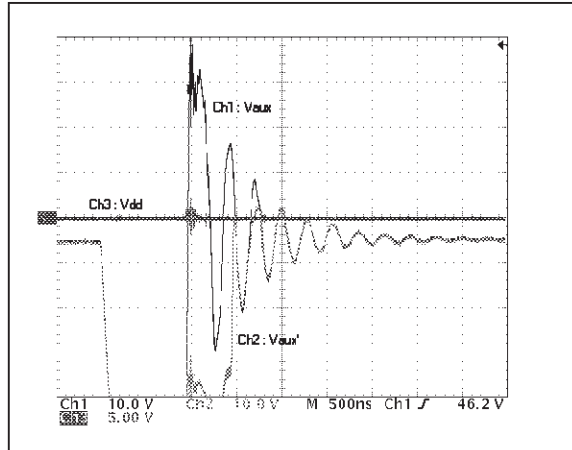**Figure 32: Vdd, Vaux and Vaux' in normal operation**

Figure 33: Vdd, Vaux and Vaux' in short circuit

Note that R4 was doing the same thing, but in a less efficient way. In normal mode, this resistor avoids excessive Vdd voltage, which should reach the internal reference voltage (13V) and interferes with the secondary feedback. With new design, it is possible to eliminate this resistor, and even to add a couple of turns on the auxiliary winding.

As a result, the short circuit current is no more limited by the Vdd voltage and it increases because the VIPer50 is internally limited to 2A, which is double of what needed for full load. The Zener diode D4 acts as clamper limiting the max peak current to a more reasonable level (about 1.25A), this avoids the transformer core saturation also during the start up.

Figure 34 gives the output short circuit current, using the above mentioned circuit the average output current is about 2A. This current is more acceptable than the previous one, and it appears that the converter is able to withstand indefinitely the short circuit condition.

Figure 34: Vdd and Iout in short circuit with improvements
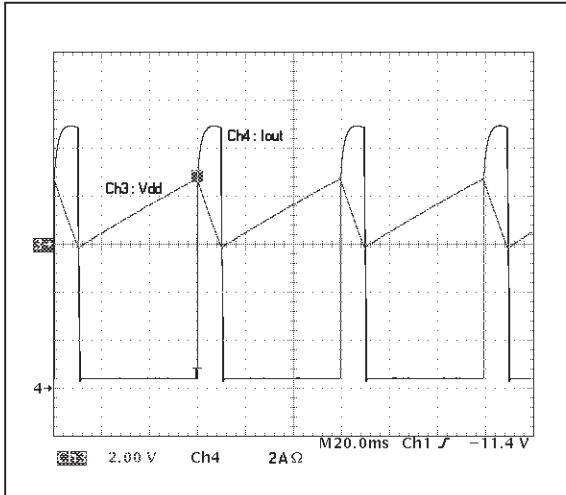
5. CONCLUSION

It appears that the VIPer50 is well suited for such applications in which the output power ranges from hundreds of milli Watts to a few dozen of Watts.

The most interesting points are:

1. The automatic burst mode which is implemented through an internal comparator on the compensation pin. This feature allows the control of very low load, by still maintaining a good efficiency, or offering very low input power for zero load operation. From this point of view, the transformer design is very important, but the present note shows the good behavior of standard transformers.

2. In the case that the transformer doesn't demonstrate a good behavior in short circuit or shows an early intervention of primary regulation, a simple circuit (one general purpose PNP bipolar transistor, one small capacitor and one resistor) greatly improves the performances of the whole power supply.

ANNEX 1

Component List

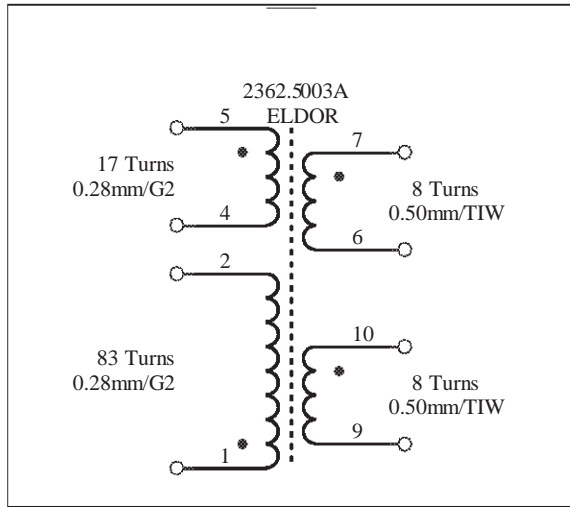| Reference	Value	Part Number	Note
CON1	2 Pins connector		
C1	220n/275Vac		
C10	1000u/16V	FA Series	Panasonic
C11	470u/25V	FA Series	Panasonic
C12	470u/25V	HFZ Series	Panasonic
C2	150n/275Vac		
C3	47u/400V	B43503 Series	Siemens
C4	47u		
C5	8n2		
C6	33n/630V		
C7	0u47		
C8	4n7/3KV		Murata
C9	10n		
D1	Bridge	DF06720M	
D2	1N4148		
D3	600V-1A Turbo	STTA106	STMicroelectronics
D4	3V3 - 1/2W		
D5	Adj. Shunt reg.	TL431	STMicroelectronics
D6	45V-10A Schttky	STPS1045	STMicroelectronics
F1	2.0AT-250Vac		
IC1		VIPer50	STMicroelectronics
ISO1	Optocoupler	TCDT1101G	Temic
L2	2u2	ELC08D2R7E	Panasonic
P1	2K2		
R1	5K1		
R2	3K9		
R3	56K - 1W		
R4	6.8		
R5	330		
R6	1K		
R7	4K7		
R8	3K3		
TR1	2 X 56mH	42H270500	RADIOHM
TR2	15W Transformer	2362.5003A	ELDOR

Annex 2   **Mechanical drawings**
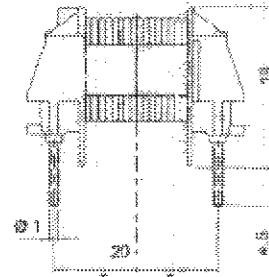
Transformer specification

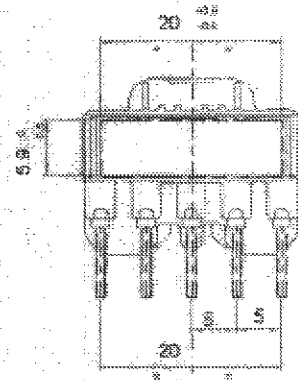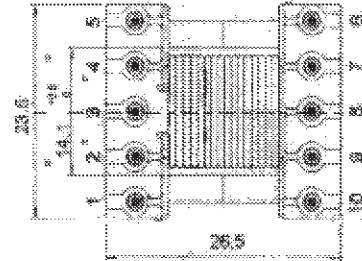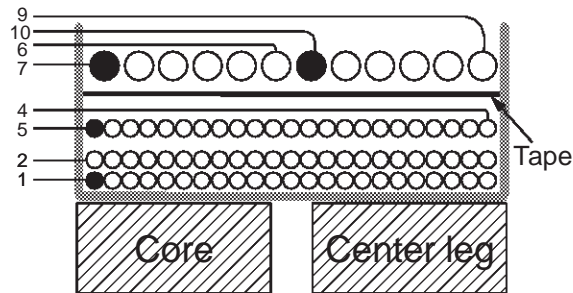Primary inductance   : 0.82 mH
Primary leakage inductance : 30µH (max)

CORE   : E20-10-6
Material   : N27
Gap   : 0.4mm

Transformer diagram

2362.5003A
ELDOR

5
17 Turns
0.28mm/G2
4

7
8 Turns
0.50mm/TIW
6

2
83 Turns
0.28mm/G2

10
8 Turns
0.50mm/TIW
9

1

Windings

9
10
6
7

4
5

2
1

Tape

Core   Center leg

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