USH5053 HIVIC

450 VOLT PIN DRIVER

UNIVERSAL SEMICONDUCTOR

T-52-13-90

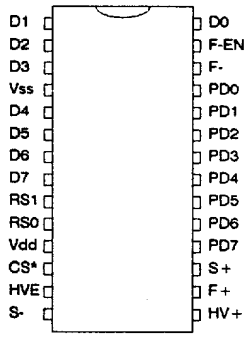
FEATURES

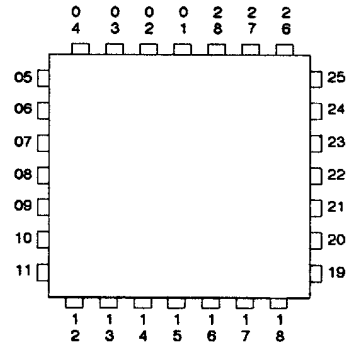
* Immunity to Latch-up
* Integrated Pin Drivers
* On-chip CMOS control logic
* Bi-directional Sensing
* Internal Level Shifters
* uP Bus Compatible
* Push-Pull Driver
* Kelvin Sensing
* Low Leakage
* Dielectric Isolated Process

DESCRIPTION

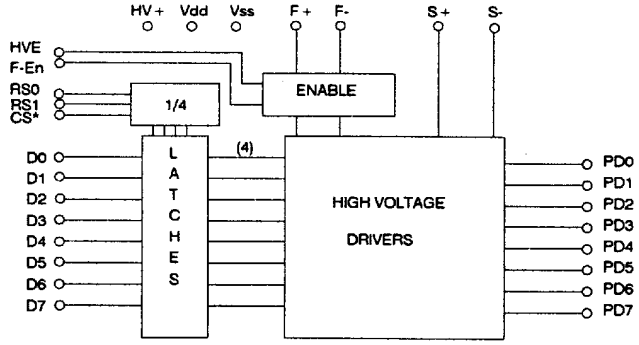
The USH5053 is Universal's High Voltage Integrated Circuit (HIVIC) that incorporates on the same HIVIC, 8 independent channels of high voltage switching and low voltage CMOS logic to interface to a microprocessor bus for switch control. This chip is designed for those applications where 450 volt testing or signal switching is needed. Each channel has 450V dielectrically isolated DMOS FETs that connect the pad to either a positive rail, a low drive rail, a high sense rail, or a low sense rail. The configuration allows push-pull drive and/or remote Kelvin sensing.

Pin Configuration





Block Diagram



1925 Zanker Road, San Jose, CA 95112 * PH (408)436-1906 * FAX (408)436-1125 * TWX 910-338-7617

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Pin Description

D 0-7	Data to be sent into the three banks of eight latches used to control the high voltage drivers.
RS 0-1	Selects the active bank of latches for data storage and reset.
CS*	Active low chip strobe that will clock the data into the set of latches selected by RS 0-1 (see Register Selection Table). This signal must be a clocked chip enable for the device. When RS 0-1 are in the 10 state & CS* is clocked, the Force latches will assume the state of the data lines D 0-7. With the RS 0-1 lines in the 01 state, CS* will clock the data into the 01 state, CS* will clock data into the Sense latches. State 11 of the RS 0-1 lines will clock data into the polarity latches. State 00 of the RS lines will reset all three sets of latches on the CS* strobe.
HVE	Enable signal to the F+com transistor that will select the device during the application of high voltage to the system. Only those devices placing high voltage onto the test board should have HVE active.
F-EN	Control similar to the HVE signal except it is for a transistor common to the F- line.
HV+	Voltage for the level shift circuits. It must be 15 to 20 volts more positive than the F+ forcing voltage.
F+	Test voltage programmed onto the board under test, minus any drops in the chip.
F-	Return for the F+ line and should be programmed to the other side of the resistance under test.
S+, S-	Sensing lines used for Kelvin measurements for continuity tests or low value resistance tests.
Vdd	+10V logic supply pin.
Vss	Ground reference pin for both the logic and high voltage control supply HV+.
PD 0-7	Eight high voltage pin driver/sense lines.

ABSOLUTE MAXIMUM RANGES

LEVEL	PARAMETER	SYMBOL	RATING	UNIT
High Voltage	Continuous Drain Current	ID	50	mA
	(output devices F+, F-)		-	V
	+HV, F+, PD 0-7	BV	450	V
	Pulsed Drain Current (100us)	IDp	100	mA
CMOS Control	DC Supply Voltage	Vdd	-0.5 to 15	VDC
	DC Input Voltage	Vin	-0.5 to Vdd +.5	VDC
	DC Input Current	Iin	+/-10	mA
	(any one output)			
Packaged Device	Operating Temperature	Top	0 to 70	C
	Storage Temperature	Tst	-55 to +150	C
	Power Dissipation	Pd	1	W

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DC ELECTRICAL CHARACTERISTICS T_A = 25 Deg C				
PARAMETER	**CONDITIONS**	**MIN**	**MAX**	**UNIT**
IL (HV+)	Test #1		50	uA
IL (F+Com)	Test #2		15	nA
IL (PD 0-7)	Test #3		80	nA
IL (S+)	Test #4		15	nA
IL (S-)	Test #5		15	nA
IL (F-)	Test #6		15	nA
IS-	Test # 7		1	mA
IS-	Test #8		100	nA
Ron TF+	Test #10		200	ohms
Ron TF-	Test #11		220	ohms
Ron S+	Test #12		2	k ohms
Ron S-	Test #13		2.2	k ohms
Vdd		8	10	V
Idd			100	uA
Vih	Logic hi	7		V
Vil	Logic lo		3	V
Iin		-1	+1	uA
Cin			10	pf

AC ELECTRICAL CHARACTERISTICS T_A = 25 Deg C				
PARAMETER	**CONDITIONS**	**MIN**	**MAX**	**UNIT**
tRS setup	Rs to CS*	30		ns
tRS hold	Rs after CS*		30	ns
tD setup	Dx to CS*	40		ns
tD hold	Dx after CS*		40	ns
tCS* width		30		ns
t wait	CS* to +HV	200		ns
t settle	HV+ to CS*	200		ns
t slew	HV+ ^ to PDx	2		us
t per	HV+ to HV+ ^	5		us

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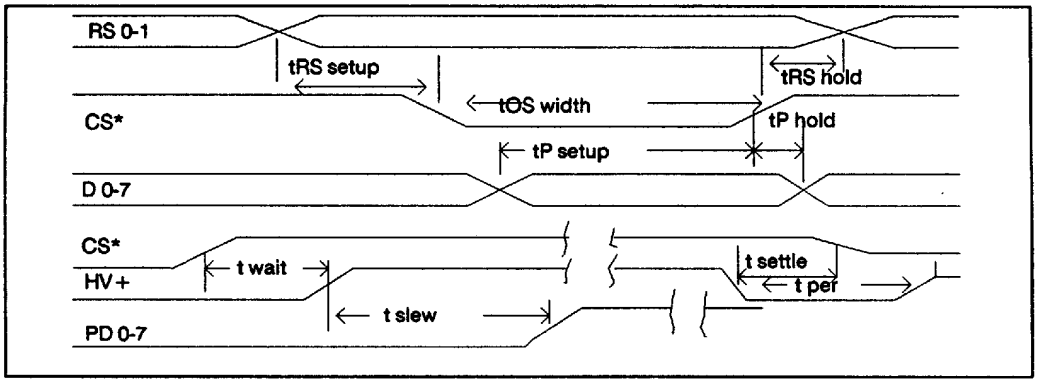
Timing Diagram



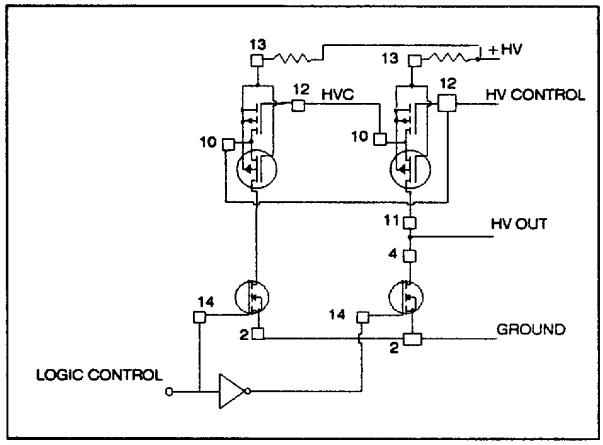
TEST CONSIDERATIONS

Test #1 verifies the leakage in the internal level shifters by putting 400V on the HV+ rail with all switches off. This allows the user to calculate the amount of current needed for those devices that will take leakage current from the HV+ line. Test #2 uses the HV+ and also applies 385V to the F+ pin to test the F+com transistor for leakage. Again, this will test for leakage current from the F+ force line on those chips not actively powering the test board. Test #3 has the F+com closed and one of the f+ switches on, with the other 7 off. This is the conditions of of powering the point under test with the leakage point returns on another chip(s). Test #4 uses the same forcing configuration and checks the s+ transistor leakage by measuring the current at the S+ node. Test #5 repeats this for s- leakage and test #6 for the f- switch. The resultant leakage currents will be used to maintain the programmed current within the allowable range or in contributing an error to the measurement in the case of sense lines.

HIGH VOLTAGE LEVEL SHIFTER

In order to drive the devices associated with the upper power rail of the chip (Fcom, S+, & f+), one must shift the control signals up to ths high voltage node. This would be done with a resistor inverter in discrete circuitry. However, in integrated form this would cause undue power dissipation, (e.g. 1mA at 250V would cause a quarter watt times the number of stages). A more practical way has been developed and patented by Universal. Using a pair of low voltage P channel transistors, a pair of high voltage P & N channel push-pull stages with the low voltage control line and its inversion, the signal is shifted up to the high voltage with no DC power. This is a practical demonstration of an integrated approach to high voltage electronics in applications like this pin driver (see illustration).

High Voltage Level Shifter



SYSTEM USAGE

The primary application for the USH5053 HIVIC is in "bareboard" and cable test equipment where it is used to insure that no leakage paths exist. In addition, the boards may be tested for continuity from point to point. In this mode a Kelvin contact is available to eliminate on resistance variations of the internal switches. A variation on the leakage test using rapidly programmed signals to simulate AC will allow for a coupling measurement.

Power connections to the unit are required in the form of +10 volts for the logic, a high voltage rampable power supply to the test level, and the HV+ supply rail that must be 15 volts above the test voltage. A ramped supply must be used because of the possibilty of encountering a short on the test board. Sensing should detect the the current being drawn and stop when the current/power becomes excessive. The

current available in the high voltage mode should be limited to no more than 2mA during the ramp. This will protect those parts of the circuit that are subject to power dissipation. Low voltage (less than 50V) tests will allow the maximum 25mA. Either a single supply with this compliance or two supplies should be used.

Certain features have been included in the chip to enhance the test operation. For the continuity tests, KElvin testing has been configured. A constant current source would be used to supply the stimulus through th F+ node to the F- node at ground potential. The S+ and S- nodes would be used to measure the voltage drop through the unknown resistance of the path. This configuration will minimize the effects of the contact resistance of the various transistors. By using this method, the circuit is more practical to integrate. Careful design has been used to to keeo leakage currents to tha lowest feasible value. This becomes very critical due to the thousands of test points involved. One must account for all these in the total system design.

NOMENCLATURE

Considerations in device usage is explained in the following comments on test configurations. In this section the following nomenclature will be used: 1) HV+ is a power supply that should ride 15V above programmed facing voltage; 2) F+ is the high voltage test (forcing) voltage that is ramped up for the test; 3) S+ is the sense line to the more positive side; 4) S- is the lower sense line; 5) F- is the lower forcing voltage line; 6) the transistor from the F+ line is the F+ com device (reduces leakage currents by isolating all non-driving devices from the high voltage and through the level shifting circuit keeps this internal rail at near ground); 7) f+ is the transistor from the internal F+ rail to the pad; 8) f- is the transistor from the pad to the F- rail; 9) s+ is the transistor from the pad to the S+ rail; 10) F-com is a transistor in series with the f- transistors and the F- line.

RS 0-1 Register Selection Table

RS1	RS0	Data Operation
0	1	Dx to Force latches
1	0	Dx to Sense latches
1	1	Dx to polarity latches
0	0	All latches reset

Configuration at each PD Pad